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Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C646xx
RAM Size	8K x 8
Interface	I²C, USB, USART
Number of I/O	32
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64613-80nc

Endpoint data is serviced either directly by the 8051, or moved on or off-chip using the DMA system built into the CY7C646xx. Bulk data is available in 64-byte random-access buffers that can also be addressed as a FIFO using the special AutoPointer feature. Each endpoint has a unique interrupt vector. This allows ISRs (Interrupt Service Routines) automatically to be called with minimum overhead and latency, simply by including the ISR address in an interrupt jump table.

2.4 Default USB Machine

When the CY7C64613 is plugged into USB with no EEPROM attached to its I^2C port (but **with** the SCL and SDA pull-ups installed), the intelligent SIE enumerates as a generic USB device with the following characteristics:

ID bytes (hex)

VID (Vendor ID)	0547
PID (Product ID)	2235
DID (Device ID)	0000

Default Endpoints

Endpoint	Type	Alternate Setting		
		0	**1**	**2**
		Max Packet Size (bytes)		
0	CTL	64	64	64
1 IN	INT	0	16	64
2 IN	BULK	0	64	64
2 OUT	BULK	0	64	64
4 IN	BULK	0	64	64
4 OUT	BULK	0	64	64
6 IN	BULK	0	64	64
6 OUT	BULK	0	64	64
8 IN	ISO	0	16	256
8 OUT	ISO	0	16	256
9 IN	ISO	0	16	16
9 OUT	ISO	0	16	16
10 IN	ISO	0	16	16
10 OUT	ISO	0	16	16

Powering up with default USB characteristics allows code to be written without initial consideration of the enumeration code that establishes the default USB device, speeding the learning process.

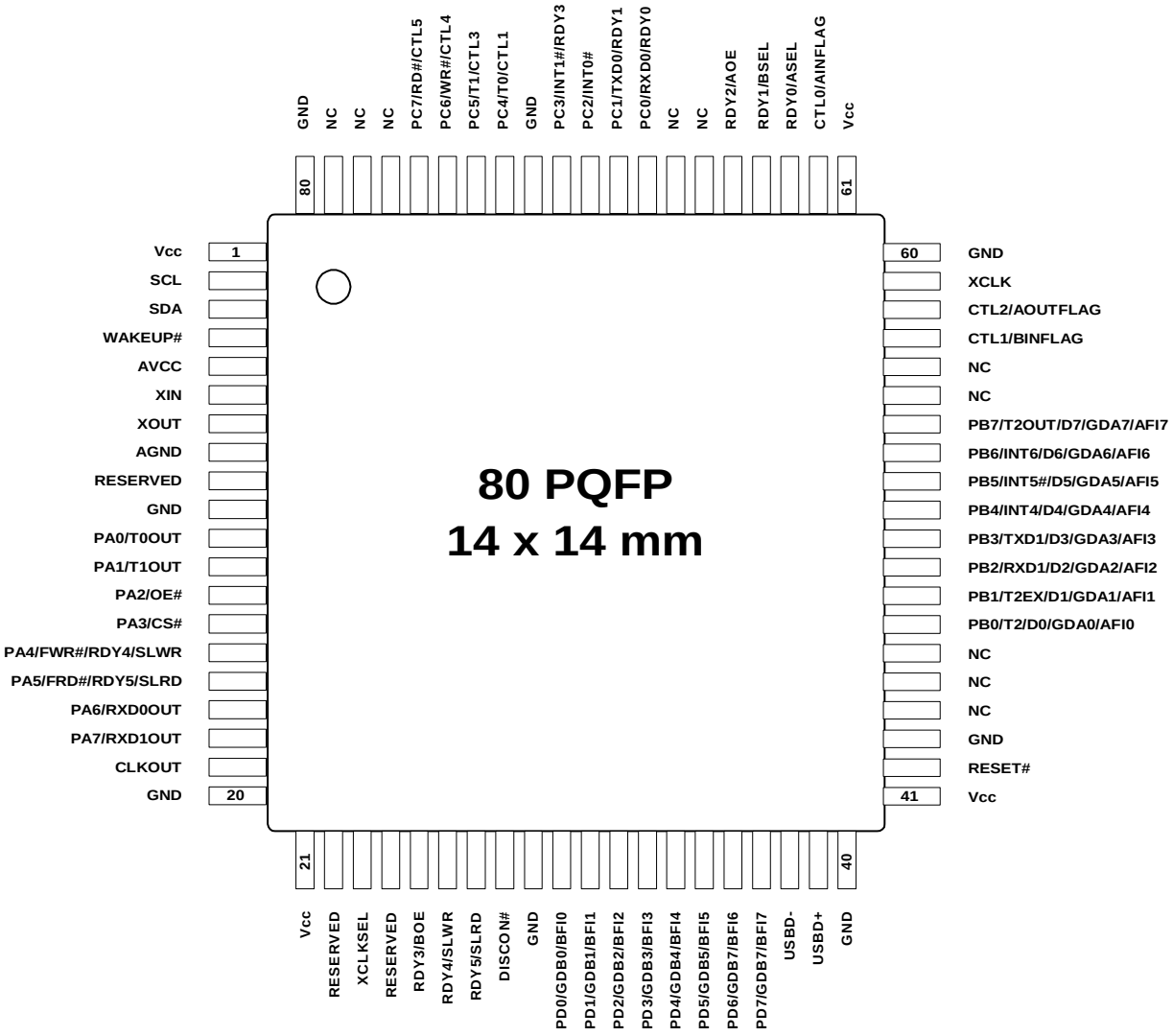
2.5 IBN (In-Bulk-NAK) Interrupts

The CY7C646xx has an interrupt that indicates that an IN token has been received by an endpoint, and the SIE has NAK'd the transfer due to no data being available in the endpoint buffer. Interrupt request bits are provided for endpoints EP1N through EP7IN, and a previously reserved vector is added to the USB vectored interrupts.

2.6 Slave FIFOs

Many high-bandwidth USB designs use a FIFO between the USB interface chip and external logic to match data rates, or to smooth the USB data delivery (which, being packet oriented, occurs in bursts). The CY7C646xx moves this glue logic into the part by providing four 64-byte internal slave FIFOs. The FIFOs also provide two important interface functions, external clocking and bus width conversion.

Using external clocking, external logic (such as a DSP or ASIC) can clock data into or out of the slave FIFOs under control of its own clock, rather than synchronizing with the clock supplied by the CY7C646xx (24 or 48 MHz). The FIFOs can be controlled


80 PQFP
14 x 14 mm
1 Vcc
2 SCL
3 SDA
4 WAKEUP#
5 AVCC
6 XIN
7 XOUT
8 AGND
9 RESERVED
10 GND
11 PA0/T0OUT
12 PA1/T1OUT
13 PA2/OE#
14 PA3/CS#
15 PA4/FWR#/RDY4/SLWR
16 PA5/FRD#/RDY5/SLRD
17 PA6/RXD0OUT
18 PA7/RXD1OUT
19 CLKOUT
20 GND
21 Vcc
22 RESERVED
23 XCLKSEL
24 RESERVED
25 RDY3/BOE
26 RDY4/SLWR
27 RDY5/SLRD
28 DISCON#
29 GND
30 PD0/GDB0/BFI0
31 PD1/GDB1/BFI1
32 PD2/GDB2/BFI2
33 PD3/GDB3/BFI3
34 PD4/GDB4/BFI4
35 PD5/GDB5/BFI5
36 PD6/GDB7/BFI6
37 PD7/GDB7/BFI7
38 USBD-
39 USBD+
40 GND
41 Vcc
42 RESET#
43 GND
44 PB0/T2/D0/GDA0/AFI0
45 PB1/T2EX/D1/GDA1/AFI1
46 PB2/RXD1/D2/GDA2/AFI2
47 PB3/TXD1/D3/GDA3/AFI3
48 PB4/INT4/D4/GDA4/AFI4
49 PB5/INT5#/D5/GDA5/AFI5
50 PB6/INT6/D6/GDA6/AFI6
51 PB7/T2OUT/D7/GDA7/AFI7
52 NC
53 NC
54 NC
55 NC
56 XCLK
57 GND
58 CTL0/AINFLAG
59 RDY0/ASEL
60 RDY1/BSEL
61 RDY2/AOE
62 NC
63 NC
64 PC0/RXD0/RDY0
65 PC1/TXD0/RDY1
66 PC2/INT0#
67 PC3/INT1#/RDY3
68 GND
69 PC4/T0/CTL1
70 PC5/T1/CTL3
71 PC6/WR#/CTL4
72 PC7/RD#/CTL5
73 NC
74 NC
75 NC
76 GND
77 CTL1/BINFLAG
78 CTL2/AOUTFLAG
79 NC
80 GND

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
65	38	24	USBD–	I/O/Z	Z	**USB D– Signal**. Connect to the USB D– signal through a 24Ω resistor.
66	39	25	USBD+	I/O/Z	Z	**USB D+ Signal**. Connect to the USB D+ pin through a 24Ω resistor.
105			A0	Output	L	**8051 Address Bus**. This bus is driven at all times. When the 8051 is addressing internal RAM it reflects the internal address. During DMA transfers that use the RD# and WR# strobes, the address bus contains the incrementing DMA source or destination address for data transferred over D[7..0].
106			A1	Output	L	
107			A2	Output	L	
108			A3	Output	L	
114			A4	Output	L	
115			A5	Output	L	
116			A6	Output	L	
117			A7	Output	L	
118			A8	Output	L	
120			A9	Output	L	
121			A10	Output	L	
122			A11	Output	L	
127			A12	Output	L	
128			A13	Output	L	
1			A14	Output	L	
2			A15	Output	L	
8			D0	I/O/Z	Z	**8051 Data Bus**. This bidirectional bus is high-impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is also used for DMA transfers that use the RD#/FRD#, WR#,FWR# pins as strobes. The data bus is active only for external bus accesses, and is driven LOW in suspend.
9			D1	I/O/Z	Z	
10			D2	I/O/Z	Z	
11			D3	I/O/Z	Z	
13			D4	I/O/Z	Z	
14			D5	I/O/Z	Z	
15			D6	I/O/Z	Z	
16			D7	I/O/Z	Z	
33			PSEN#	Output	H	**Program Store Enable**. This active-LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x1B40-0xFFFF when the EA pin is LOW, or from 0x0000-0xFFFF when the EA pin is HIGH.
41			BKPT	Output	L	**Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the USBBAV register (BPEN=1). If the BPPULSE bit in the USBBAV register is HIGH, this signal pulses HIGH for eight 24-/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the USBBAV register.
69	42	28	RESET#	Input	N/A	**Active LOW Reset**. Resets the entire chip. This pin is normally tied to V_{CC} through a 10K resistor, and to GND through a 1-µF capacitor. Hysteresis input.
51			EA	Input	N/A	**External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x1B3F. If EA=0 the 8051 fetches this code from its internal RAM. IF EA=1 the 8051 fetches this code from external memory.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
19	6	6	XIN	Input	N/A	**Crystal Input**. Connect this signal to a 12-MHz series-resonant, fundamental mode crystal and 22–33 pF capacitor to GND. Also connect a 1-MΩ resistor between XIN and XOUT.
20	7	7	XOUT	Output	N/A	**Crystal Output**. Connect this signal to a 12-MHz series-resonant, fundamental mode crystal and 22–33 pF capacitor to GND. Also connect a 1-MΩ resistor between XIN and XOUT.
34	19	12	CLKOUT	O/Z	24 MHz	24- or 48-MHz clock, phase locked to the 12-MHz input clock. Output frequency is set by an external EEPROM bit (Config0.2). If no EEPROM is connected to the I^2C port (but the required pull-up resistors are present), the 8051 defaults to 24-MHz operation. The 8051 may three-state this output by setting CPUCS.1=1. The CLKOUT pin may be inverted by setting the boot EEPROM bit CONFIG0.1=1.
Port A						
25	11		PA0 or T0OUT	I/O/Z	I (PA0)	Multiplexed pin whose function is selected by two bits: PORTACFG.0 and IFCONFIG.3. **PA0** is a bidirectional IO port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
26	12		PA1 or T1OUT	I/O/Z	I (PA1)	Multiplexed pin whose function is selected by two bits: PORTACFG.1 and IFCONFIG.3. **PA1** is a bidirectional IO port pin. **T1OUT** is an active-HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.
27	13		PA2 or OE# or	I/O/Z	I (PA2)	Multiplexed pin whose function is selected by two bits: PORTACFG.2 and IFCONFIG.3. **PA2** is a bidirectional IO port pin. **OE#** is an active-LOW output enable for external memory. If the OE# pin is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive (high) at power-on.
28	14		PA3 or CS#	I/O/Z	I (PA3)	Multiplexed pin whose function is selected by the PORTACFG.3 bit. **PA3** is a bidirectional I/O port pin. **CS#** is an active-LOW chip select for external memory. If the CS# pin is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive (HIGH) at power-on.
29	15	10	PA4 or FWR# or RDY4 or SLWR	I/O/Z	I (PA4)	Multiplexed pin whose function is selected by the following bits: PORTACFG.4, PORTACF2.4, and IFCONFIG[1..0]. **PA4** is a bidirectional I/O port pin. **FWR#** is the write strobe output for an external FIFO connected to the data bus D[7..0]. If the FWR# pin is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive at power-on. **RDY4** is a GPIF input signal. **SLWR** is the write strobe input for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
30	16	11	PA5 or FRD# or RDY5 or SLRD	I/O/Z	I (PA5)	Multiplexed pin whose function is selected by the following bits: PORTACFG.5, PORTACF2.5, and IFCONFIG[1..0]. **PA5** is a bidirectional I/O port pin. **FRD#** is the write strobe output for an external FIFO connected to the data bus D[7..0]. If the FRD# pin is used, it should be externally pulled up to V_{CC} to ensure that the read strobe is inactive at power-on. **RDY5** is a GPIF input signal. **SLRD** is the read strobe input for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].
31	17		PA6 or RXD0OUT	I/O/Z	I (PA6)	Multiplexed pin whose function is selected by the PORTACFG.6 bit. **PA6** is a bidirectional I/O port pin. **RXD0OUT** is an active-HIGH signal from 8051 UART0. If RXD0OUT is selected and UART0 is in mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1.
32	18		PA7 or RXD1OUT	I/O/Z	I (PA7)	Multiplexed pin whose function is selected by the PORTACFG.7 bit. **PA7** is a bidirectional I/O port pin. **RXD1OUT** is an active-HIGH output from 8051 UART1. When RXD1OUT is selected and UART1 is in mode 0, this pin provides the output data for UART1 only when it is in sync mode. In modes 1, 2, and 3, this pin is HIGH.
Port B						
						The following descriptions apply to the PORT B pins: **D[7..0]** is the 8051 data bus. This bus is optionally available on PORT B pins to provide access to the 8051 data bus in smaller EZ-USB II packages that do not bring out the 8051 address and data buses. **GDA[7..0]** is the GPIF A data bus. **AFI[7..0]** is the bidirectional A-FIFO data bus.
79	47	29	PB0 or T2 or D[0] or GDA[0] or AFI [0]	I/O/Z	I (PB0)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.0 and IFCONFIG[1..0]. **PB0** is a bidirectional I/O port pin. **T2** is the active-HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2=1. When C/T2=0, Timer2 does not use this pin. **AFI [0]** is the bidirectional A-FIFO data bus.
80	48	30	PB1 or T2EX or D[1] or GDA[1] or AFI [1]	I/O/Z	I (PB1)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.1 and IFCONFIG[1..0]. **PB1** is a bidirectional I/O port pin. **T2EX** is an active-HIGH input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON. **AFI [1]** is the bidirectional A-FIFO data bus.
81	49	31	PB2 or RXD1 or D[2] or GDA[2] or AFI [2]	I/O/Z	I (PB2)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.2 and IFCONFIG[1..0]. **PB2** is a bidirectional I/O port pin. **RXD1**is an active-HIGH input signal for 8051 UART1, which provides data to the UART in all modes. **AFI [2]** is the bidirectional A-FIFO data bus.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
82	50	32	PB3 or TXD1 or D[3] or GDA[3] or AFI [3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.3 and IFCONFIG[1..0]. **PB3** is a bidirectional I/O port pin. **TXD1**is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode. **AFI [3]** is the bidirectional A-FIFO data bus.
83	51	33	PB4 or INT4 or D[4] or GDA[4] or AFI [4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.4 and IFCONFIG[1..0]. **PB4** is a bidirectional I/O port pin. **INT4** is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH. **AFI [4]** is the bidirectional A-FIFO data bus.
84	52	34	PB5 or INT5# or D[5] or GDA[5] or AFI [5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.5 and IFCONFIG[1..0]. **PB5** is a bidirectional I/O port pin. **INT5#** is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW. **AFI [5]** is the bidirectional A-FIFO data bus.
85	53	35	PB6 or INT6 or D[6] or GDA[6] or AFI [6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.6 and IFCONFIG[1..0]. **PB6** is a bidirectional I/O port pin. **INT6** is the 8051 INT5 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH. **AFI [6]** is the bidirectional A-FIFO data bus.
86	54	36	PB7 or T2OUT or D[7] or GDA[7] or AFI [7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.7 and IFCONFIG[1..0]. **PB7** is a bidirectional I/O port pin. **T2OUT** is the active-HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows. **AFI [7]** is the bidirectional A-FIFO data bus.
Port C						
110	68	43	PC0 or RXD0 or RDY0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by the PORTCCFG.0 and PORTCGPIF.0 bits. **PC0** is a bidirectional I/O port pin. **RXD0** is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes. **RDY0** is a GPIF input signal.
111	69	44	PC1 or TXD0 or RDY1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by the PORTCCFG.1 and PORTCGPIF.1 bits. **PC1** is a bidirectional I/O port pin. **TXD0** is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode. **RDY1** is a GPIF input signal.
112	70	45	PC2 or INT0#	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by the PORTCCFG.2 bit. **PC2** is a bidirectional I/O port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
113	71	46	PC3 or INT1# or RDY3	I/O/Z	I (PC3)	Multiplexed pin whose function is selected by the: PORTCCFG.3 and PORTCGPIF.3 bits. **PC3** is a bidirectional I/O port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0). **RDY3** is a GPIF input signal.

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
781D	ABPOLAR	FIFO Control Signals Polarity	0	0	BOE	AOE	SLRD	SLWR	ASEL	BSEL
781E	ABFLUSH	Write (data=x) to reset all flags	*	*	*	*	*	*	*	*
781F-7823 (reserved)										
7824	WFSELECT	Waveform Selector	SINGLEWR		SINGLERD		FIFOWR		FIFORD	
7825	IDLE_CS	GPIF IDLE State control	DONE	0	0	0	0	0	0	IDLEDRV
7826	IDLECTLOUT	GPIF IDLE CTL states	IOE3	IOE2	IOE1/ CTL5	IOE0/ CTL4	CTL3	CTL2	CTL1	CTL0
7827	CTLOUTCFG	GPIF CTL Drive mode	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0
7828-7829 (reserved)										
782A	GPIFADRL	GPIF Address	*	*	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
782B (reserved)										
782C	AINTC	FIFO A In Transfer Count	FITC	Transfer Count						
782D	AOUTTC	FIFO A Out Transfer Count	FITC	Transfer Count						
782E	ATRIG	Trigger a FIFO A RD/WR	*	*	*	*	*	*	*	*
782F (reserved)										
7830	BINTC	FIFO B In Transfer Count	FITC	Transfer Count						
7831	BOUTTC	FIFO B Out Transfer Count	FITC	Transfer Count						
7832	BTRIG	Trigger a FIFO B RD/WR	*	*	*	*	*	*	*	*
7833 (reserved)										
7834	SGLDATH	GPIF Data High	D15	D14	D13	D12	D11	D10	D9	D8
7835	SGLDATLTRIG	GPIF Data Low and Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7836	SGLDATLN-TRIG	GPIF Data Low and No Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7837(reserved)										
7838	READY	GPIF Ready flags	INTRDY	SAS	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
7839	ABORT	Abort current GPIF cycle	*	*	*	*	*	*	*	*
783A (reserved)										
783B	GENIE	GPIF/DMA Interrupt Enable	0	0	0	0	0	DMADN	GPWR	GPDONE
783C	GENIRQ	GPIF/DMA Interrupt Request	0	0	0	0	0	DMADN	GPWR	GPDONE
783D-7840 (reserved)										
	IO Ports D, E									
7841	OUTD	Output Port D	OUTD7	OUTD6	OUTD5	OUTD4	OUTD3	OUTD2	OUTD1	OUTD0
7842	PINSD	Input Port D pins	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
7843	OED	Port D Output Enable	0ED7	0ED6	0ED5	0ED4	0ED3	0ED2	0ED1	0ED0
7844 (reserved)										
7845	OUTE	Output Port E	OUTE7	OUTE6	OUTE5	OUTE4	OUTE3	OUTE2	OUTE1	OUTE0
7846	PINSE	Input Port E pins	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0
7847	OEE	Port E Output Enable	OEE7	OEE6	OEE5	OEE4	OEE3	OEE2	OEE1	OEE0
7848 (reserved)										
7849	PORTSETUP	Timer0 Clock source, Port-to-SFR mapping	0	0	0	0	0	0	T0CLK	SFRPORT
784A	IFCONFIG	Select 8/16 bit data bus, configure buses (IF)	52ONE	0	0	0	GSTATE	BUS16	IF1	IF0
784B	PORTACF2	Port A Configuration #2	0	0	SLRD	SLWR	0	0	0	0

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7F65	OUT13DATA	Endpoint 13 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F66	OUT14DATA	Endpoint 14 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F67	OUT15DATA	Endpoint 15 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F68	IN8DATA	Endpoint 8 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F69	IN9DATA	Endpoint 9 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6A	IN10DATA	Endpoint 10 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6B	IN11DATA	Endpoint 11 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6C	IN12DATA	Endpoint 12 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6D	IN13DATA	Endpoint 13 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6E	IN14DATA	Endpoint 14 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6F	IN15DATA	Endpoint 15 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
	Isochronous Byte Counts									
7F70	OUT8BCH	EP8 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F71	OUT8BCL	EP8 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F72	OUT9BCH	EP9 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F73	OUT9BCL	EP9 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F74	OUT10BCH	EP10 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F75	OUT10BCL	EP10 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F76	OUT11BCH	EP11 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F77	OUT11BCL	EP11 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F78	OUT12BCH	EP12 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F79	OUT12BCL	EP12 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7A	OUT13BCH	EP13 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7B	OUT13BCL	EP13 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7C	OUT14BCH	EP14 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7D	OUT14BCL	EP14 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7E	OUT15BCH	EP15 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7F	OUT15BCL	EP15 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F80-7F91 (reserved)										
	CPU Registers									
7F92	CPUCS	Control & Status	rv3	rv2	rv1	rv0	24/48	CLKINV	CLKOUT OE	8051RES
7F93	PORTACFG	Port A Configuration	RxD1out	RxD0out	FRD	FWR	CS	OE	T1out	T0out
7F94	PORTBCFG	Port B Configuration	T2OUT	INT6	INT5	INT4	TxD1	RxD1	T2EX	T2
7F95	PORTCCFG	Port C Configuration	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0
	Input-Output Port Registers									
7F96	OUTA	Output Register A	OUTA7	OUTA6	OUTA5	OUTA4	OUTA3	OUTA2	OUTA1	OUTA0
7F97	OUTB	Output Register B	OUTB7	OUTB6	OUTB5	OUTB4	OUTB3	OUTB2	OUTB1	OUTB0
7F98	OUTC	Output Register C	OUTC7	OUTC6	OUTC5	OUTC4	OUTC3	OUTC2	OUTC1	OUTC0
7F99	PINSA	Port Pins A	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0
7F9A	PINSB	Port Pins B	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
7F9B	PINSC	Port Pins C	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0
7F9C	OEA	Output Enable A	OEA7	OEA6	OEA5	OEA4	OEA3	OEA2	OEA1	OEA0
7F9D	OEB	Output Enable B	OEB7	OEB6	OEB5	OEB4	OEB3	OEB2	OEB1	OEB0

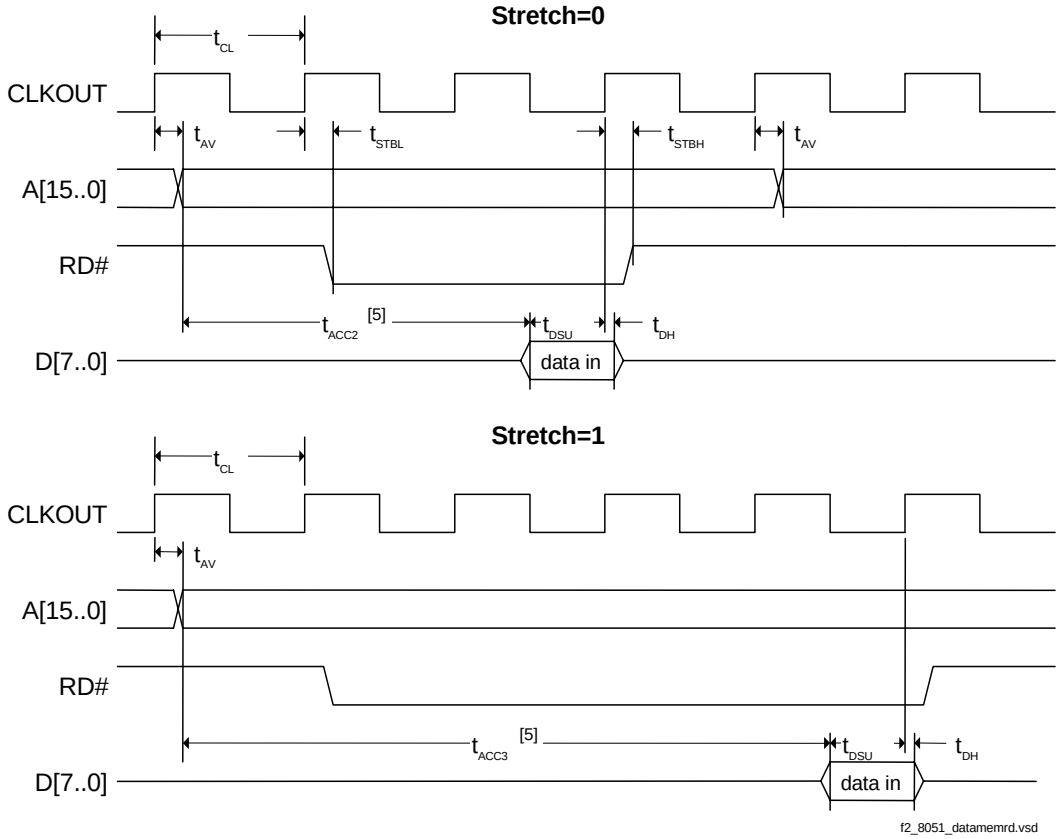
4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7F9E	OEC	Output Enable C	OEC7	OEC6	OEC5	OEC4	OEC3	OEC2	OEC1	OEC0
7F9F	UART230	230k Baud Configuration	0	0	0	0	0	0	UART1	UART0
	Isochronous Control/Status Registers									
7FA0	ISOERR	ISO OUT Endpoint Error	ISO15 ERR	ISO14 ERR	ISO13 ERR	ISO12 ERR	ISO11 ERR	ISO10 ERR	ISO9 ERR	ISO8 ERR
7FA1	ISOCTL	Isochronous Control	*	*	*	*	PPSTAT	0	0	ISODISAB
7FA2	ZBCOUT	Zero Byte Count bits	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8
7FA3 (reserved)										
7FA4 (reserved)										
	I^2C Registers									
7FA5	I2CS	Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE
7FA6	I2DAT	Data	d7	d6	d5	d4	d3	d2	d1	d0
7FA7	I2CMODE	STOP Int Enable, I^2C bus speed	0	0	0	0	0	0	STOPIE	400KHZ
	Interrupts									
7FA8	IVEC	Interrupt Vector	0	IV4	IV3	IV2	IV1	IV0	0	0
7FA9	IN07IRQ	EPIN Interrupt Request	IN7IR	IN6IR	IN5IR	IN4IR	IN3IR	IN2IR	IN1IR	IN0IR
7FAA	OUT07IRQ	EPOUT Interrupt Request	OUT7IR	OUT6IR	OUT5IR	OUT4IR	OUT3IR	OUT2IR	OUT1IR	OUT0IR
7FAB	USBIRQ	USB Interrupt Request	0	0	IBNIR	URESIR	SUSPIR	SUTOKIR	SOFIR	SUDAVIR
7FAC	IN07IEN	EP0–7IN Int Enables	IN7IEN	IN6IEN	IN5IEN	IN4IEN	IN3IEN	IN2IEN	IN1IEN	IN0IEN
7FAD	OUT07IEN	EP0–7OUT Int Enables	OUT7IEN	OUT6IEN	OUT5IEN	OUT4IEN	OUT3IEN	OUT2IEN	OUT1IEN	OUT0IEN
7FAE	USBIEN	USB Int Enables	0	0	IBNIE	URESIE	SUSPIE	SUTOKIE	SOFIE	SUDAVIE
7FAF	USBBAV	Breakpoint & Autovector	*	*	*	INT2SFC	BREAK	BPPULSE	BPEN	AVEN
7FB0	IBNID	IN-Bulk-NAK ID	EP7IN	EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN
7FB1	IBNMASK	IN-Bulk-NAK Intr. mask	EP7IN	EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN
7FB2	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8
7FB3	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0
	Bulk Endpoints 0–7									
7FB4	EP0CS	Control & Status	*	*	*	*	OUTBSY	INBSY	HSNAK	EP0STALL
7FB5	IN0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FB6	IN1CS	Control & Status	*	*	*	*	*	*	in1bsy	in1stl
7FB7	IN1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FB8	IN2CS	Control & Status	*	*	*	*	*	*	in2bsy	in2stl
7FB9	IN2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBA	IN3CS	Control & Status	*	*	*	*	*	*	in3bsy	in3stl
7FBB	IN3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBC	IN4CS	Control & Status	*	*	*	*	*	*	in4bsy	in4stl
7FBD	IN4BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBE	IN5CS	Control & Status	*	*	*	*	*	*	in5bsy	in5stl
7FBF	IN5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC0	IN6CS	Control & Status	*	*	*	*	*	*	in6bsy	in6stl
7FC1	IN6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC2	IN7CS	Control & Status	*	*	*	*	*	*	in7bsy	in7stl
7FC3	IN7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC4 (reserved)										

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7FC5	OUT0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC6	OUT1CS	Control & Status	*	*	*	*	*	*	out1bsy	out1stl
7FC7	OUT1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC8	OUT2CS	Control & Status	*	*	*	*	*	*	out2bsy	out2stl
7FC9	OUT2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FCA	OUT3CS	Control & Status	*	*	*	*	*	*	out3bsy	out3stl
7FCB	OUT3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FCC	OUT4CS	Control & Status	*	*	*	*	*	*	out4bsy	out4stl
7FCD	OUt4BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FCE	OUT5CS	Control & Status	*	*	*	*	*	*	out5bsy	out5stl
7FCF	OUT5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FD0	OUT6CS	Control & Status	*	*	*	*	*	*	out6bsy	out6stl
7FD1	OUT6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FD2	OUT7CS	Control & Status	*	*	*	*	*	*	out7bsy	out7stl
7FD3	OUT7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC5	OUT0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC6	OUT1CS	Control & Status	*	*	*	*	*	*	out1bsy	out1stl
	Global USB Registers									
7FD4	SUDPTRH	Setup Data Ptr H	A15	A14	A13	A12	A11	A10	A9	A8
7FD5	SUDPTRL	Setup Data Ptr L	A7	A6	A5	A4	A3	A2	A1	A0
7FD6	USBCS	USB Control & Status	WakeSRC	*	*	*	DisCon	DiscOE	ReNum	SIGR-SUME
7FD7	TOGCTL	Toggle Control	Q	S	R	IO	0	EP2	EP1	EP0
7FD8	USBFRAMEL	Frame Number L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
7FD9	USBFRAMEH	Frame Number H	0	0	0	0	0	FC10	FC9	FC8
7FDA (reserved)										
7FDB	FNADDR	Function Address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0
7FDC (reserved)										
7FDD	USBPAIR	Endpoint Control	ISOsend0	*	PR6OUT	PR4OUT	PR2OUT	PR6IN	PR4IN	PR2IN
7FDE	IN07VAL	Input Endpoint 0–7 valid	IN7VAL	IN6VAL	IN5VAL	IN4VAL	IN3VAL	IN2VAL	IN1VAL	1
7FDF	OUT07VAL	Output Endpoint 0–7 valid	OUT7VAL	OUT6VAL	OUT5VAL	OUT4VAL	OUT3VAL	OUT2VAL	OUT1VAL	1
7FE0	INISOVAL	Input EP 8–15 valid	IN15VAL	IN14VAL	IN13VAL	IN12VAL	IN11VAL	IN10VAL	IN9VAL	IN8VAL
7FE1	OUTISOVAL	Output EP 8–15 valid	OUT15VAL	OUT14VAL	OUT13VAL	OUT12VAL	OUT11VAL	OUT10VAL	OUT9VAL	OUT8VAL
7FE2	FASTXFR	Fast Transfer Mode	FISO	FBLK	RPOL	RMOD1	RMOD0	WPOL	WMOD1	WMOD0
7FE3	AUTOPTRH	Auto-Pointer H	A15	A14	A13	A12	A11	A10	A9	A8
7FE4	AUTOPTRL	Auto-Pointer L	A7	A6	A5	A4	A3	A2	A1	A0
7FE5	AUTODATA	Auto Pointer Data	D7	D6	D5	D4	D3	D2	D1	D0
7FE6-7FE7 (reserved)										
	Setup Data									
7FE8	SETUPDAT	8 bytes of SETUP data	d7	d6	d5	d4	d3	d2	d1	d0
	Isochronous FIFO Sizes									
7FF0	OUT8ADDR	Endpt 8 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF1	OUT9ADDR	Endpt 9 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF2	OUT10ADDR	Endpt 10 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0

9.3 Data Memory Read



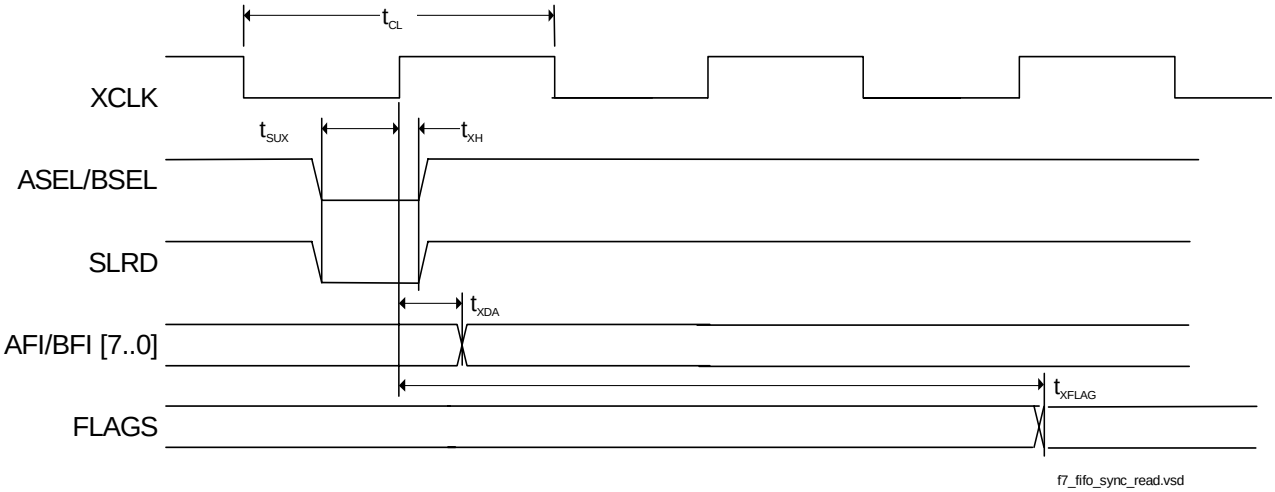
Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		41.66		ns	24 MHz
			20.83		ns	48 MHz
t_{AV}	Delay from Clock to Valid Address	0		10	ns	
t_{STBL}	Clock to RD Low	0		8	ns	
t_{STBH}	Clock to RD High	0		8	ns	
t_{DSU}	Data Set-up to Clock			10	ns	
t_{DH}	Data Hold Time	0			ns	

Note:

5. t_{ACC2} and t_{ACC3} are computed from the above parameters as follows:
   t_{ACC2}(24 MHz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 106 ns
   t_{ACC2}(48 Mhz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 44 ns

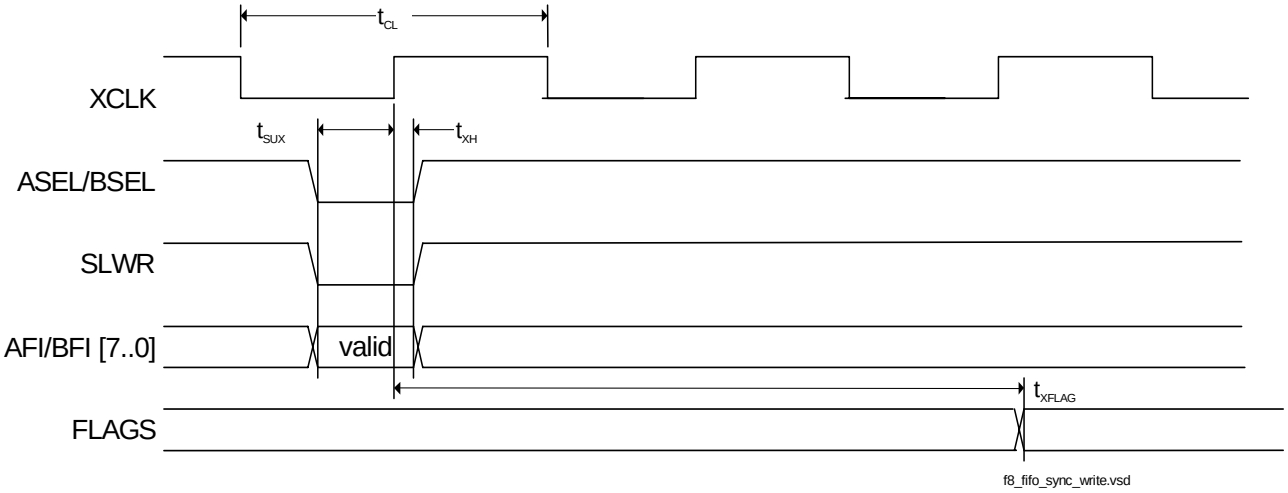
   t_{ACC3}(24 MHz) = $5*t_{CL} - t_{AV} - t_{DSU}$ = 188 ns
   t_{ACC3}(48 Mhz) = $5*t_{CL} - t_{AV} - t_{DSU}$ = 85 ns

9.8 Slave FIFOs—Synchronous Read



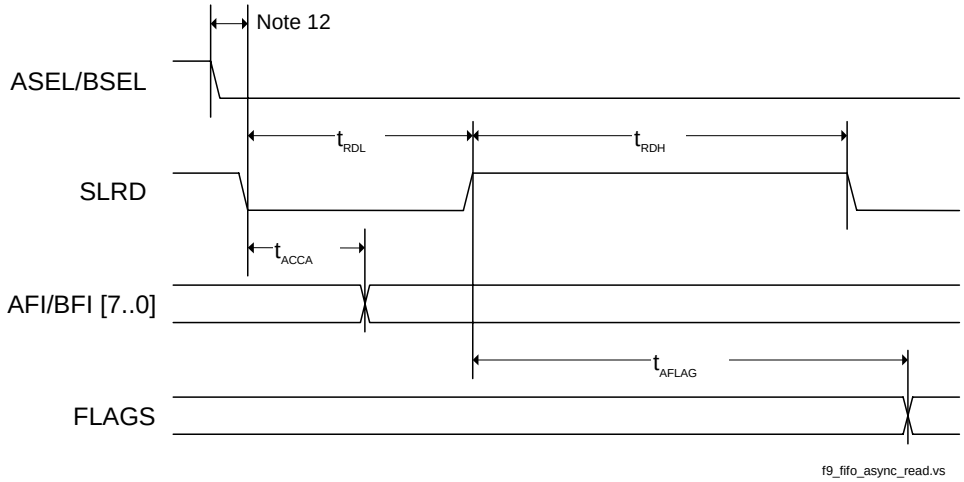
Parameter	Description	Min.	Max.	Unit
t_{SUX}	Strobe & Sel to External Clock Set-up Time		9	ns
t_{XH}	External Clock to Strobe & Sel Hold Time	6		ns
t_{XDA}	Clock to A/B FIFO data		13	ns
t_{XFLAG}	Clock to FIFO flag		$2t_{CL}$+11	ns

9.9 Slave FIFOs—Synchronous Write



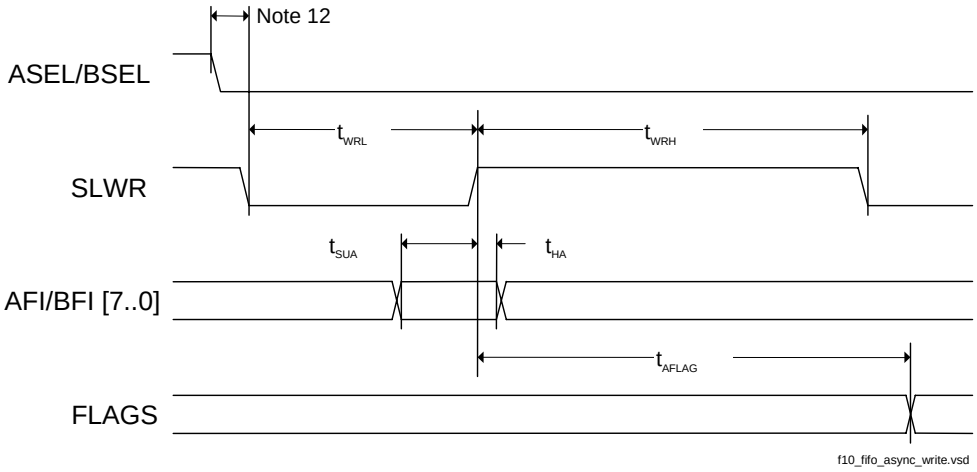
Parameter	Description	Min.	Typ.	Max.	Unit
t_{CL}	CLKOUT Period		41.66		ns
			20.83		ns
t_{SUX}	Sel, Strobe & Data Set-up to External Clock			9	ns
t_{XH}	External Clock to Sel, Strobe & Data Hold Time	2			ns
t_{XFLAG}	External Clock to FIFO Flag			$2t_{CL}$+11	ns

9.10 Slave FIFOs—Asynchronous Read[10, 11]



Parameter	Description	Min.	Max.	Unit	Notes
t_{RDL}	SLRD strobe active	30		ns	
t_{RDH}	SLRD strobe inactive		70	ns	
			90	ns	double byte mode
t_{ACCA}	Read active to FIFO data valid		40	ns	
t_{AFLAG}	SLRD inactive to FIFO flag		95	ns	

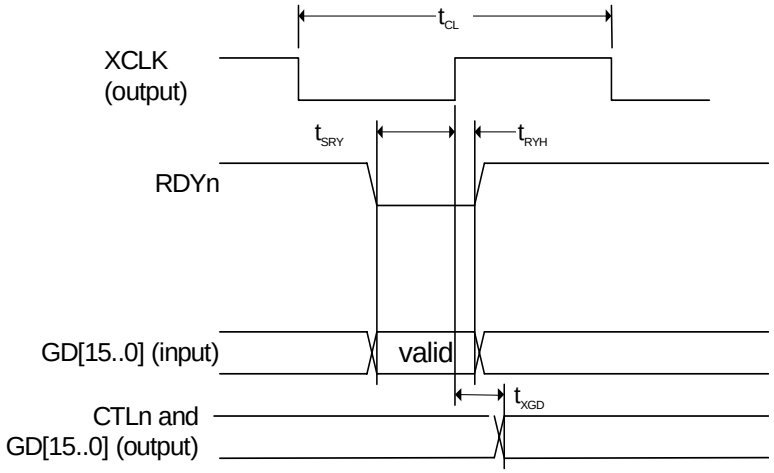
9.11 Slave FIFOs—Asynchronous Write[10, 11]



Parameter	Description	Min.	Max.	Unit
t_{WRL}	Slave Write Strobe Active	30		ns
t_{WRH}	Slave Write Strobe Inactive	70		ns
t_{SUA}	Async Data Set-up Time to Write Strobe Inactive	10		ns
t_{HA}	Async Data Hold Time to Write Strobe Inactive	5		ns
t_{AFLAG}	Async Write Strobe Inactive to FIFO Flag Valid		95	ns

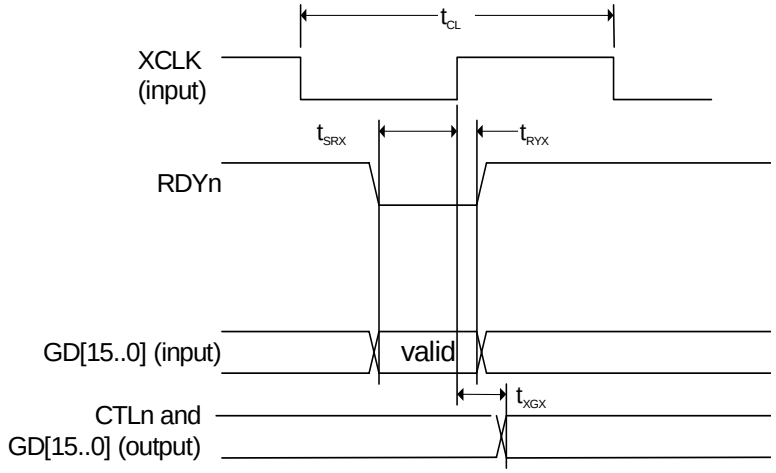
Notes:
10. The timing diagram assumes OEA/OEB is active.
11. The read operation begins when both A/BSEL and SLRD are active, and ends when either is inactive.
12. The polarities of ASEL/BSEL and SLRD are programmable. Active-LOW is shown.

9.12 GPIF Signals (Internally Clocked)



Parameter	Description	Min.	Max.	Unit
t_{SRY}	RDYn and GPIF Data to External Clock Set-up Time		9	ns
t_{RYH}	External Clock to RDYn and GPIF Data Hold Time	2		ns
t_{XGD}	Clock to GPIF Data and CTLn output		13	ns

9.13 GPIF Signals (Externally Clocked)



Parameter	Description	Min.	Max.	Unit
t_{SRX}	RDYn and GPIF Data to External Clock Set-up Time		9	ns
t_{RYX}	External Clock to RDYn and GPIF Data Hold Time	2		ns
t_{XGX}	Clock to GPIF Data and CTLn output		13	ns

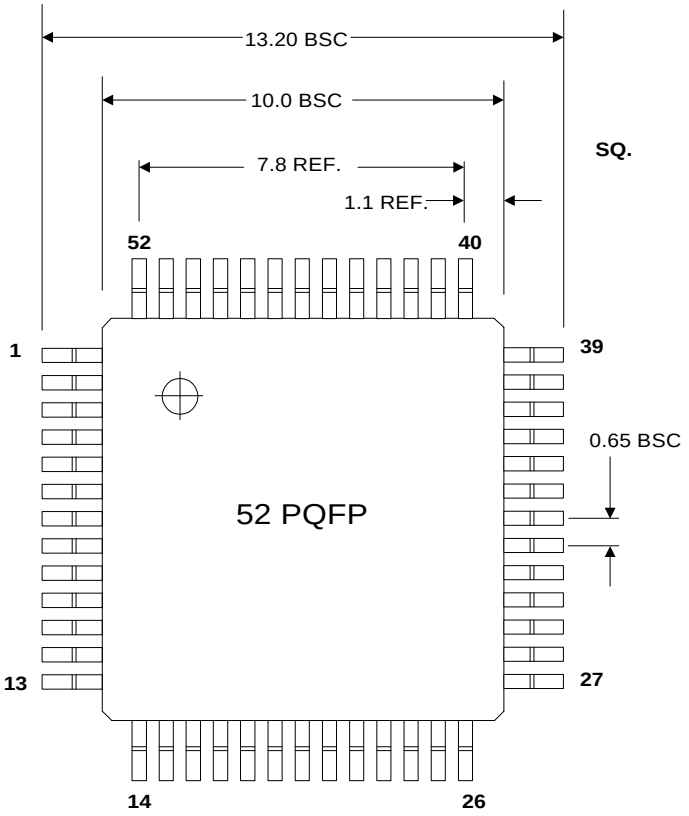
Note:
13. t_{cl} for an XCLK input must be greater than 20.83 ns.

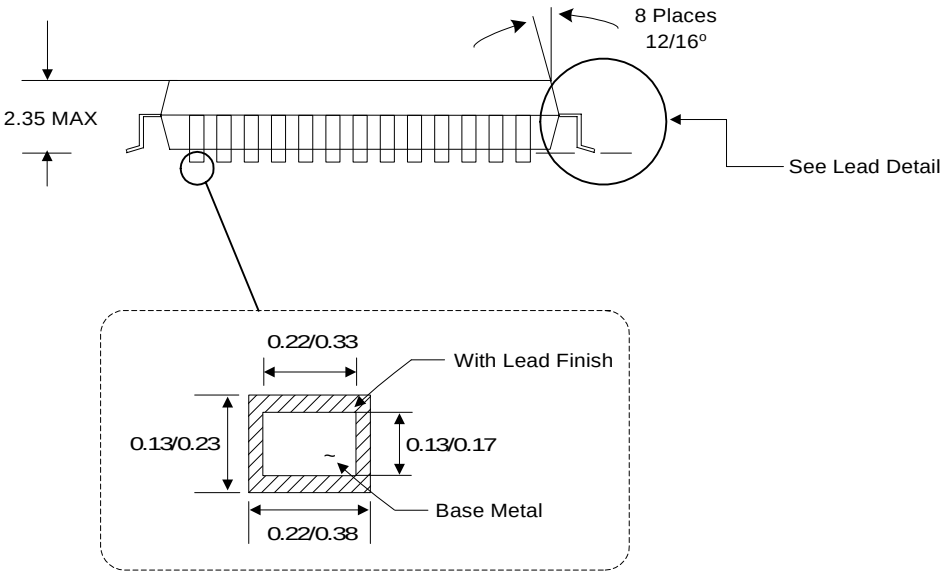
10.0 Ordering Information

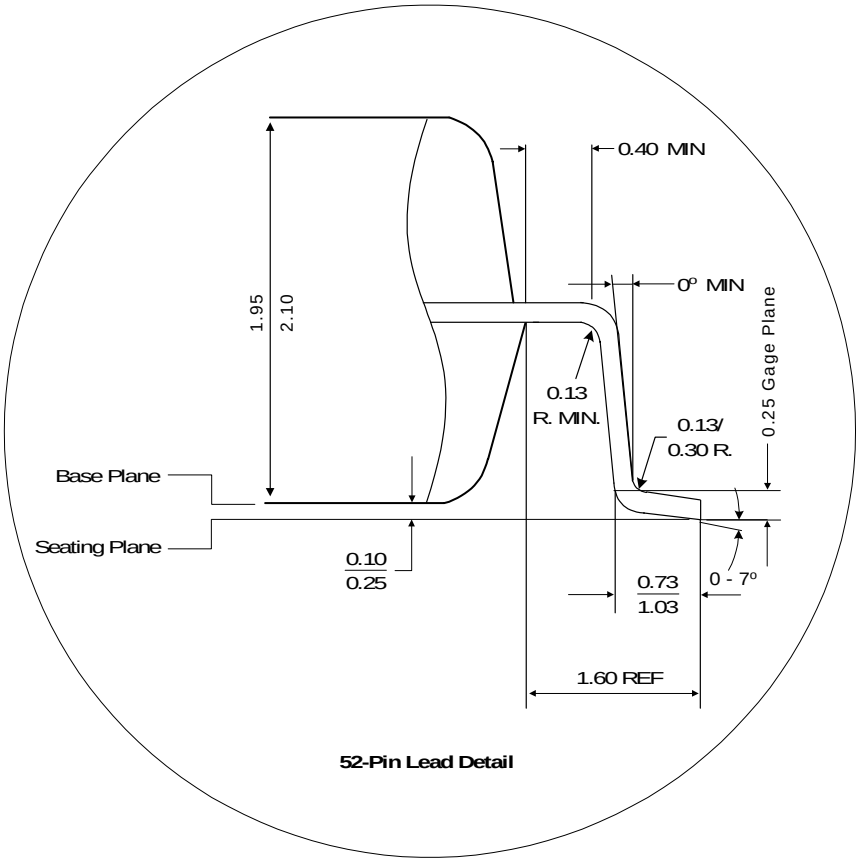
Part Number	Package Type	RAM Size	Burst I/O Rate (Bytes/sec)	# Prog I/Os	Dataport	Isochronous Support
CY7C64601-52NC	52 PQFP	4K	48 Mbytes	16	8-bit	No
CY7C64603-52NC	52 PQFP	8K	48 Mbytes	16	8-bit	No
CY7C64613-52NC	52 PQFP	8K	48 Mbytes	16	8-bit	Yes
CY7C64603-80NC	80 PQFP	8K	96 Mbytes	32	16-bit	No
CY7C64613-80NC	80 PQFP	8K	96 Mbytes	32	16-bit	Yes
CY7C64603-128NC	128 PQFP	8K	96 Mbytes	40	16-bit + Addr	No
CY7C64613-128NC	128 PQFP	8K	96 Mbytes	40	16-bit + Addr	Yes
EZ-USB FX Xcelerator Development Kit	CY3671					

11.0 Package Diagrams

11.1 52 PQFP

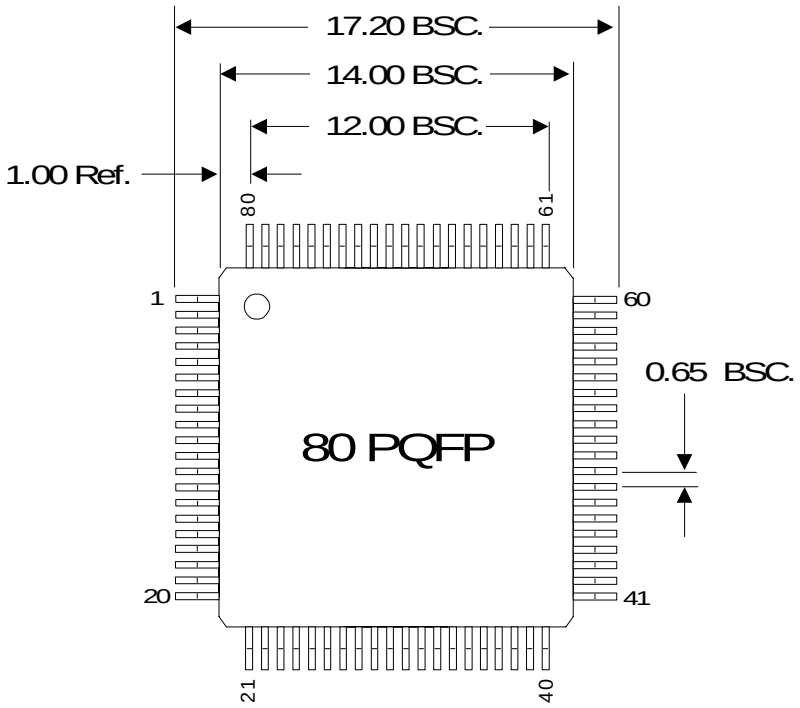


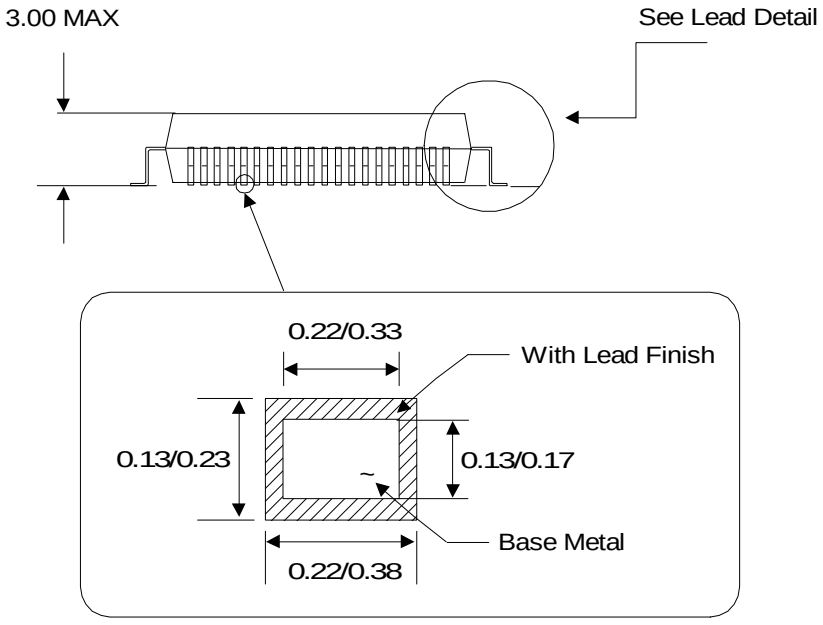




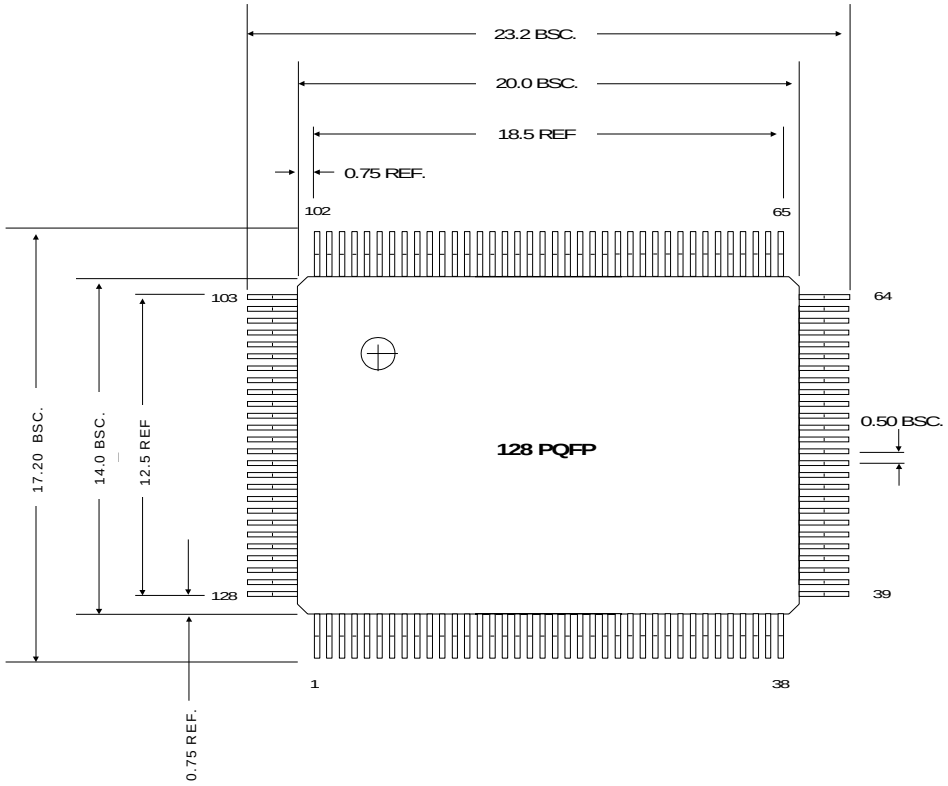
52-Pin Lead Detail

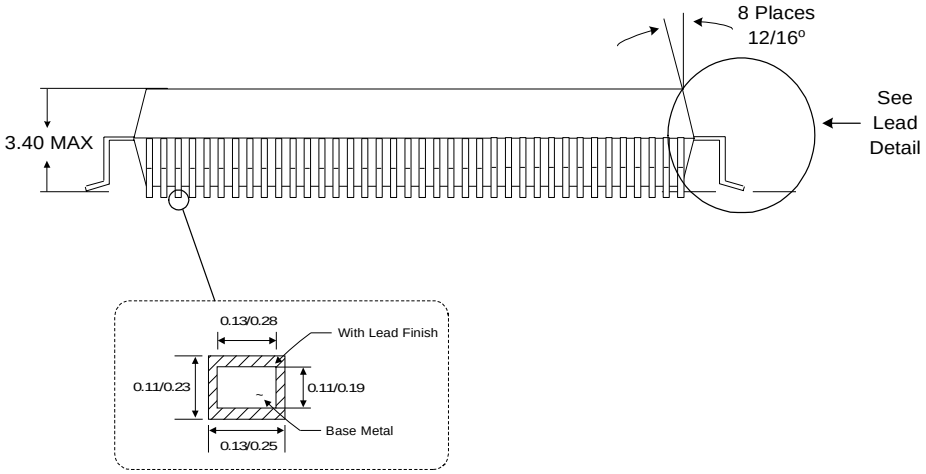
11.2 80 PQFP

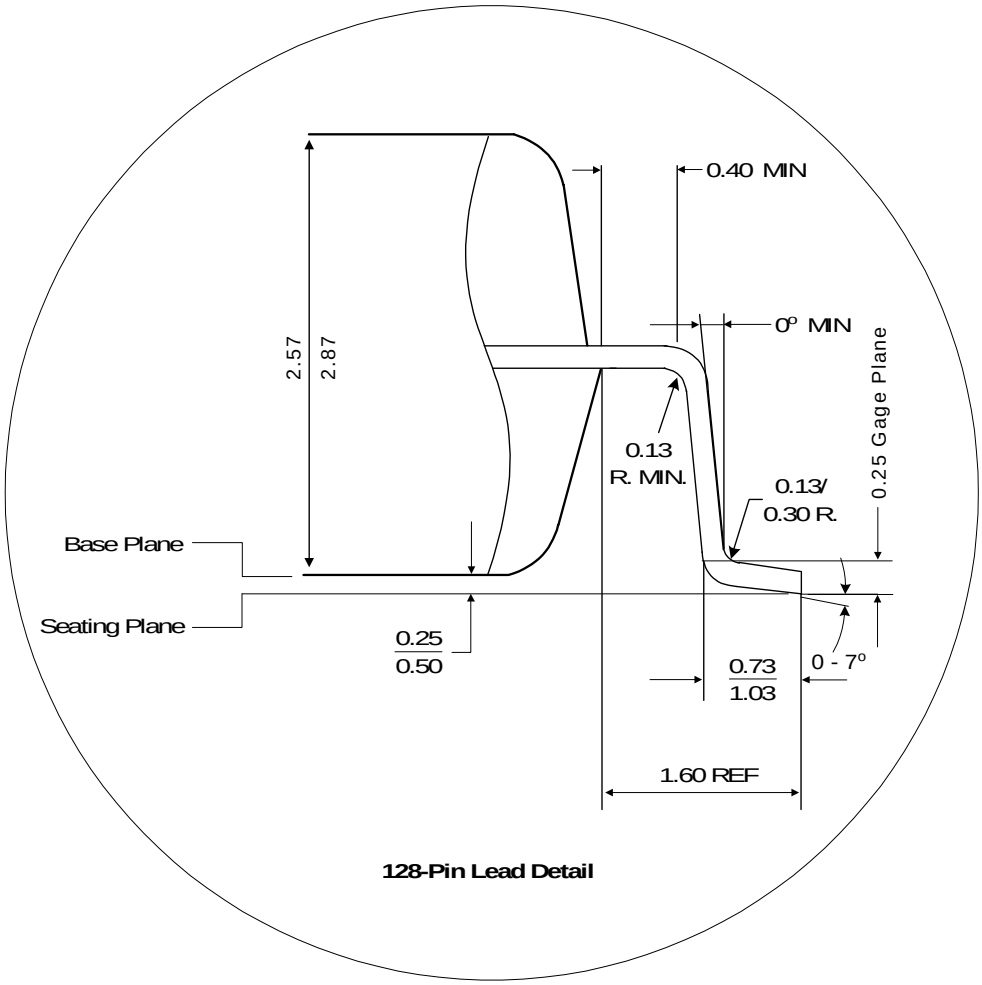

17.20 BSC.
14.00 BSC.
12.00 BSC.
1.00 Ref.
80
61
1
60
0.65 BSC.
80 PQFP
20
41
21
40


3.00 MAX
See Lead Detail
0.22/0.33
With Lead Finish
0.13/0.23
0.13/0.17
Base Metal
0.22/0.38

11.3 128 PQFP


23.2 BSC.
20.0 BSC.
18.5 REF
0.75 REF.
102
65
103
64
128 PQFP
0.50 BSC.
17.20 BSC.
14.0 BSC.
12.5 REF
128
39
1
38
0.75 REF.


8 Places
12/16°
See
Lead
Detail
3.40 MAX
0.13/0.28
With Lead Finish
0.11/0.23
0.11/0.19
Base Metal
0.13/0.25



128-Pin Lead Detail

Document Title: CY7C64601/CY7C64603/CY7C64613 EZ USB FX USB Microcontroller Document Number: 38-08005				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110206	11/11/01	SZV	Change from Spec number: 38-00903 to 38-08005