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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	SmartCard, SPI, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	46
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5122d-rdrim

USB Smart Card Reader Using the AT83C5123 Version

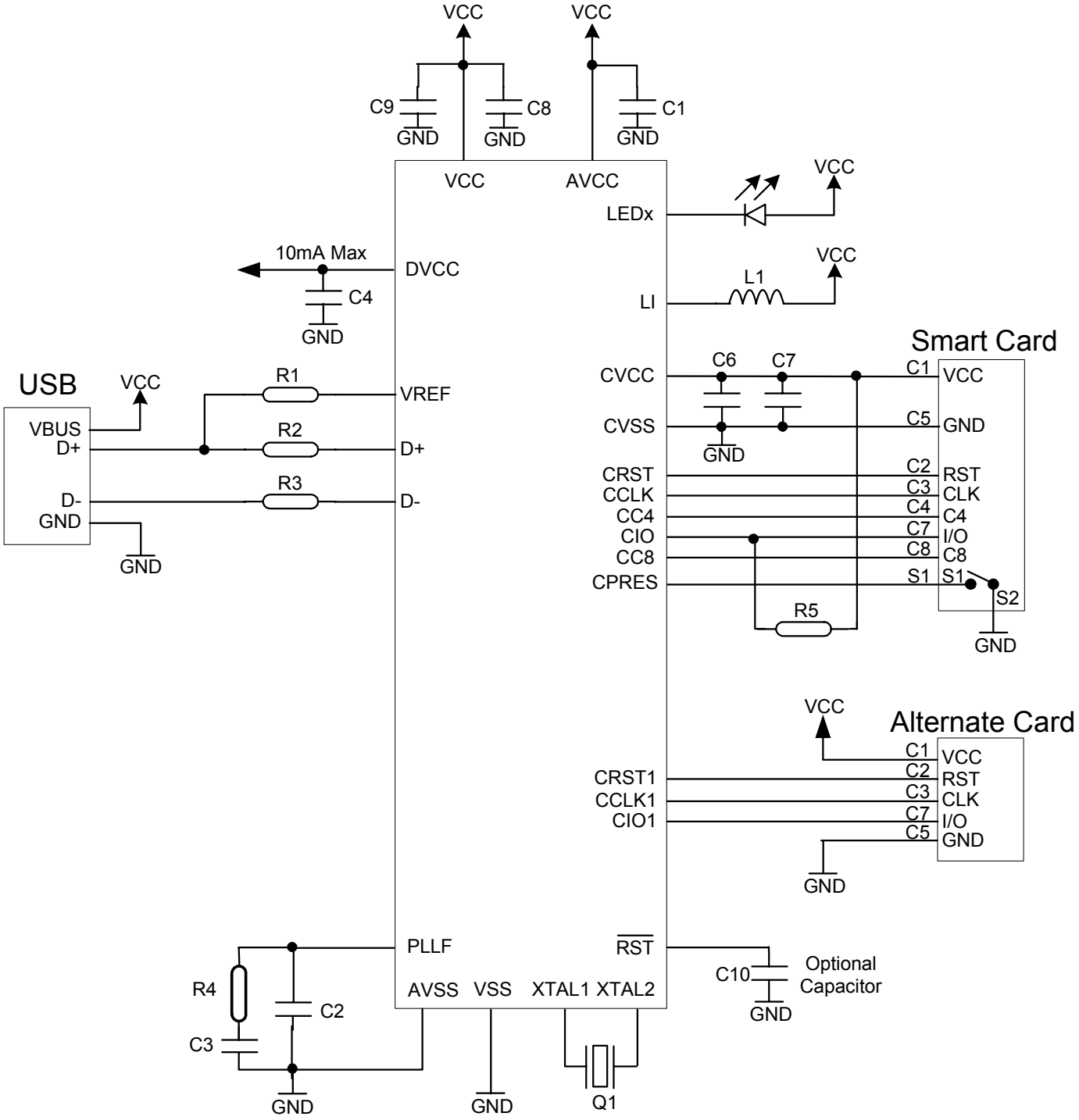


Table 8. CRAM Configuration Register - RCON (D1h)

7	6	5	4	3	2	1	0
-	-	-	-	RPS	-	-	-

Bit Number	Bit Mnemonic	Description
7 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
3	RPS	**CRAM Memory Mapping Bit** Set to map the CRAM memory during MOVX instructions Clear to map the XRAM memory during MOVX. This bit has priority over the EXTRAM bit.
2-0	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.

Reset Value = XXXX 0XXXb

AT8xC5122's CRAM and E2PROM Versions

The AT8xC5122's CRAM and E2PROM versions implements :

- 32 KB of ROM mapped from 8000 to FFFF in which is embedded a bootloader for In-System Programming feature

- 32 KB of CRAM (Code RAM) , a volatile program memory mapped from 0000 to 7FFF

In CRAM versions only :

- 512 bytes of E2PROM can be optionally implemented to store permanent data

In E2PROM version :

- 32KB of E2PROM are implemented to store permanent code

Warnings :

– some bytes of user program memory space are reserved for bootloader configuration. Depending on the configuration, up to 256 bytes of code may be not available for the user code from 7F00h location. Refer to bootloader datasheet for further details.

– Port P3.7 may be used by the bootloader as a hardware condition at reset to select the In-System Programming mode. Once the bootloader has started, the P3.7 Port is no more used.

Table 18. SCIB SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCICLK	C1h	Smart Card Frequency Prescaler Register	XTSCS(1)		SCICLK5-0					

Note: 1. Only for AT8xC5122

Table 19. DC/DC SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
DCCKPS	BFh	DC/DC Converter Reload Register	MODE	OVFADJ	BOOST[1-0]		DCCKPS3-0			

Table 20. Keyboard SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBF(1)	9Eh	Keyboard Flag Register	KBE7 - 0							
KBE(1)	9Dh	Keyboard Input Enable Register	KBF7 - 0							
KBLS(1)	9Ch	Keyboard Level Selector Register	KBLS7 - 0							

Note: 1. Only for AT8xC5122

Table 21. SPI SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON(1)	C3h	Serial Peripheral Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA(1)	C4h	Serial Peripheral Status-Control	SPIF	WCOL		MODF				
SPDAT(1)	C5h	Serial Peripheral Data	R7 - 0							

Notes: 1. Only for AT8xC5122

Table 22. USB SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
USBCON	BCh	USB Global Control	USBE	SUSPCLK	SDRMWUP	DETACH	UPRSM	RMWUPE	CONFG	FADDEN
USBADDR	C6h	USB Address	FEN	UADD6-0						
USBINT	BDh	USB Global Interrupt			WUPCPU	EORINT	SOFINT			SPINT
USBIEN	BEh	USB Global Interrupt Enable			EWUPCPU	EEORINT	ESOFINT			ESPINT
UEPNUM	C7h	USB Endpoint Number					EPNUM3-0			
UEPCONX	D4h	USB Endpoint X Control	EPEN	NAKIEN	NAKOUT	NAKIN	DTGL	EPDIR	EPTYPE1	EPTYPE0
UEPSTAX	CEh	USB Endpoint X Status	DIR	RXOUTB1	STALLRQ	TXRDY	STL/CRC	RXSETUP	RXOUTB0	TXCMP
UEPRST	D5h	USB Endpoint Reset		EP6RST	EP5RST	EP4RST	EP3RST	EP2RST	EP1RST	EP0RST
UEPINT	F8h	USB Endpoint Interrupt		EP6INT	EP5INT	EP4INT	EP3INT	EP2INT	EP1INT	EP0INT

Registers

Table 36. Port Mode Register 0 - PMOD0 (91h) for AT8xC5122

7	6	5	4	3	2	1	0
P3C1	P3C0	P2C1	P2C0	CPRESRES	-	P0C1	P0C0

Bit Number	Bit Mnemonic	Description
7 - 6	P3C1-P3C0	**Port 3 Configuration bits (Applicable to P3.0, P3.1, P3.3, P3.4 only)** **00** Quasi bi-directional **01** Push-pull **10** Output Low Speed **11** Input with weak pull-up
5-4	P2C1-P2C0	**Port 2 Configuration bits** **00** Quasi bi-directional **01** Push-pull **10** Output Low Speed **11** Input with weak pull-down
3	CPRESRES	**Card Presence Pull-up resistor** Cleared to connect the internal 100K pull-up Set to disconnect the internal pull-up
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1-0	P0C1-P0C0	**Port 0 Configuration bits** **00** C51 Standard P0 **01** Reserved **10** Output Low Speed **11** Push-pull

Reset Value = 0000 0x00b

Table 37. Port Mode Register 0 - PMOD0 (91h) for AT83C5123

7	6	5	4	3	2	1	0
P3C1	P3C0	-	-	CPRESRES	-	-	-

Bit Number	Bit Mnemonic	Description
7 - 6	P3C1-P3C0	**Port 3 Configuration bits (Applicable to P3.0, P3.1, P3.3, P3.4 only)** **00** Quasi bi-directional **01** Push-pull **10** Output Low Speed **11** Input with weak pull-up
5-4		**Reserved** The value read from these bits are indeterminate. Do not set these bit.
3	CPRESRES	**Card Presence Pull-up resistor** Cleared to connect the internal 100K pull-up Set to disconnect the internal pull-up
2-0	-	**Reserved** The value read from these bits are indeterminate. Do not set these bit.

Reset Value = 00xx 0xxxb

Smart Card Interface Block (SCIB)

The SCIB provides all signals to interface directly with a smart card. The compliance with the ISO7816, EMV'2000, GSM and WHQL standards has been certified.

Both synchronous (e.g. memory card) and asynchronous smart cards (e.g. microprocessor card) are supported. The component supplies the different voltages requested by the smart card. The power off sequence is directly managed by the SCIB.

The card presence switch of the smart card connector is used to detect card insertion or card removal. In case of card removal, the SCIB de-activates the smart card using the de-activation sequence. An interrupt can be generated when a card is inserted or removed.

Any malfunction is reported to the microcontroller (interrupt + control register).

The different operating modes are configured by internal registers.

- Support of ISO/IEC 7816
- character mode
- one transmit/receive buffer
- 11 bits ETU counter
- 9 bits guard time counter
- 32 bits waiting time counter
- Auto character repetition on error signal detection in transmit mode
- Auto error signal generation on parity error detection in receive mode
- Power on and power off sequence generation
- Manual mode to drive directly the card I/O

ATR Answer To Reset. Response from the ICC to a Reset initiated by the Terminal

F and D F = Clock Rate Conversion Factor, D = Bit rate adjustment factor. ETU is defined as : ETU = F/(D*f) with f = Card Clock frequency. If f is in Hertz, ETU is in second. F and D are available in the ATR (byte TA1). The default values are F=372, D=1.

Guard Time The time between 2 leading edges of the start bit of 2 consecutive characters is comprised of the character duration (10) plus the guard time. Be aware that the Guard Time counter and the Guard Time registers in the AT8xC5122/23 consider the time between 2 consecutive characters. So the equation is Guard Time Counter = Guard Time + 10. In other words, the Guard Time is the number of Stop Bits between 2 characters sent in the same direction.

Extra Guard Time ISO IEC 7816-3 and EMV introduce the Extra Guard time to be added to the minimum Guard Time. Extra Guard Time only apply to consecutive characters sent by the terminal to the ICC. The TC1 byte in the ATR define the number N. For N=0 the character to character duration is 12 ETUs. For N=254 the character to character duration is 266. For N=255 (special case) The minimum character to character duration is to be used : 12 for T=0 protocol and 11 for T=1 protocol.

Block Guard Time The time between the leading edges of 2 consecutive characters sent in opposit direction. ISO IEC 7816-3 and EMV recommend a fixed Block Guard Time of 22 ETUs.

Work Waiting Time (WWT) In T=0 protocol WWT is the interval between the leading edge of any character sent by the ICC, and the leading edge of the previous character sent either by the ICC or the Terminal. If no character is received by the terminal after WWTmax time, the Terminal initiates a De-Activation Sequence.

Character Waiting Time (CWT) In T=1 protocol CWT is the interval between the leading edge of 2 consecutive characters sent by the ICC. If the next character is not received by the Terminal after CWTmax time, the Terminal initiates a De-Activation Sequence.

Block Waiting Time (BWT) In T=1 protocol BWT is the interval between the leading edge of the start bit of the last character sent by the Terminal that gives the right to sent to the ICC, and the leading edge of the start bit of the first character sent by the ICC. If the first character from the ICC is not received by the Terminal after BWTmax time, the Terminal initiates a De-Activation Sequence.

Waiting Time Extention (WTX) In T=1 protocol the ICC can request a Waiting Time Extension with a S(WTX request) request. The Terminal should acknowlege it. The Waiting time between the leading edge of the start bit of the last character sent by the Terminal that gives the right to sent to the ICC, and the leading edge of the start bit of the first character sent by the ICC will be BWT*WTX ETUs.

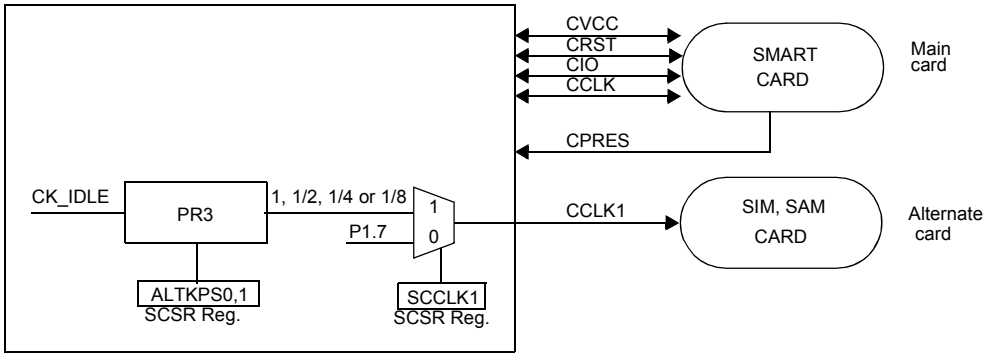
Parity error in T=0 protocol In T=0 protocol, a Terminal (respectively an ICC) detecting a parity error while receiving a character shall force the Card IO line at 0 starting at 10.5 ETUs, thus reducing the first Guard bit by half the time. The Terminal (respectively an ICC) shall maintain a 0 for 1 ETU min and 2 ETUs max (according to ISO IEC) or to 2 ETUs (according to EMV). The ICC (respectively a Terminal) shall monitor the Card IO to detect this error signal then attempt to repeat the character. According to EMV, following a parity error the character can be repeated one time, if parity error is detected again this procedure can be repeated 3 more times. The same character can be transmitted 5 times in total. ISO

Alternate Card

A second card named ‘Alternate Card’ can be controlled.

The Clock signal CCLK1 can be adapted to the XTAL frequency. Thanks to the clock prescaler which can divide the frequency by 1, 2, 4 or 8. The bits ALTKPS0 and ALTKPS1 in SCSR Register are used to set this factor.

Figure 44. Alternate Card



Registers

There are fifteen registers to control the SCIB macro-cell. They are described from Table 58 to Table 45.

Some of the register widths are greater than a byte. Despite the 8 bits access provided by the BIU, the address mapping of this kind of register respects the following rule :

The Low significant byte register is implemented at the higher address.

This implementation makes access to these registers easier when using high level programming languages (C,C++).

Table 45. Smart Card Contacts Register - SCCON (S:ACh, SCRS=0)

7	6	5	4	3	2	1	0
CLK	-	CARDC8	CARDC4	CARDIO	CARDCLK	CARDRST	CARDVCC

Bit Number	Bit Mnemonic	Description
7	CLK	**Card Clock Selection** Clear this bit to use the Card CLK bit (CARDCLK bit below) to drive Card CLK (P1.4) pin. Set this bit to use CK_XTAL1 or CK_PLL signals for CK_ISO to drive the Card CLK pin (CCLK = P1.4 pin) **Note:** internal synchronization avoids glitches on the CLK pin when switching this bit.
6	-	**Reserved** This bit can be changed by software but the read value is indeterminate.
5	CARDC8	**Card C8** Clear this bit to drive a low level on the Card C8 pin (CC8 = P1.1 pin). Set this bit to set a high level on the Card C8 pin (CC8 = P1.1 pin).. The CC8 pin can be used as a pseudo bi-directional I/O when this bit is set. **Warning** : VCARDOK=1 (SCISR.4 bit) condition must be true to change the state of CC8 pin
4	CARDC4	**Card C4** Clear this bit to drive a low level on the Card C4 pin (CC4 = P1.3 pin). Set this bit to set a high level on the Card C4 pin (CC4 = P1.3 pin). The CC4 pin can be used as a pseudo bi-directional I/O when this bit is set. **Warning** : VCARDOK=1 (SCISR.4 bit) condition must be true to change the state of CC4 pin
3	CARDIO	**Card I/O** If UART bit is cleared in SCICR register, this bit enables the use of the Card IO pin (CIO = P1.0) as a C51 pseudo bi-directional port : To read from CIO (P1.0) port pin : set CARDIO (P1.0) bit then read CARDIO (P1.0) bit to have the CIO port value To write in CIO (P1.0) port pin : set CARDIO (P1.0) bit to write a 1 in CIO (P1.0) port pin , clear CARDIO (P1.0) bit to write a 0 in CIO (P1.0) port pin. **Warning** : VCARDOK=1 (SCISR.4 bit) condition must be true to change the state of CIO pin
2	CARDCLK	**Card CLK** When the CLK bit is cleared in SCCON Register, the value of this bit is driven to the Card CLK pin. **Warning** : VCARDOK=1 (SCISR.4 bit) condition must be true to change the state of Card CLK pin
1	CARDRST	**Card RST** Clear this bit to drive a low level on the Card RST pin. Set this bit to set a high level on the Card RST pin. **Warning** : VCARDOK=1 (SCISR.4 bit) condition must be true to change the state of Card RST pin
0	CARDVCC	**Card VCC Control** Clear this bit to desactivate the Card interface and set its power-off. The other bits of SCCON register have no effect while this bit is cleared. Set this bit to power-on the Card interface. The activation sequence should be handled by software.

Reset Value = 0X00 0000b

Table 49. Smart Card Selection Register - SCSR (S:ABh)

7	6	5	4	3	2	1	0
-	BGTEN	-	CREPSEL	ALTKPS1	ALTKPS0	SCCLK1	SCRS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
6	BGTEN	**Block Guard Time Enable** Set this bit to select the minimum interval between the leading edge of the start bits of the last character received from the ICC and the first character sent by the Terminal. The transfer of GT[8-0] value to the BGT counter is done on the rising edge of the BGTEN. Clear this bit to suppress the minimum time between reception and transmission.
5	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
4	CREPSEL	**Character repetition selection** Clear this bit to select 5 times transmission (1 original + 4 repetitions) before parity error indication (conform to EMV) Set this bit to select 4 times transmission (1 original + 3 repetitions) before parity error indication
3-2	ALTKPS1:0	**Alternate Card Clock prescaler factor** 00 ALTKPS = 0: prescaler factor equals 1 01 ALTKPS = 1: prescaler factor equals 2 10 ALTKPS = 2: prescaler factor equals 4 (reset value) 11 ALTKPS = 3: prescaler factor equals 8
1	SCCLK1	**Alternate card clock selection** Set to select the prescaled PR3 clock for CCLK1 (P1.7) pin Clear to select P1.7 port bit
0	SCRS	**Smart Card Register Selection** The SCRS bit selects which set of the SCIB registers is accessed.

Reset Value = X000 1000b

Table 50. Smart Card Transmit / Receive Buffer - SCIBUF (S:AA)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
-	-	**Smart Card Transmit / Receive Buffer** - A new byte can be written in the buffer to be transmitted on the I/O pin when SCTBE bit is set. The bits are sorted and copied on the I/O pin versus the active convention. - A new byte received from I/O pin is ready to be read when SCRI bit is set. The bits are sorted versus the active convention.

Reset Value = 0000 0000b

Figure 63. USB Interrupt Control Block Diagram

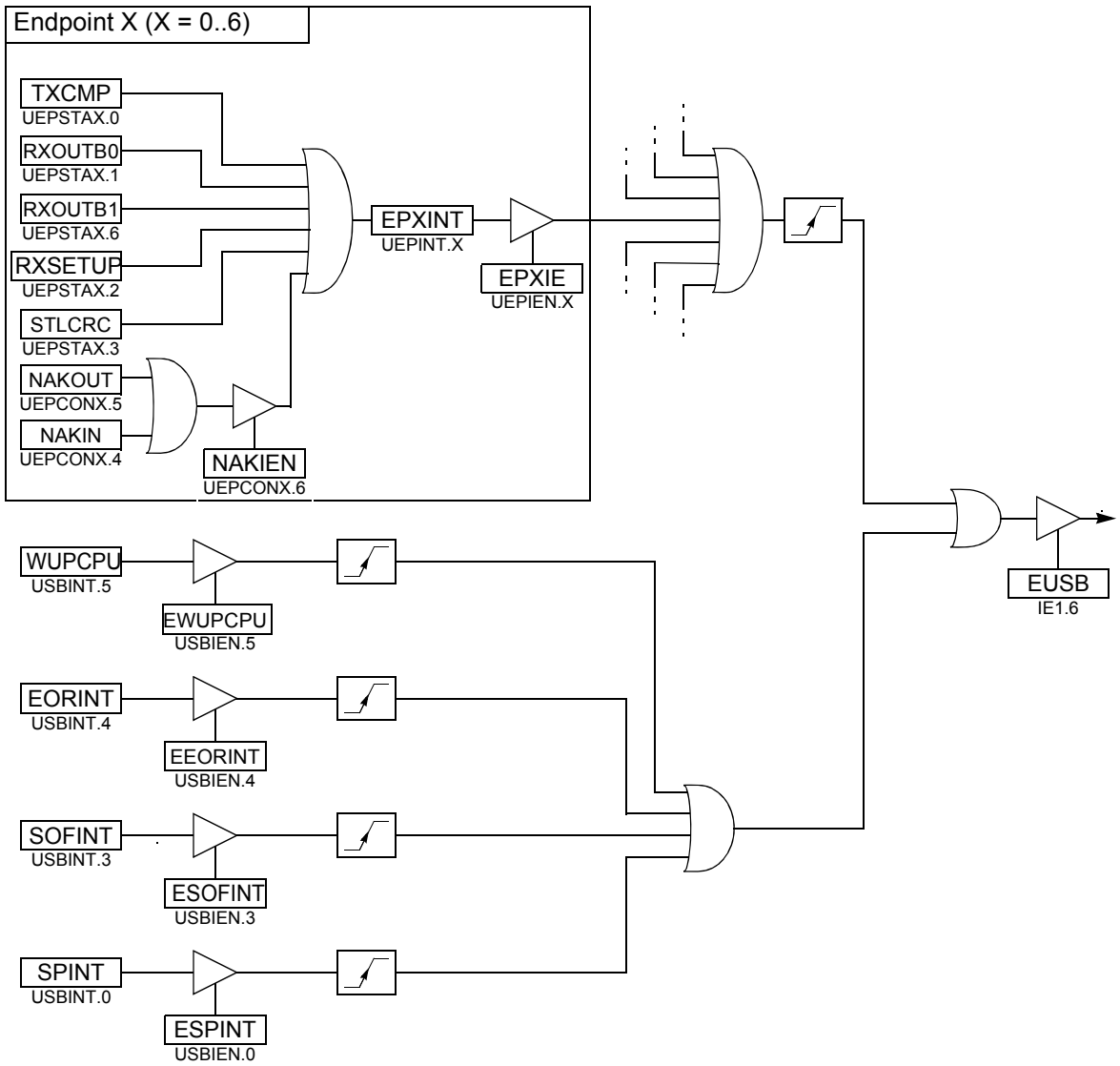
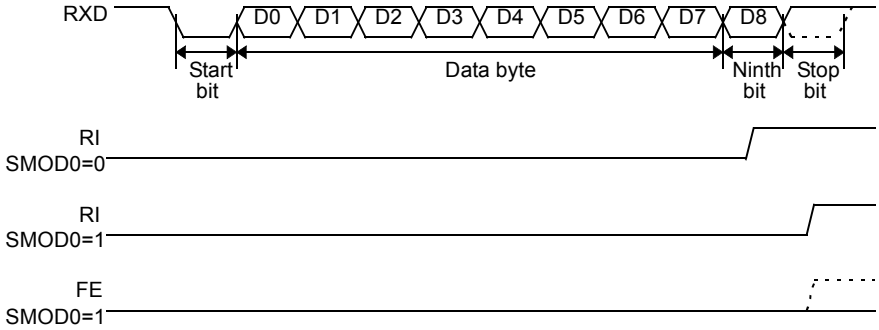


Figure 66. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.
To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't care bits (defined by zeros) to form the device's given address. The don't care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:SADDR1111 0001b
SADEN1111 1010b
Given1111 0X0Xb

Slave B:SADDR1111 0011b
SADEN1111 1001b
Given1111 0XX1b

Slave C:SADDR1111 0011b
SADEN1111 1101b
Given1111 00X1b

Table 78. Slave Address Mask Register for UART - SADEN (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 79. Slave Address Register for UART - SADDR (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 80. Serial Buffer Register for UART - SBUF (99h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb

Table 81. Baud Rate Reload Register for the internal baud rate generator, UART - BRL (9Ah)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 82. Baud Rate Control Register - BDRCON - (9Bh)

7	6	5	4	3	2	1	0
-	-	-	BRR	TBCK	RBCK	SPD	M0SRC

Bit Number	Bit Mnemonic	Description
7 - 5	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
4	BRR	**Baud Rate Run Control bit** Cleared to stop the internal Baud Rate Generator. Set to start the internal Baud Rate Generator.
3	TBCK	**Transmission Baud rate Generator Selection bit for UART** Cleared to select Timer 1 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
2	RBCK	**Reception Baud Rate Generator Selection bit for UART** Cleared to select Timer 1 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
1	SPD	**Baud Rate Speed Control bit for UART** Cleared to select the SLOW Baud Rate Generator. Set to select the FAST Baud Rate Generator.
0	M0SRC	**Baud Rate Source select bit in Mode 0 for UART** Cleared to select F_{CK_SI}/6 as the Baud Rate Generator. Set to select the internal Baud Rate Generator for UART in mode 0.

Reset Value = XXX0 0000b (Not bit addressable)

Table 99. Interrupt Enable Register 1 - IEN1 (B1h) for AT8xC5122

7	6	5	4	3	2	1	0
-	EUSB	-	-	ESCI	ESPI	-	EKB

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
6	EUSB	**USB Interrupt Enable bit** Cleared to disable USB interrupt . Set to enable USB interrupt.
5 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
3	ESCI	**SCI interrupt Enable bit** Cleared to disable SCIinterrupt . Set to enable SCI interrupt.
2	ESPI	**SPI interrupt Enable bit** Cleared to disable SPI interrupt . Set to enable SPI interrupt.
1	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
0	EKB	**Keyboard interrupt Enable bit** Cleared to disable keyboard interrupt . Set to enable keyboard interrupt.

Reset Value = X0XX 00X0b (Bit addressable)

Table 102. Interrupt Priority High Register 0 - IPH0 (B7h)

7	6	5	4	3	2	1	0
-	-	-	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7 - 5	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
4	PSH	**Serial port Priority High bit** PSH PSL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	External interrupt 0 Priority High bit PX0H PX0L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = X000 0000b (Not bit addressable)

Table 103. Interrupt Priority Low Register 1 - IPL1 (B2h) for AT8xC5122

7	6	5	4	3	2	1	0
-	PUSBL	-	-	PSCIL	PSPIL	-	PKBDL

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not change this bit.
6	PUSBL	**USB Interrupt Priority bit** Refer to PUSBH for priority level.
5 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
3	PSCIL	**SCI Interrupt Priority bit** Refer to PSPIH for priority level.
2	PSPIL	**SPI Interrupt Priority bit** Refer to PSPIH for priority level.
1	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
0	PKBL	**Keyboard Interrupt Priority bit** Refer to PKBDH for priority level.

Reset Value = X00X 00X0b (Bit addressable)

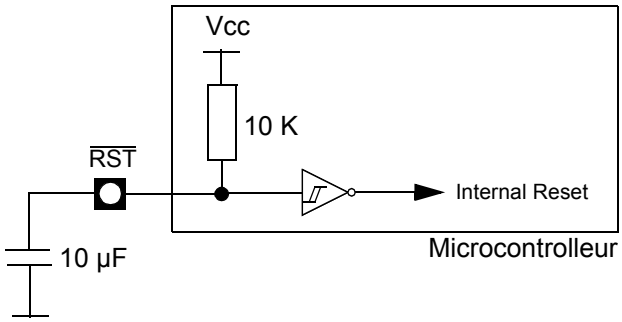
Reset pin

As explained in the POR section there is no need to use the reset pin as the internal reset function at power up is ensured by the POR. Anyway, if some applications requires a long reset, a reset controlled by the user or a reset controlled by external superviser device, the use of the reset pin is necessary.

Long Reset

As the pad integrates an internal pull-up of 10K, only an external capacitor of at least 10 µF is required to have an impact on the reset duration.

Figure 103. Long Reset



Reset Controlled by the User

The external capacitor is not needed if no long reset is required.

Figure 104. Reset Controlled by the User

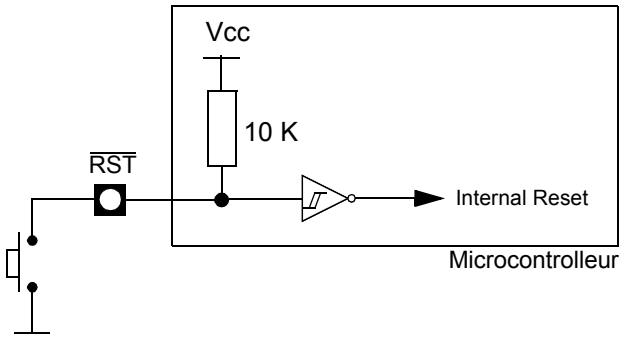


Table 111. Timeout value for F_{CK_WD} = 24 MHz / X2

S2	S1	S0	Timeout for F_{CK_WD}= 24 MHz / X2
0	0	0	4.10 ms
0	0	1	8.19 ms
0	1	0	16.38 ms
0	1	1	32.77 ms
1	0	0	65.54 ms
1	0	1	131.07 ms
1	1	0	262.14 ms
1	1	1	524.29 ms

Table 112. Watchdog Timer Enable register (Write Only) - WDTRST (A6h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = XXXX XXXXb

The WDTRST register is used to reset / enable the WDT by writing 1EH then E1H in sequence.

Power Management

Before activating the Idle Mode or Power Down Mode, the CPU clock must be switched to on-chip oscillator source if the PLL is used to fed the CPU clock.

Idle Mode

An instruction that sets PCON.0 indicates that it is the last instruction to be executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high level.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

Power Down Mode

To save maximum power, a power-down mode can be invoked by software (see Table 13, PCON register).

WARNING: To minimize power consumption, all peripherals and I/Os with static current consumption must be set in the proper state. I/Os programmed with low speed output configuration (KB_OUT) must be switch to push-pull or Standard C51 configuration before entering power-down. The CVCC generator must also be switch off.

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$, $\overline{INT1}$, Keyboard, Card insertion/removal and USB Interrupts are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input. When Keyboard Interrupt occurs after a power-down mode, 1024 clocks are necessary to exit to power-down mode and enter in operating mode.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 108. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power-down exit will be completed when the first input is released. In this case, the higher priority interrupt service routine is executed. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put AT83R5122, AT8xC5122/23 into power-down mode.

USB Interface

Figure 112. USB Interface

Symbol	Parameter	Min	Typ[5]	Max	Unit
V_{REF}	USB Reference Voltage	3.0		3.6	V
V_{IH}	Input High Voltage for D+ and D- (driven)	2.0		4.0	V
V_{IHZ}	Input High Voltage for D+ and D- (floating)	2.7		3.6	V
V_{IL}	Input Low Voltage for D+ and D-			0.8	V
V_{OH}	Output High Voltage for D+ and D-	2.8		3.6	V
V_{OL}	Output Low Voltage for D+ and D-	0.0		0.3	V

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