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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	SmartCard, SPI, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	46
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5122ds-rdtum

Table 2. Pin Description (Continued)

Port	VQFP64	VQFP32	PLCC68	PLCC28	QFN64	QFN32	Internal Power Supply	ESD	I/O	Reset Level	Alt	Reset Config	Conf 1	Conf 2	Conf 3	Led
P2.6	49	-	62	-	49	-	VCC	2KV	I/O	1	A14	Port51	Push-pull	KB_OUT	Input WPU	
P2.7	46	-	57	-	46	-	VCC	2KV	I/O	1	A15	Port51	Push-pull	KB_OUT	Input WPU	
P3.0	45	22	56	24	45	22	VCC	2KV	I/O	1	RxD	Port51	Push-pull	KB_OUT	Input WPU	
P3.1	48	24	59	25	48	24	VCC	2KV	I/O	1	TxD	Port51	Push-pull	KB_OUT	Input WPU	
P3.2	43	20	54	23	43	20	VCC	2KV	I/O	1	INT0	Port51				LED0
P3.3	41	19	52	22	41	19	VCC	2KV	I/O	1	INT1	Port51	Push-pull	KB_OUT	Input WPU	
P3.4	39	18	50	21	39	18	VCC	2KV	I/O	1	T0	Port51	Push-pull	KB_OUT	Input WPU	LED1
P3.5	44	21	55	-	44	21	VCC	2KV	I/O	1	T1	Port51				
P3.6	36	17	47	20	36	17	VCC	2KV	I/O	1	WR	Port51				LED2
P3.7	26	13	37	16	26	13	VCC	2KV	I/O	1	RD	Port51				LED3
P4.0	42	-	53	-	42	-	VCC	2KV	I/O	1	MISO	Port51				
P4.1	40	-	51	-	40	-	VCC	2KV	I/O	1	MOSI	Port51				
P4.2	38	-	49	-	38	-	VCC	2KV	I/O	1	SCK	Port51				
P4.3	37	-	48	-	37	-	VCC	2KV	I/O	1		Port51	Push-pull	KB_OUT	Input MPU	LED4
P4.4	35	-	46	-	35	-	VCC	2KV	I/O	1		Port51	Push-pull	KB_OUT	Input MPU	LED5
P4.5	33	-	44	-	33	-	VCC	2KV	I/O	1		Port51	Push-pull	KB_OUT	Input MPU	LED6
P5.0	14	7	23	-	14	7	VCC	2KV	I/O	1	KB0	Port51	Push-pull	Input MPU	Input WPU	
P5.1	13	-	22	-	13	-	VCC	2KV	I/O	1	KB1	Port51	Push-pull	Input MPU	Input WPU	
P5.2	11	-	20	-	11	-	VCC	2KV	I/O	1	KB2	Port51	Push-pull	Input MPU	Input WPU	
P5.3	10	-	19	-	10	-	VCC	2KV	I/O	1	KB3	Port51	Push-pull	Input WPD	Input WPU	
P5.4	8	-	17	-	8	-	VCC	2KV	I/O	1	KB4	Port51	Push-pull	Input WPD	Input WPU	

Table 6. Auxiliary Register 1 AUXR1- (0A2h) for AT8xC5122

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7 - 6	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
5	ENBOOT	**Enable Boot ROM (CRAM / E2PROM version only)** Set this bit to map the Boot ROM from 8000h to FFFFh. If the PC increments beyond 7FFFh address, the code is fetch from internal ROM Clear this bit to disable Boot ROM. If the PC increments beyond 7FFFh address, the code is fetch from external code memory (C51 standard roll over function) This bit is forced to 1 at reset
4	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
3	GF3	This bit is a general-purpose user flag.
2	0	Always cleared.
1	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
0	DPS	**Data Pointer Selection** Cleared to select DPTR0. Set to select DPTR1.

Reset Value = XX1X XX0X0b (Not bit addressable)

Table 7. Auxiliary Register 1 AUXR1- (0A2h) for AT83C5123

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7 - 6	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
5		**Reserved** The value read from this bit is indeterminate. Do not change these bits.
4	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
3	GF3	This bit is a general-purpose user flag.
2	0	Always cleared.
1	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
0	DPS	**Data Pointer Selection** Cleared to select DPTR0. Set to select DPTR1.

Reset Value = XXXX XX0X0b (Not bit addressable)

Table 8. CRAM Configuration Register - RCON (D1h)

7	6	5	4	3	2	1	0
-	-	-	-	RPS	-	-	-

Bit Number	Bit Mnemonic	Description
7 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
3	RPS	**CRAM Memory Mapping Bit** Set to map the CRAM memory during MOVX instructions Clear to map the XRAM memory during MOVX. This bit has priority over the EXTRAM bit.
2-0	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.

Reset Value = XXXX 0XXXb

AT8xC5122's CRAM and E2PROM Versions

The AT8xC5122's CRAM and E2PROM versions implements :

- 32 KB of ROM mapped from 8000 to FFFF in which is embedded a bootloader for In-System Programming feature

- 32 KB of CRAM (Code RAM) , a volatile program memory mapped from 0000 to 7FFF

In CRAM versions only :

- 512 bytes of E2PROM can be optionally implemented to store permanent data

In E2PROM version :

- 32KB of E2PROM are implemented to store permanent code

Warnings :

– some bytes of user program memory space are reserved for bootloader configuration. Depending on the configuration, up to 256 bytes of code may be not available for the user code from 7F00h location. Refer to bootloader datasheet for further details.

– Port P3.7 may be used by the bootloader as a hardware condition at reset to select the In-System Programming mode. Once the bootloader has started, the P3.7 Port is no more used.

Table 17. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IPH0	B7h	Interrupt Priority Control High 0				PSH	PT1H	PX1H	PT0H	PX0H
IPL1	B2h	Interrupt Priority Control Low 1		PUSBL			PSCIL	PSPIL(1)		PKBL(1)
IPH1	B3h	Interrupt Priority Control High 1		PUSBH			PSCIH	PSPIH(1)		PKBH(1)
ISEL	A1h	Interrupt Enable Register	CPLEV		PRESIT	RXIT	OELEV	OEEN	PRESEN	RXEN

Note: 1. Only for AT8xC5122

Table 18. SCIB SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCGT0	B4h	Smart Card Transmit Guard Time Register 0	GT7 - 0							
SCGT1	B5h	Smart Card Transmit Guard Time Register 1								GT8
SCWT0	B4h	Smart Card Character/ Block Waiting Time Register 0	WT7 - 0							
SCWT1	B5h	Smart Card Character/ Block Waiting Time Register 1	WT15-8							
SCWT2	B6h	Smart Card Character/ Block Waiting Time Register 2	WT23-16							
SCWT3	C1h	Smart Card Character/ Block Waiting Time Register 3	WT31-24							
SCICR	B6h	Smart Card Interface Control Register	RESET	CARDDET	VCARD1-0		UART	WTEN	CREP	CONV
SCCON	ACh	Smart Card Interface Contacts Register	CLK		CARDC8	CARDC4	CARDIO	CARDCLK	CARDRST	CARDVCC
SCETU0	ACh	Smart Card ETU Register 0	ETU7 - 0							
SCETU1	ADh	Smart Card ETU Register 1	COMP					ETU10-8		
SCISR	ADh	Smart Card UART Interface Status Register (Read only)	SCTBE	CARDIN	ICARDOVF	VCARDOK	SCWTO	SCTC	SCRC	SCPE
SCIIR	AEh	Smart Card UART Interrupt Identification Register (Read only)	SCTBI		ICARDERR	VCARDERR	SCWTI	SCTI	SCRI	SCPI
SCIER	AEh	Smart Card UART Interrupt Enable Register	ESCTBI		ICARDER	EVCARDER	ESCWTI	ESCTI	ESCRI	ESCPI
SCSR	ABh	Smart Card Selection Register		BGTEN		CREPSEL	ALTKPS1-0		SCCLK1	SCRS
SCIBUF	AAh	Smart Card Buffer Register	Can store a new byte to be transmitted on the I/O pin when SCTBE is set. Bit ordering on the I/O pin depends on the convention Provides the byte received from the I/O pin when SCRI is set. Bit ordering on the I/O pin depends on the convention.							

Table 26. Clock Configuration Register 0 - CKCON0 (S:8Fh)

7	6	5	4	3	2	1	0
-	WDX2	-	SIX2	-	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	WDX2	**Watchdog clock** This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect. Cleared to bypass the 1/2 prescaler. Set to select the 1/2 output for this peripheral.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	SIX2	**Enhanced UART clock (Mode 0 and 2)** This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect. Cleared to bypass the 1/2 prescaler. Set to select the 1/2 output for this peripheral.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	T1X2	**Timer 1 clock** This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect. Cleared to bypass the 1/2 prescaler. Set to select the 1/2 output for this peripheral.
1	T0X2	**Timer 0 clock** This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect. Cleared to bypass the 1/2 prescaler. Set to select the 1/2 output for this peripheral.
0	X2	**System clock Control bit** Cleared to select the PRT output for CPU and all the peripherals . Set to bypass the PRT prescaler and to enable the individual peripherals ‘X2’ bits.

Reset Value = X0X0 X000b

IEC7816-3 says this procedure is mandatory in ATR for card supporting T=0 while EMV says this procedure is mandatory for T=0 but does not apply for ATR.

Functional Description

The architecture of the Smart Card Interface Block can be detailed as follows:

Barrel Shifter

The Barrel Shifter performs the translation between 1 bit serial data and 8 bits parallel data

The barrel function is useful for character repetition since the character is still present in the shifter at the end of the character transmission.

This shifter is able to shift the data in both directions and to invert the input or output value in order to manage both direct and inverse ISO7816-3 convention.

Coupled with the barrel shifter is a parity checker and generator.

There are 2 registers connected to this barrel shifter, one for the transmission and one for the reception. They act as buffers to relieve the CPU of timing constraints.

SCART FSM

(Smart Card Asynchronous Receiver Transmitter Finite State Machine)

This is the core of the block. Its purpose is to control the barrel shifter. To sequence correctly the barrel shifter for a reception or a transmission, it uses the signals issued by the different counters. One of the most important counters is the guard time counter that gives time slots corresponding to the character frame.

The SCART FSM is enabled only in UART mode.

The transition from the receipt mode to the transmit mode is done automatically. Priority is given to the transmission. Transmission refers to Terminal transmission to the ICC. Reception refers to reception by the Terminal from the ICC.

ETU Counter

The ETU (Elementary Timing Unit) counter controls the working frequency of the barrel shifter, in fact it generates the enable signal of the barrel shifter. It receives the Card Clock, and generates the ETU clock. The Card Clock frequency is called “f” below. The ETU counter is 11 bit wide.

A special compensation mode can be activated. It accomodates situations where the ETU is not an integer number of Card Clock (CK_ISO). The compensation mode is controlled by the COMP bit in SCETU1 register bit position 7. With COMP=1 the ETU of every character even bits is reduced by 1 Card Clock period. As a result, the average ETU is : ETU_average = (ETU - 0.5). One should bear in mind that the ETU counter should be programmed to deliver a faster ETU which will be reduced by the COMP mechanism, not the other way around. This allows to reach the required precision of the character duration specified by the ISO7816-3 standard.

Example1 : F=372, D=32 => ETU= F/D = 11.625 clock cycles.

We select ETU[10-0] = 12 , COMP=1. ETUaverage= 12 - (0.5*COMP) = 11.5

The result will be a full character duration (10 bit) = (10 - 0.107)*ETU. The EMV specification is (10 +/- 0.2)*ETU

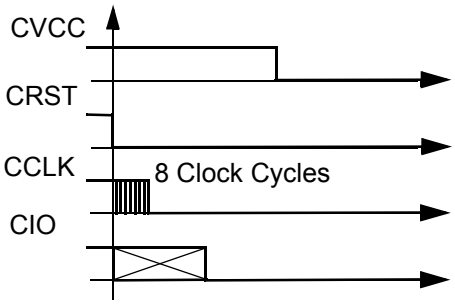
Guard Time Counter

The minimum time between the leading edge of the start bit of 2 consecutive characters transmitted by the Terminal is controlled by the Guard Time counter, as described in Figure 32.

Removal of the smart card will automatically start the power off sequence as described in Figure 38.

The SCIB deactivation sequence after a reset of the CPU or after a lost of power supply is ISO7816-3 compliant. The switching order of the signals is the same as in Figure 38 but the delay between signals is analog and not clock dependant.

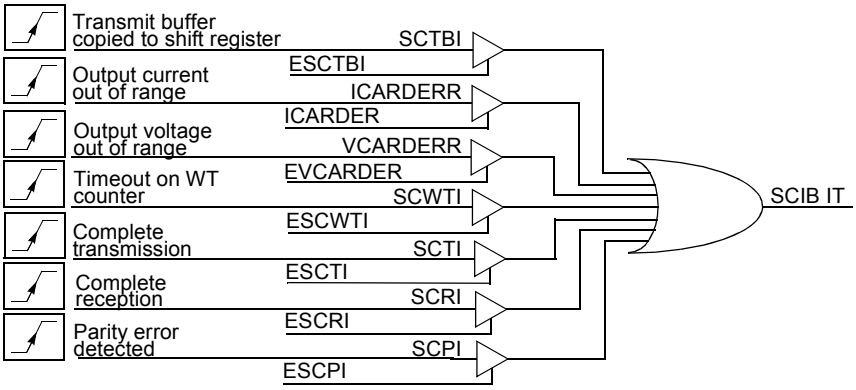
Figure 38. SCIB Deactivation Sequence after a Card Extraction



Interrupt Generator

There are several sources of interruption but the SCIB macro-cell issues only one interrupt signal: SCIBIT.

Figure 39. SCIB Interrupt Sources



This signal is high level active. Each of the sources is able to activate the SCIB interruption which is cleared when the Smart Card Interrupt register is read by the microcontroller.

If during the read of the Smart Card Interrupt register another interrupt occurs, the activation of the corresponding bit in the Smart Card Interrupt register and the new SCIB interruption is delayed until the interrupt register is read by the microcontroller.

Warning : Each bit of the SCIIR register is irrelevant while the corresponding interruption is disabled in SCIER register. When the interruption mode is not used, the bits of the SCISR register must be used instead of the bits of the SCIIR register.

Table 44. Smart Card Interface Control Register - SCICR (S:B6h, SCRS = 1)

7	6	5	4	3	2	1	0
RESET	CARDDET	VCARD1	VCARD0	UART	WTEN	CREP	CONV

Bit Number	Bit Mnemonic	Description
7	RESET	**Reset** Set this bit to reset and deactivate the Smart Card Interface. Clear this bit to activate the Smart Card Interface. This bit acts as an active high software reset.
6	CARDDET	**Card Presence Detector Sense** Clear this bit to indicate the card presence detector is open when no card is inserted (CPRES is high). Set this bit to indicate the card presence detector is closed when no card is inserted (CPRES is low).
5-4	VCARD[1:0]	**Card Voltage Selection:** VCARD[1] VCARD[0] CVCC 0 0 0 V 0 1 1.8 V 1 0 3.0 V 1 1 5.0 V
3	UART	**Card UART Selection** Clear this bit to use the CARDIO bit (P1.0) bit to drive the Card I/O (P1.0) pin. Set this bit to use the Smart Card UART to drive the Card I/O pin (P1.0 pin). Controls also the Waiting Time Counter as described in Section “Waiting Time (WT) Counter”, page 67
2	WTEN	**Waiting Time Counter Enable** Clear this bit to stop the counter and enable the load of the Waiting Time counter hold registers. The hold registers are loaded with SCWT0, SCWT1, SCWT2 and SCWT3 values when SCWT2 is written. Set this bit to start the Waiting Time Counter. The counters stop when it reaches the timeout value. If the UART bit is set, the Waiting Time Counter automatically reloads with the hold registers whenever a start bit is sent or received.
1	CREP	**Character Repetition** Clear this bit to disable parity error detection and indication on the Card I/O pin in receive mode and to disable character repetition in transmit mode. Set this bit to enable parity error indication on the Card I/O pin in receive mode and to set automatic character repetition when a parity error is indicated in transmit mode. Depending upon CREPSET bit is SCSR register, the receiver can indicate parity error up to 4times (3 repetitions) or up to 5times (4 repetitions) after which it will raise the parity error bit SCPE bit in the SCISR register. If parity interrupt is enabled, the SCPI bit in SCIIR register will be set too. Alternately, the transmitter will detect ICC character repetition request. After 3 or 4 unsuccessful repetitions (depending on CREPSEL bit in SCSR register), the transmitter will raise the parity error bit SCPE bit in the SCISR register. If parity interrupt is enabled, the SCPI bit in SCIIR register will be set too. **Note** : Character repetition mode is specified for T=0 protocol only and should not be used in T=1 protocol (block oriented protocol)
0	CONV	**ISO Convention** Clear this bit to use the direct convention: b0 bit (LSB) is sent first, the parity bit is added after b7 bit and a low level on the Card I/O pin represents a’0’. Set this bit to use the inverse convention: b7 bit (LSB) is sent first, the parity bit is added after b0 bit and a low level on the Card I/O pin represents a’1’.

Reset Value = 0000 0000b

Table 46. Smart Card UART Interface Status Register - SCISR (S:ADh, SCRS=0)

7	6	5	4	3	2	1	0
SCTBE	CARDIN	ICARDOVF	VCARDOK	SCWTO	SCTC	SCRC	SCPE

Bit Number	Bit Mnemonic	Description
7	SCTBE	**UART Transmit Buffer Empty Status** This bit is set by hardware when the Transmit Buffer is copied to the transmit shift register of the Smart Card UART. It is cleared by hardware when SCIBUF register is written.
6	CARDIN	**Card Presence Status** This bit is set by hardware if there is a card presence (debouncing filter has to be done by software). This bit is cleared by hardware if there is no card presence.
5	ICARDOVF	**Card Current Overflow Status** This bit is set when the current on card is above the limit specified by bit OVFADJ in DCCKPS register (Table 61 on page 92) It is cleared by hardware.
4	VCARDOK	**Card Voltage Correct Status** This bit is set when the output voltage is within the voltage range specified by VCARD[1:0] in SCICR register. It is cleared otherwise.
3	SCWTO	**Waiting Time Counter Timeout Status** This bit is set by hardware when the Waiting Time Counter has expired. It is cleared by the reload of the counter or by the reset of the SCIB.
2	SCTC	**UART Transmitted Character Status** This bit is set by hardware when the Smart Card UART has transmitted a character. If character repetition mode is selected, this bit will be set only after a successful transmission. If the last allowed repetition in not successful, this bit will not be set. It is cleared by software when this register is read.
1	SCRC	**UART Received Character Status** This bit is set by hardware when the Smart Card UART has received a character It is cleared by hardware when SCIBUF register is read. If character repetition mode is selected, this bit will be set only after a successful reception. If the last allowed repetition is still unsuccessful, this bit will be set to let the user read the erroneous value if necessary.
0	SCPE	**Character Reception Parity Error Status** This bit is set when a parity error is detected on the received character. It is cleared by software when this register is read. If character repetition mode is selected, this bit will be set only if the ICC report an error on the last allowed repetition of a TERMINAL transmission, or if a reception parity error is found on the last allowed ICC character repetition.

Reset Value = 1000 0000b

Table 59. Smart Card Clock Reload Register - SCICLK (S:C1h, SCRS=1)

7	6	5	4	3	2	1	0
XTSCS	-	SCICLK5	SCICLK4	SCICLK3	SCICLK2	SCICLK1	SCICLK0

Bit Number	Bit Mnemonic	Description
7	XTSCS	**Smart Card Clock Selection Bit** If XTSCS bit is set OR EXT48 bit is set (in PLLCON register) , CK_PLL is used to generate CK_ISO. Otherwise, CK_XTAL1 is used to generate CK_ISO. See the Clock Tree diagram figure 17.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
5 - 0	SCICLK[5:0]	**SCIB clock reload register** Prescaler 2 reload value is used to defines the card clock frequency. If SCICLK[5:0] is smaller than 48 : Fck_iso = Fck_pll or Fck_XTAL1/ (2 * (48 - SCICLK[5:0])) If SCICLK[5:0] is equal to 48 : Fck_iso = Fck_XTAL1 SCICLK[5:0] must be smaller than 49.

Reset Value = 0X10 1111b *(default value for a divider by two)*

DC/DC Converter

The Smart Card voltage (CVCC) is supplied by the integrated DC/DC converter which is controlled by several registers:

- The SCICR register (Table 44 on page 77) controls the CVCC level by means of bits VCARD[1:0].
- The SCCON register (Table 45 on page 78) enables to switch the DC/DC converter on or off by means of bit CARDVCC.
- The DCCKPS register (Table 61 on page 92) controls the DC/DC clock and current.

The DC/DC converter cannot be switched on while the CPRES pin remains inactive. If CPRES pin becomes inactive while the DC/DC converter is operating an automatic shut down sequence of the DC/DC converter is initiated by the electronics.

It is mandatory to switch off the DC/DC Converter before entering in Power-down mode.

Configuration

The DC/DC Converter can work in two different modes which are selected by bit MODE in DCCKPS register:

- Pump Mode: an external inductance of 10 µH must be connected between pins LI and VCC. VCC can be higher or lower than CVCC.
- Regulator mode : no external inductance is required but VCC must be always higher than CVCC+0.3V. The Regulation mode will work even if an external inductance of 10 µH is connected between pins LI and VCC

The DC/DC clock prescaler which is controlled by bits DCCKPS[3:0], in DCCKPS register must be configured to set the DC/DC clock to a working frequency of 4 MHz which depends upon the value of the crystal. There is no need to change the default configuration set by the reset sequence if an 8 MHz crystal is used by the application.

The DC/DC Converter implements a current overflow controller which avoids permanent damage of the DC/DC converter in case of short circuit between CVCC and CVSS. The maximum limit is around 100 mA. It is possible to increase this limit in normal operating

Miscellaneous

USB Reset

The EORINT bit in the USBINT register is set by hardware when a End of Reset has been detected on the USB bus. This triggers a USB interrupt if enabled. The USB controller is still enabled, but all the USB registers are reset by hardware. The firmware should clear the EORINT bit to allow the next USB reset detection.

STALL Handshake

This function is only available for Control, Bulk, and Interrupt endpoints.

The firmware has to set the STALLRQ bit in the UEPSTAX register to send a STALL handshake at the next request of the Host on the endpoint selected with the UEPNUM register. The RXSETUP, TXRDY, TXCMPL, RXOUTB0 and RXOUTB1 bits must be first reset to 0. The bit STLCRC is set at 1 by the USB controller when a STALL has been sent. This triggers an interrupt if enabled.

The firmware should clear the STALLRQ and STLCRC bits after each STALL sent.
The STALLRQ bit is cleared automatically by hardware when a valid SETUP PID is received on a CONTROL type endpoint.

Start of Frame Detection

The SOFINT bit in the USBINT register is set when the USB controller detects a Start Of Frame PID. This triggers an interrupt if enabled. The firmware should clear the SOFINT bit to allow the next Start of Frame detection.

Frame Number

When receiving a Start of Frame, the frame number is automatically stored in the UFNUML and UFNUMH registers. The CRCOK and CRCERR bits indicate if the CRC of the last Start Of Frame is valid (CRCOK set at 1) or corrupt (CRCERR set at 1). The UFNUML and UFNUMH registers are automatically updated when receiving a new Start of Frame.

Data Toggle Bit

The Data Toggle bit is set by hardware when a DATA 0 packet is received and accepted by the USB controller and cleared by hardware when a DATA 1 packet is received and accepted by the USB controller. This bit is reset when the firmware resets the endpoint FIFO using the UEPRST register.

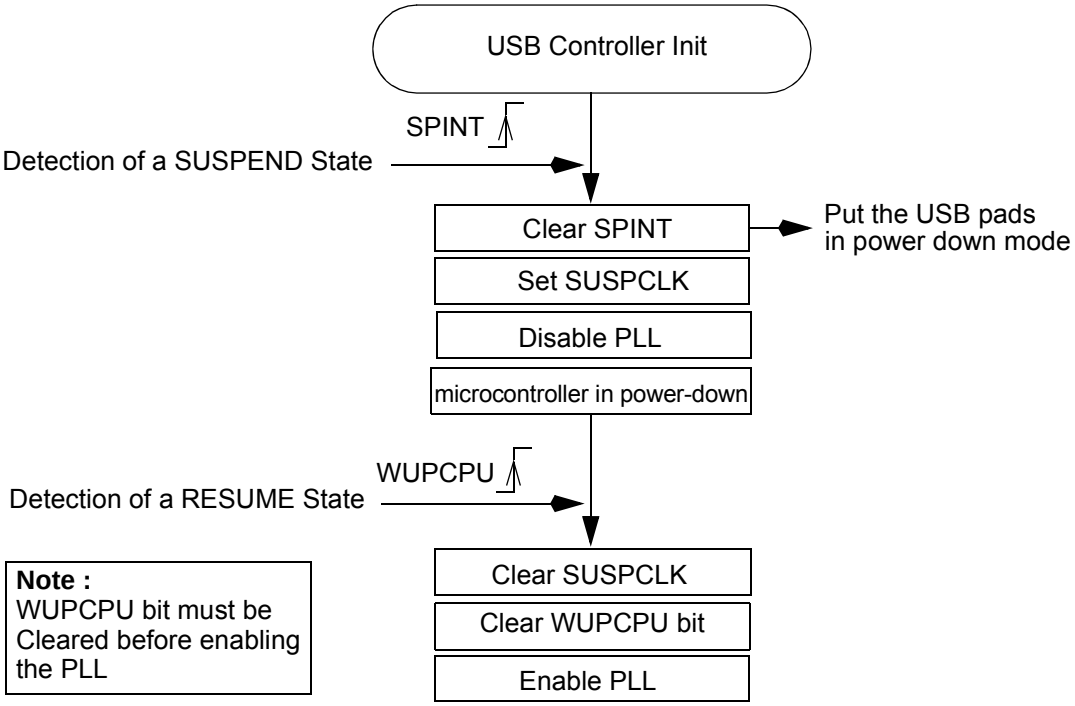
For Control endpoints, each SETUP transaction starts with a DATA 0 and data toggling is then used as for Bulk endpoints until the end of the Data stage (for a control write transfer). The Status stage completes the data transfer with a DATA 1 (for a control read transfer).

For Isochronous endpoints, the device firmware should ignore the data-toggle.

NAK Handshakes

When a NAK handshake is sent by the USB controller to a IN or OUT request from the Host, the NAKIN or NAKOUT bit is set by hardware. This information can be used to determine the direction of the communication during a Control transfer.
These bits are cleared by software.

Figure 58. Example of a Suspend/Resume Management



Warning: The core must be switched in external clock mode before disabling the PLL.

Upstream Resume

A USB device can be allowed by the Host to send an upstream resume for Remote Wake-up purpose.

When the USB controller receives the SET_FEATURE request: DEVICE_REMOTE_WAKEUP, the firmware should set to 1 the RMWUPE bit in the USBCON register to enable this function. RMWUPE value should be 0 in the other cases.

If the device is in SUSPEND mode, the USB controller can send an upstream resume by clearing first the SPINT bit in the USBINT register and by setting then to 1 the SDRMWUP bit in the USBCON register. The USB controller sets to 1 the UPRSM bit in the USBCON register. All clocks must be enabled first. The Remote Wake is sent only if the USB bus was in Suspend state for at least 5 ms. When the upstream resume is completed, the UPRSM bit is reset to 0 by hardware. The firmware should then clear the SDRMWUP bit.

Serial I/O Port

The serial I/O port in the AT83R5122, AT8xC5122/23 is compatible with the serial I/O port in the 80C52.

The I/O port provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

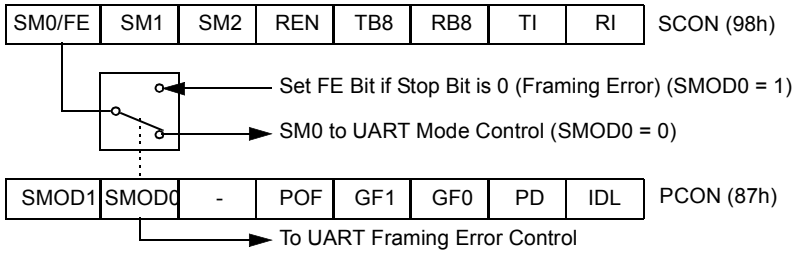
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (Modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 64).

Figure 64. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Figure 69 on page 128) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 65 and Figure 66).

Figure 65. UART Timings in Mode 1

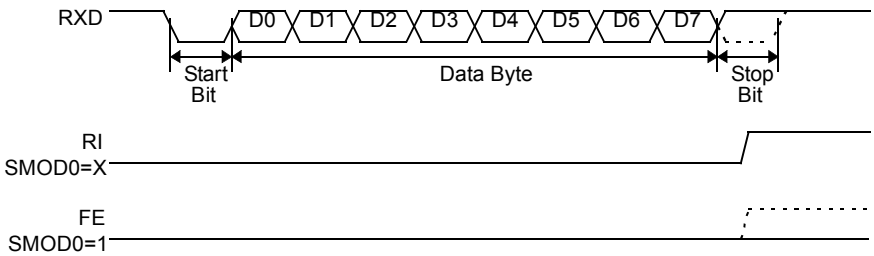


Figure 85. Data Transmission Format (CPHA = 0)

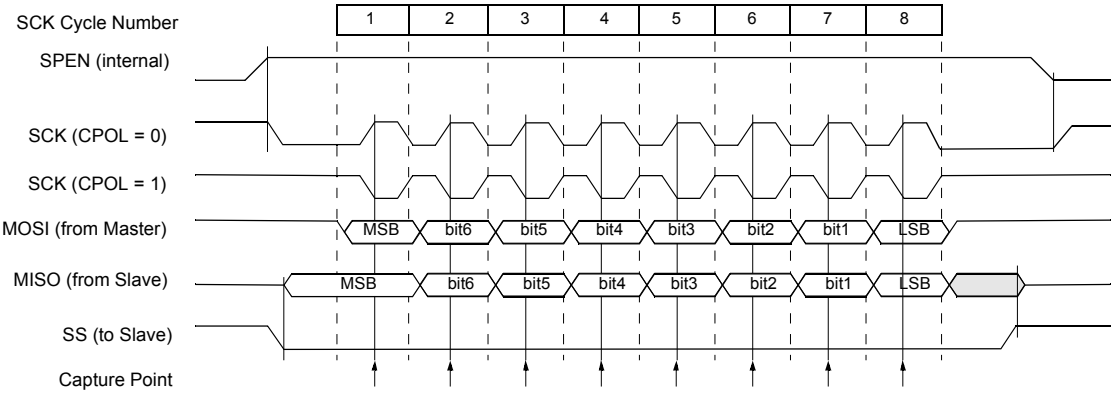
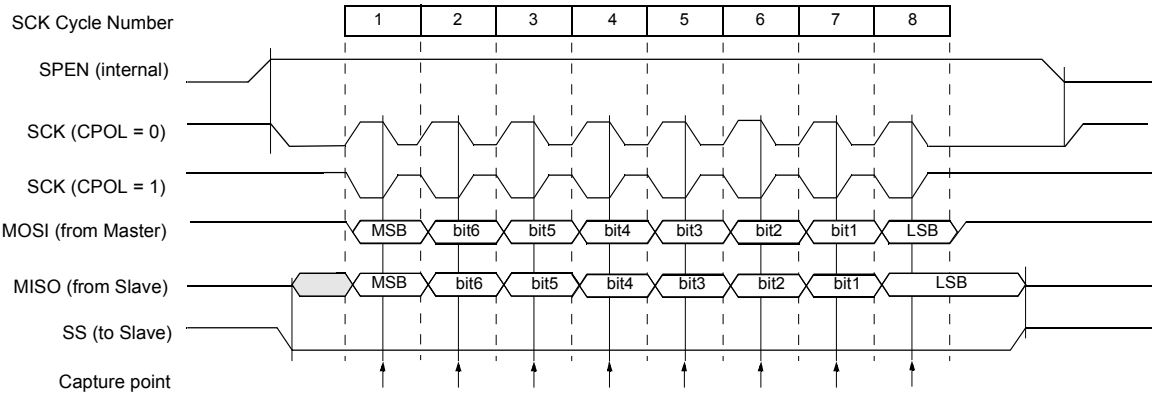


Figure 86. Data Transmission Format (CPHA = 1)



As shown in Figure 85, the first SCK edge is the MSB capture strobe. Therefore the Slave must begin driving its data before the first SCK edge, and a falling edge on the $\overline{SS}$ pin is used to start the transmission. The $\overline{SS}$ pin must be toggled high and then low between each byte transmitted (Figure 87).

Figure 87. CPHA/$\overline{SS}$ Timing

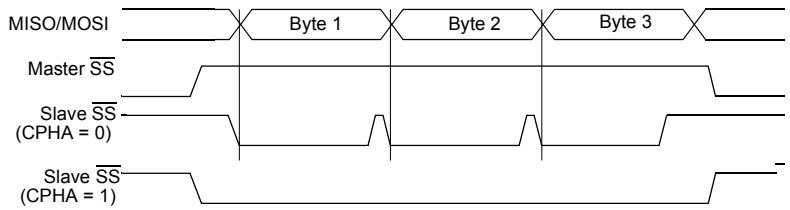


Figure 86 shows an SPI transmission in which CPHA is “1”. In this case, the Master begins driving its MOSI pin on the first SCK edge. Therefore, the Slave uses the first SCK edge as a start transmission signal. The $\overline{SS}$ pin can remain low between transmis-

For normal Timer operation (GATE0= 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE0 and TR0 allows external pin INT0# to control Timer operation.

Timer 0 overflow (count rolls over from all 1s to all 0s) sets the TF0 flag and generates an interrupt request.

It is important to stop the Timer/Counter before changing modes.

Mode 0 (13-bit Timer)

Mode 0 configures Timer 0 as a 13-bit Timer which is set up as an 8-bit Timer (TH0 register) with a modulo-32 prescaler implemented with the lower five bits of the TL0 register (see Figure 89). The upper three bits of the TL0 register are indeterminate and should be ignored. Prescaler overflow increments the TH0 register.

Figure 90 gives the overflow period calculation formula.

Figure 89. Timer/Counter x (x= 0 or 1) in Mode 0

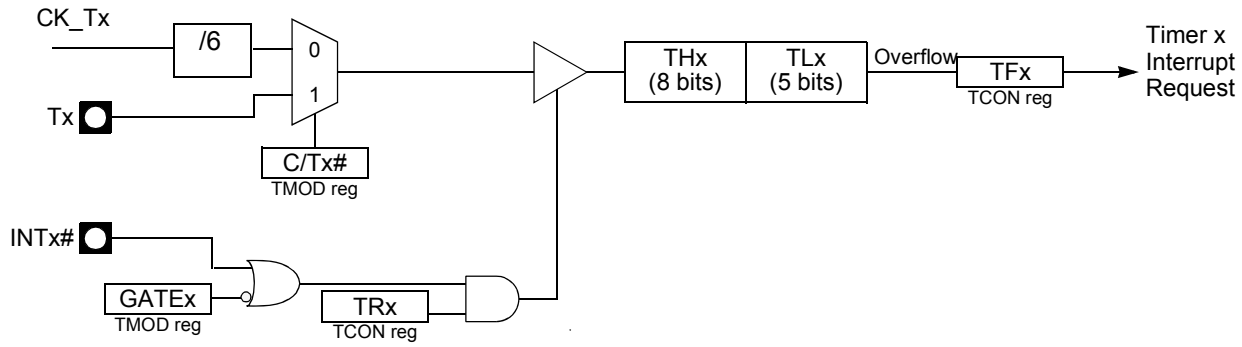


Figure 90. Mode 0 Overflow Period Formula

$$TFx_{PER} = \frac{6 \cdot (16384 - (THx, TLx))}{F_{CK\_Tx}}$$

Mode 1 (16-bit Timer)

Mode 1 configures Timer 0 as a 16-bit Timer with the TH0 and TL0 registers connected in a cascade (see Figure 91). The selected input increments the TL0 register.

Figure 92 gives the overflow period calculation formula when in timer mode.

Interrupt Sources and Vectors

Table 108. Interrupt Vectors

Interrupt Source	Polling Priority at Same Level	Vector Address
Reset	0 (Highest Priority)	C:0000h
INT0	1	C:0003h
Timer 0	2	C:000Bh
INT1	3	C:0013h
Timer 1	4	C:001Bh
UART	6	C:0023h
Reserved	7	C:002Bh
Reserved	5	C:0033h
Keyboard Controller (1)	8	C:003Bh
Reserved	9	C:0043h
SPI Controller (1)	10	C:004Bh
Smart Card Controller	11	C:0053h
Reserved	12	C:005Bh
Reserved	13	C:0063h
USB Controller	14	C:006Bh
Reserved	15 (Lowest Priority)	C:0073h

Note: 1. Only fot AT8xC5122

Figure 101. Static behaviour of POR and PFD

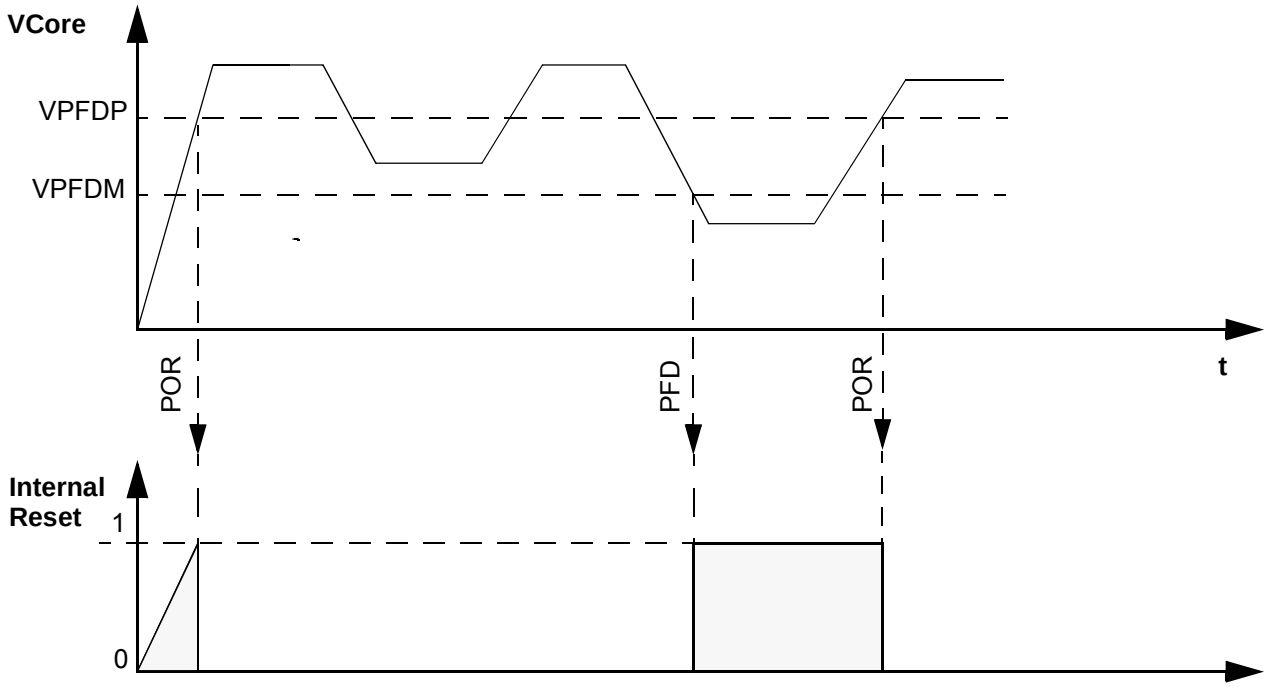
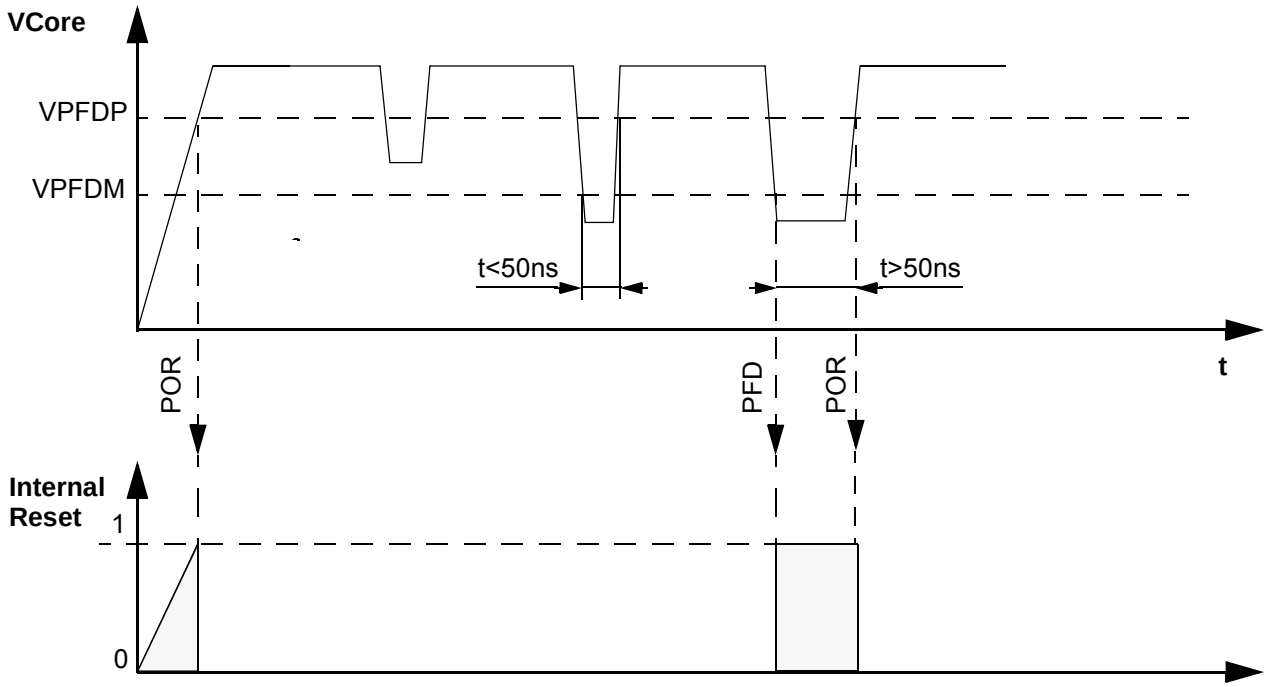


Figure 102. Dynamic behaviour of POR and PFD



Reset Controlled by an External Superviser Device

As the reset pin can be forced in output by the Watch-Dog timer (WDT) or the POR/PFD features, there can be a conflict between the external superviser device and the microcontroller's reset pin when in one side the external superviser is pulling the reset pin to VCC and in another side the WDT or POR/PFD features tries to force the reset pin to ground. Therefore, it recommended to insert a series resistor of 1.8K +/-10% or a diode (1N4148 for instance) between the external superviser device and the reset pin as detailed in the following figures.

Figure 105. Use of an External Serial Resistor

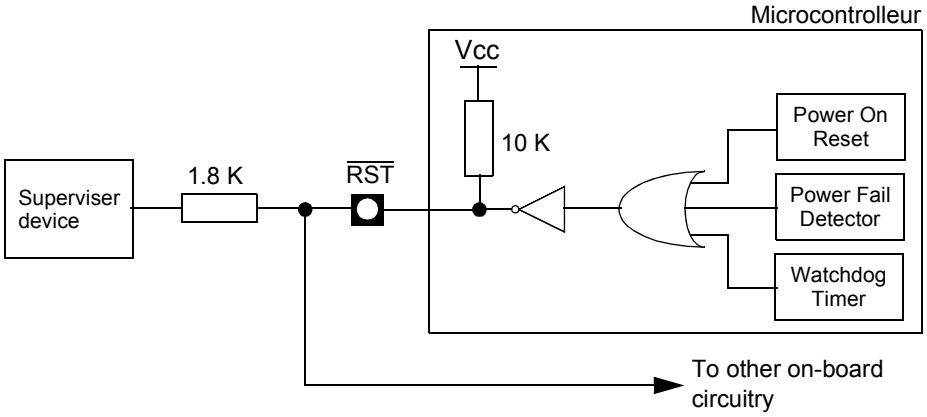
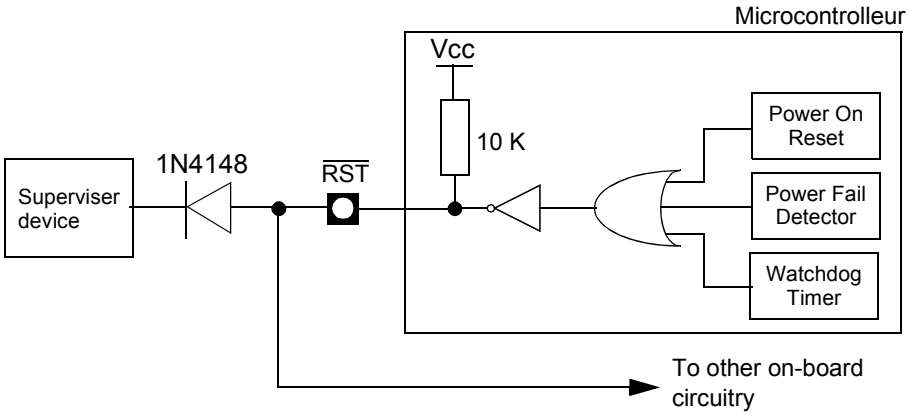
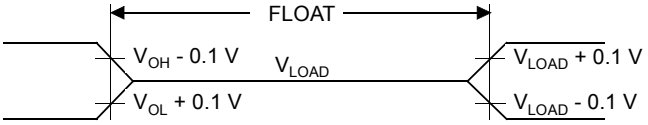


Figure 106. Use of an External Diode



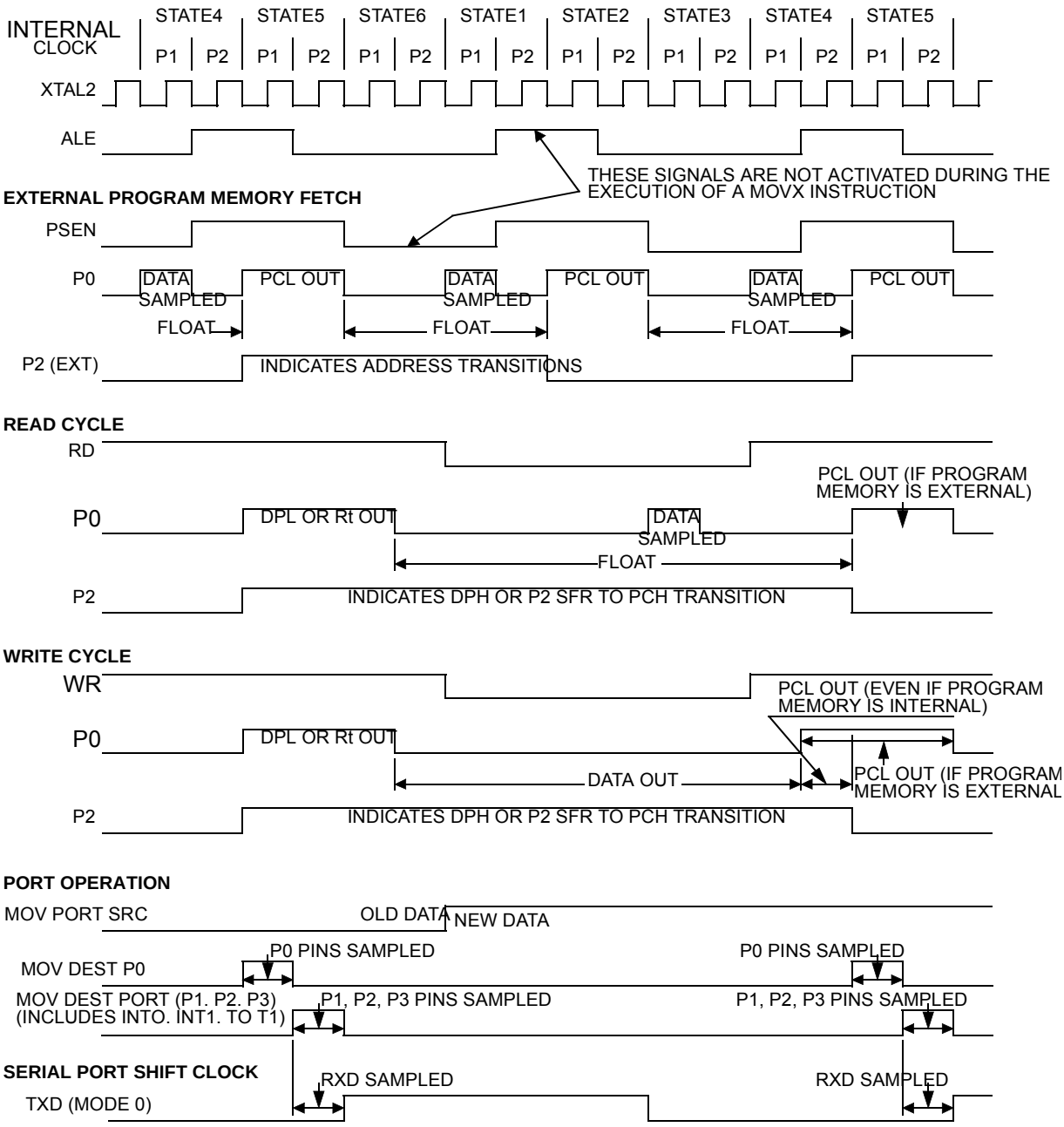
Float Waveforms



For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 must be changed to XTAL2/2.



Datasheet Revision History

Changes from 4202A to 4202B

1. Product AT8xEC5122 added.
2. Products AT83C5123 and AT83EC5123 added.

Changes from 4202B to 4202C

1. All sections updated.
2. QFN64 and QFN32 packages added.
3. SCIB section : VCC must be higher than 4.0V when DC/DC is operated at 5V.

Changes from 4202C to 4202D

1. Product AT89C5122DS added (EA pin changed to VCC)
2. Typical applications section: external pull-up shown on CIO pin
3. Ports section : Detailed explanations on CIO, CC4, CC8 quasi-bidirectional ports
4. Ordering information section: AT89C5122DS part-numbers added

Changes from 4202D to 4202E

1. Changed input voltage frequency from 3.6V to 3.0V throughout the document.
2. Update of DC parameters of smart card interface to be EMV 4.1 compliant.

Changes from 4202E to 4202F

1. Product AT83EC5122 and AT83EC5123 removed.
2. Product AT83R5122 added.
3. Package PLCC28 not supported anymore.
4. Global update.