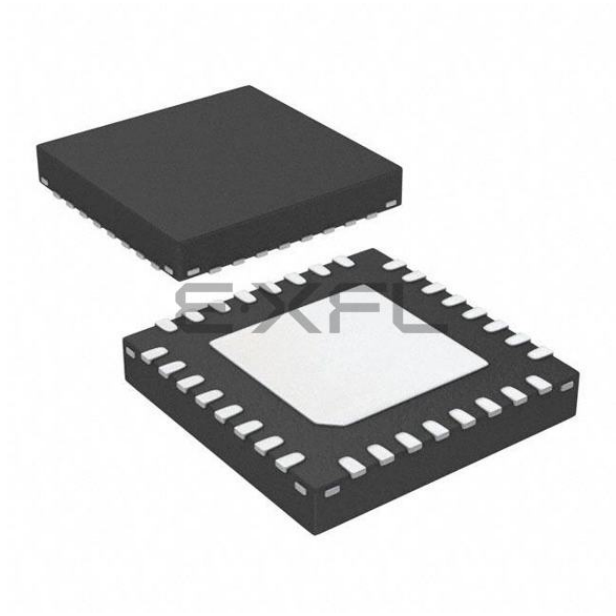

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x14b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb11f16e-b-qfn32

Low Pin Count Package Description

AT83C5123 version

Figure 6. VQFP32 Package Pinout

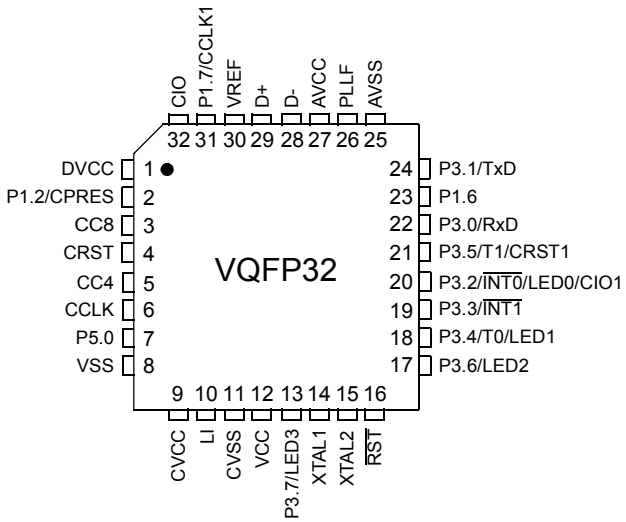
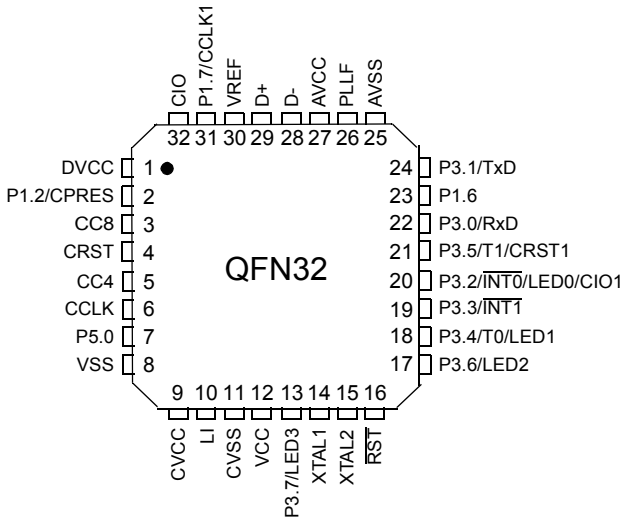
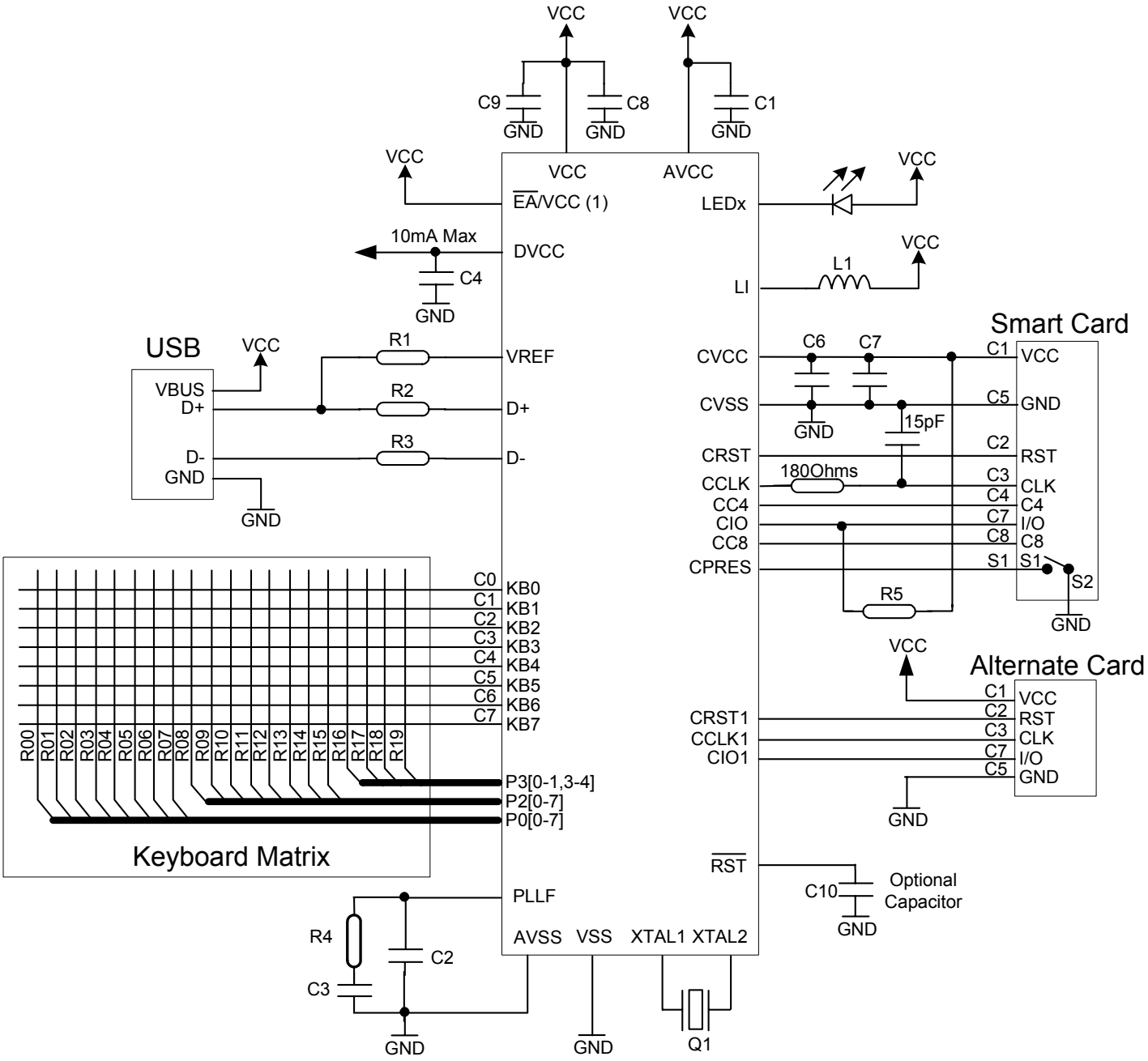


Figure 7. QFN32 Package Pinout

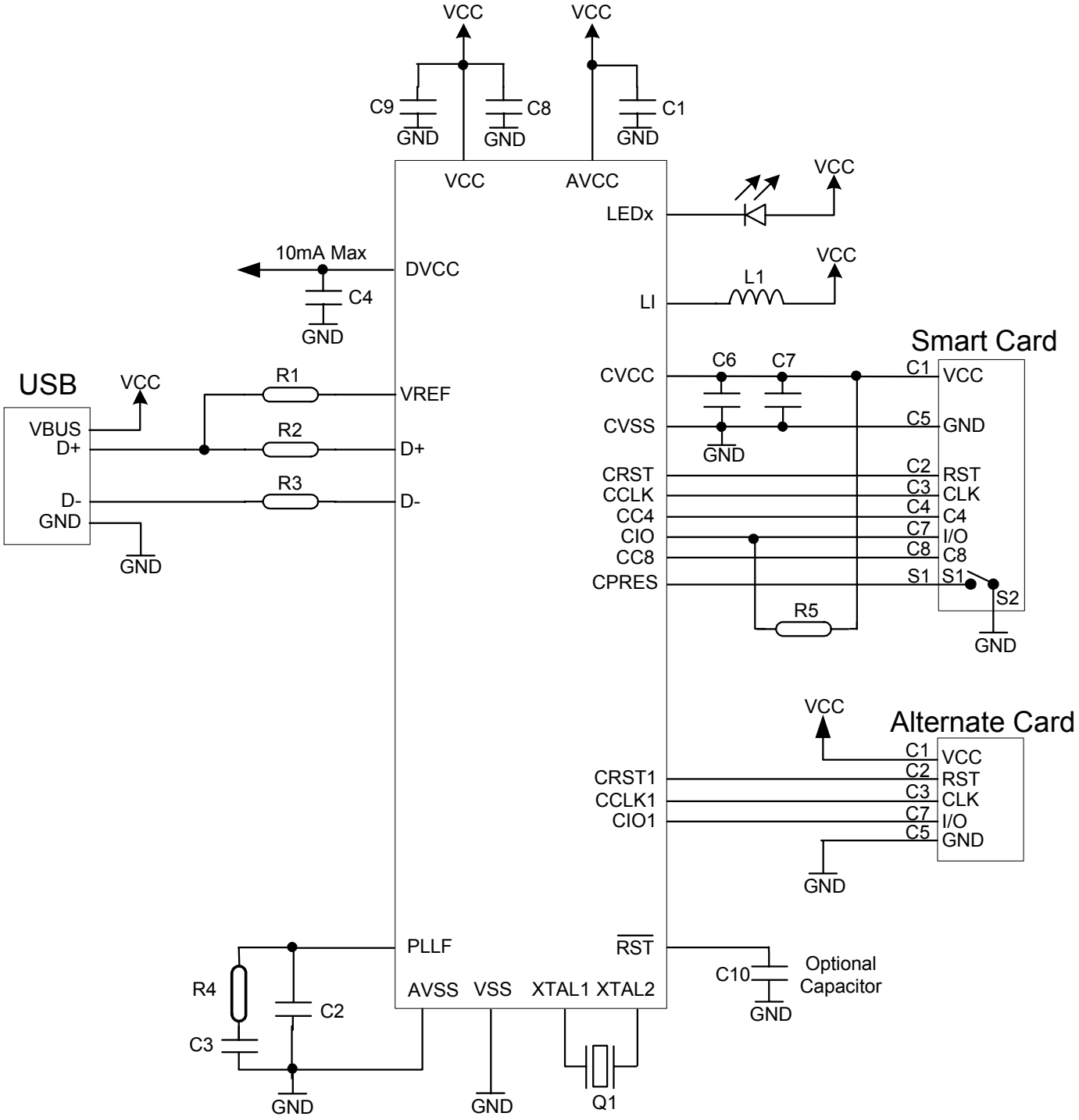




Notes :

1 - Pin configuration depends on product versions

USB Smart Card Reader Using the AT83C5123 Version



Registers

Table 5. Auxiliary Register - AUXR (8Eh)

7	6	5	4	3	2	1	0
DPU	-	-	-		XRS0	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	DPU	**Disable weak Pull-up** 0 weak pull-up is enabled 1 weak pull-up is disabled
6-3	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
2	XRS0	**XRAM Size** 0 256 bytes (default) 1 512 bytes
1	EXTRAM	**EXTRAM bit** Cleared to access internal XRAM using MOVX @ Ri/ @ DPTR. Set to access external memory. Programmed by hardware after Power-up regarding Hardware Security Byte (HSB), default setting , XRAM selected.
0	AO	**ALE Output bit** Cleared , ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used)(default). Set , ALE is active only when a MOVX or MOVC instruction is used.

Reset Value = 0XXX X000b

Table 6. Auxiliary Register 1 AUXR1- (0A2h) for AT8xC5122

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7 - 6	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
5	ENBOOT	**Enable Boot ROM (CRAM / E2PROM version only)** Set this bit to map the Boot ROM from 8000h to FFFFh. If the PC increments beyond 7FFFh address, the code is fetch from internal ROM Clear this bit to disable Boot ROM. If the PC increments beyond 7FFFh address, the code is fetch from external code memory (C51 standard roll over function) This bit is forced to 1 at reset
4	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
3	GF3	This bit is a general-purpose user flag.
2	0	Always cleared.
1	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
0	DPS	**Data Pointer Selection** Cleared to select DPTR0. Set to select DPTR1.

Reset Value = XX1X XX0X0b (Not bit addressable)

Table 7. Auxiliary Register 1 AUXR1- (0A2h) for AT83C5123

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7 - 6	-	**Reserved** The value read from this bit is indeterminate. Do not change these bits.
5		**Reserved** The value read from this bit is indeterminate. Do not change these bits.
4	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
3	GF3	This bit is a general-purpose user flag.
2	0	Always cleared.
1	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit.
0	DPS	**Data Pointer Selection** Cleared to select DPTR0. Set to select DPTR1.

Reset Value = XXXX XX0X0b (Not bit addressable)

AT8xC5122 Version

	Bit addressable	Not bit addressable					
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8h	UEPINT 0000 0000							
F0h	B 0000 0000	LEDCON0 0000 0000						
E8h	P5 1111 1111							
E0h	ACC 0000 0000	LEDCON1 XX00 0000	UBYCTX 0000 0000					
D8h								
D0h	PSW 0000 0000	RCON XXXX 0XXX			UEPCONX 1000 0000	UEPRST 0000 0000		
C8h							UEPSTAX 0000 0000	UEPDATX 0000 0000
SCRS=1 / SCRS=0 C0h	P4 1111 1111	SCICLK (1) 0X10 1111 / SCWT3 (1) 0000 0000	UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT 1111 1111	USBADDR 1000 0000	UEPNUM 0000 0000
B8h	IPL0 X000 000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0000 0000	DCCKPS 0000 0000
SCRS=1 / SCRS=0 B0h	P3 1111 1111	IEN1 XXXX X000	IPL1 00XX 00X0	IPH1 00XX 00X0	SCGT0 (1) 0000 1100 / SCWT0(1) 1000 0000	SCGT1(1) XXXX XXX0 / SCWT1 (1) 0010 0101	SCICR (1) 0000 0000 / SCWT2 (1) 0000 0000	IPH0 X000 0000
SCRS=1 / SCRS=0 A8h	IEN0 0000 0000	SADDR 0000 0000	SCIBUF XXXX XXXX	SCSR X000 1000	SCETU0 (1) 0111 0100 / SCCON (1) 0000 0000	SCETU1 (1) XXXX X001 / SCISR (1) 10X0 0000	SCIER (1) 0X00 0000 / SCIIR (1) 0X00 0000	
A0h	P2 1111 1111	ISEL 0000 0100	AUXR1 XX1X 0XX0	PLLCON XXXX X000	PLLDIV 0000 0000		WDTRST XXXX XXXX	WDTPRG XXXX X000
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000	
90h	P1 1111 1111	PMOD0(2) 0000 0000						CKRL XXXX 1111
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 0XXX X000	CKCON0 X0X0 X000
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000	PMOD1 0000 0000	CKSEL XXXX XXX0		PCON 00X1 0000

Notes: 1. Mapping is done using SCRS bit in SCSR register.
2. Grey areas : do not write in.

SFR's Description

Table 10. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator	ACC							
B	F0h	B Register	B							
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer	SP							
DPL	82h	Data Pointer Low byte (LSB of DPTR)	DPL							
DPH	83h	Data Pointer High byte (MSB of DPTR)	DPH							

Table 11. Clock SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Controller	SMOD1	SMOD0		POF	GF1	GF0	PD	IDL
CKCON0	8Fh	Clock Controller 0		WDX2		SIX2		T1X2	T0X2	X2
CKCON1	AFh	Clock Controller 1								SPIX2
CKSEL	85h	Clock Selection								CKS
CKRL	97h	Clock Reload Register					CKREL 3-0			
PLLCON	A3h	PLL Controller Register						EXT48	PLLEN	PLOCK
PLLDIV	A4h	PLL Divider register	R3-0				N3-0			
AUXR	8Eh	Auxiliary Register 0	DPU					XRS0	EXTRAM	A0
AUXR1	A2h	Auxiliary Register 1			ENBOOT(1)		GF3			DPS
RCON (1)	D1h	CRAM memory Configuration					RPS			

Note: 1. Only for AT8xC5122

Table 12. I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0(1)	80h	Port 0	P0							
P1	90h	Port 1	P1							
P2(1)	A0h	Port 2	P2							
P3	B0h	Port 3	P3							
P4(1)	C0h	Port 4	P4							
P5	E8h	Port 5	P5 (only P5.0 for AT8xC5122)							
PMOD0	91h	Port Mode Register 0	P3C1	P3C0	P2C1(1)	P2C0(1)	CPRESRES	-	P0C1(1)	P0C0(1)
PMOD1	84h	Port Mode Register 1	P5HC1(1)	P5HC0(1)	P5MC1(1)	P5MC0(1)	P5LC1	P5LC0	P4C1(1)	P4C0(1)

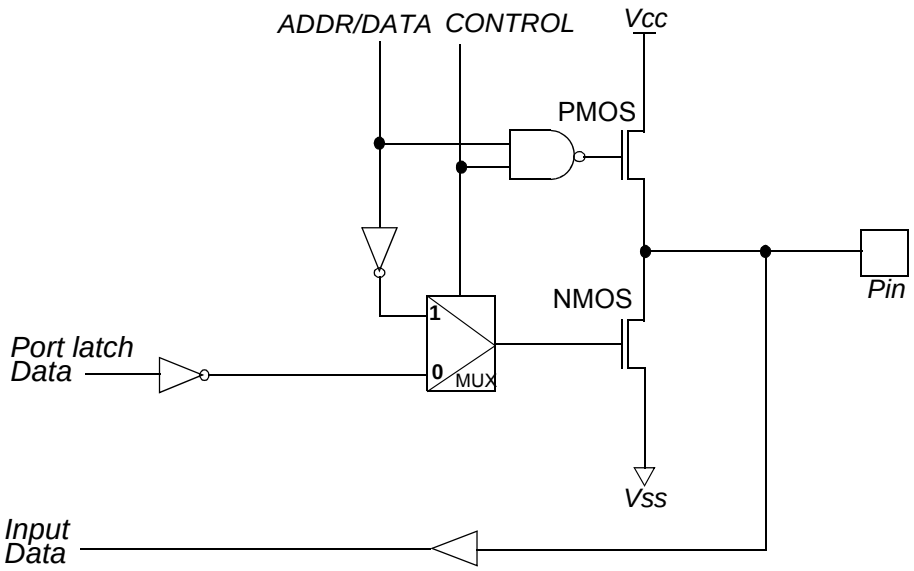
Note: 1. Only for AT8xC5122

Port Configuration

Standard I/O P0

The P0 port is described in Figure 22.

Figure 22. Standard Input/Output Port



Quasi Bi-directional Port

The default port output configuration for standard I/O ports is the quasi-bi-directional output that is common on the 80C51 and most of its derivatives. The “Port51” output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low.

When the port outputs a logic low state, it is driven strongly and is able to sink a fairly large current.

These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bi-directional output that serve different purposes.

One of these pull-ups, called the weak pull-up, is turned on whenever the port latch for the pin contains a logic 1. The weak pull-up sources a very small current that will pull the pin high if it is left floating. The weak pull-up can be turned off by the DPU bit in AUXR register.

A second pull-up, called the medium pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bi-directional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the medium pull-up turns off, and only the weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the medium pull-up and take the voltage on the port pin below its input threshold.

Note: for CIO, CC4, CC8 ports of SCIB interface , in input mode when the ICC (smart card) is driving the port pin :

- if 0 < Vin < CVCC/2 : weak pull-up is active (~100KOhm)
- if CVCC/2 < Vin < CVCC : weak (~100KOhm) and medium (~12KOhm) pull-up’s are active

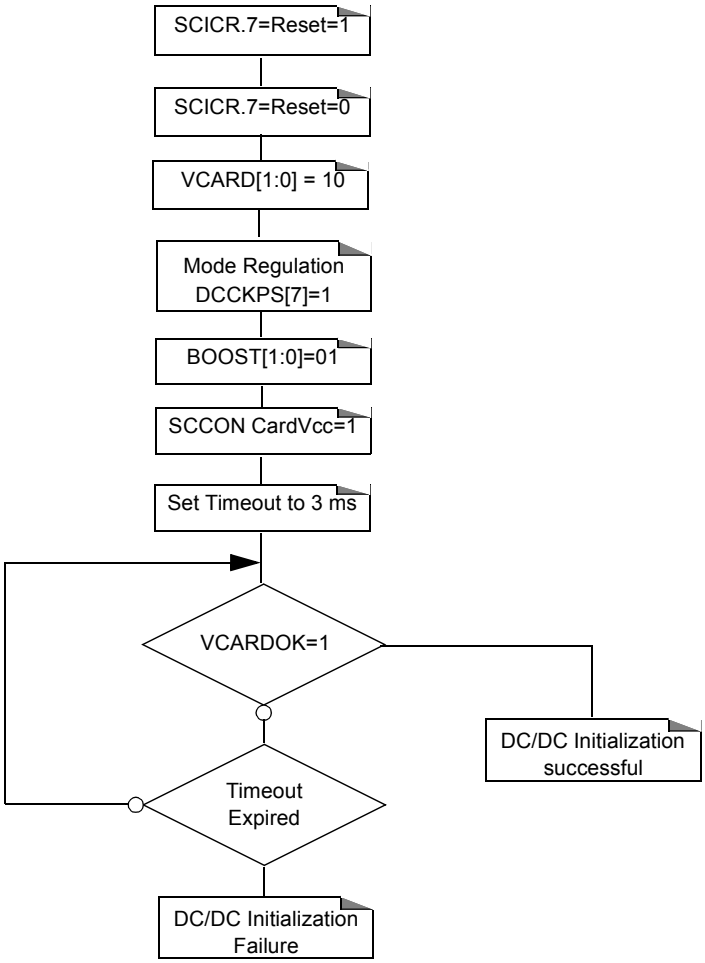
Table 44. Smart Card Interface Control Register - SCICR (S:B6h, SCRS = 1)

7	6	5	4	3	2	1	0
RESET	CARDDET	VCARD1	VCARD0	UART	WTEN	CREP	CONV

Bit Number	Bit Mnemonic	Description
7	RESET	**Reset** Set this bit to reset and deactivate the Smart Card Interface. Clear this bit to activate the Smart Card Interface. This bit acts as an active high software reset.
6	CARDDET	**Card Presence Detector Sense** Clear this bit to indicate the card presence detector is open when no card is inserted (CPRES is high). Set this bit to indicate the card presence detector is closed when no card is inserted (CPRES is low).
5-4	VCARD[1:0]	**Card Voltage Selection:** VCARD[1] VCARD[0] CVCC 0 0 0 V 0 1 1.8 V 1 0 3.0 V 1 1 5.0 V
3	UART	**Card UART Selection** Clear this bit to use the CARDIO bit (P1.0) bit to drive the Card I/O (P1.0) pin. Set this bit to use the Smart Card UART to drive the Card I/O pin (P1.0 pin). Controls also the Waiting Time Counter as described in Section “Waiting Time (WT) Counter”, page 67
2	WTEN	**Waiting Time Counter Enable** Clear this bit to stop the counter and enable the load of the Waiting Time counter hold registers. The hold registers are loaded with SCWT0, SCWT1, SCWT2 and SCWT3 values when SCWT2 is written. Set this bit to start the Waiting Time Counter. The counters stop when it reaches the timeout value. If the UART bit is set, the Waiting Time Counter automatically reloads with the hold registers whenever a start bit is sent or received.
1	CREP	**Character Repetition** Clear this bit to disable parity error detection and indication on the Card I/O pin in receive mode and to disable character repetition in transmit mode. Set this bit to enable parity error indication on the Card I/O pin in receive mode and to set automatic character repetition when a parity error is indicated in transmit mode. Depending upon CREPSET bit is SCSR register, the receiver can indicate parity error up to 4times (3 repetitions) or up to 5times (4 repetitions) after which it will raise the parity error bit SCPE bit in the SCISR register. If parity interrupt is enabled, the SCPI bit in SCIIR register will be set too. Alternately, the transmitter will detect ICC character repetition request. After 3 or 4 unsuccessful repetitions (depending on CREPSEL bit in SCSR register), the transmitter will raise the parity error bit SCPE bit in the SCISR register. If parity interrupt is enabled, the SCPI bit in SCIIR register will be set too. **Note** : Character repetition mode is specified for T=0 protocol only and should not be used in T=1 protocol (block oriented protocol)
0	CONV	**ISO Convention** Clear this bit to use the direct convention: b0 bit (LSB) is sent first, the parity bit is added after b7 bit and a low level on the Card I/O pin represents a’0’. Set this bit to use the inverse convention: b7 bit (LSB) is sent first, the parity bit is added after b0 bit and a low level on the Card I/O pin represents a’1’.

Reset Value = 0000 0000b

Figure 46. Card Vcc = 3V Initialization Procedure



advised to decrement the BOOST[1:0] bits to restore the overflow current to its normal or desired value.

Monitoring Procedure

Once the DC/DC has been successfuly initialized, it is necessary to monitor the DC/DC converter by means of bits VCARDOK and ICARDOVF in the SCISR register.

Table 60. DC/DC converter status

VCARDOK	ICARDOVF	DC/DC Status
0	0	- Not Started or switched off by application. The current overflow sensor is disabled during the DC/DC converter startup. Then if a current overflow condition is applied during the DC/DC converter startup, the DC/DC converter is unable to start and both bits VCARDOK and ICARDOVF remains at 0.
		DC/DC converter correctly started then the output voltage is out of ISO/IEC 7816-3 specifications. In this case the firmware must take appropriate actions like deactivating the DC/DC converter in compliance with ISO/IEC 7816.
0	1	Started and automatically switched off by a current overflow condition
1	0	Operating properly according to ISO/IEC 7816-3 and EMV recommendations
1	1	Not applicable

Figure 59. Example of REMOTE WAKEUP Management

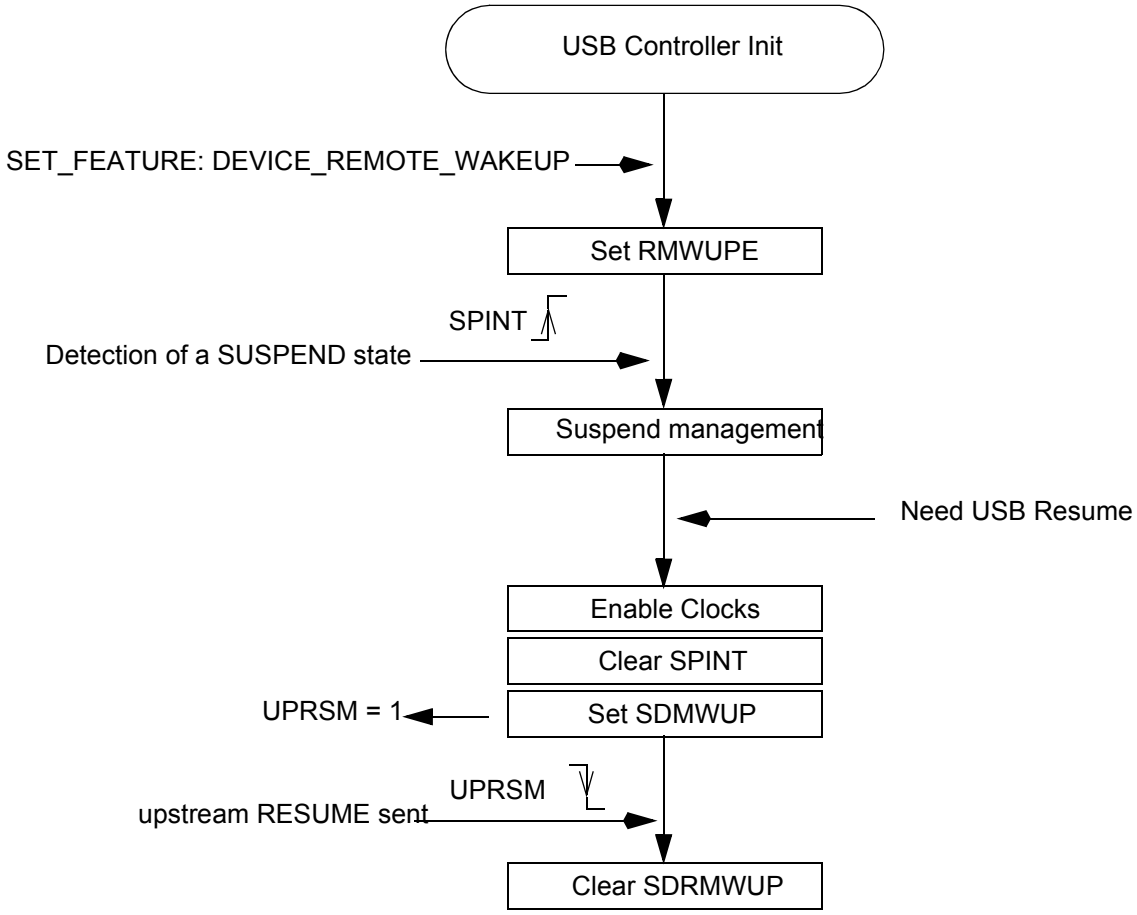


Figure 63. USB Interrupt Control Block Diagram

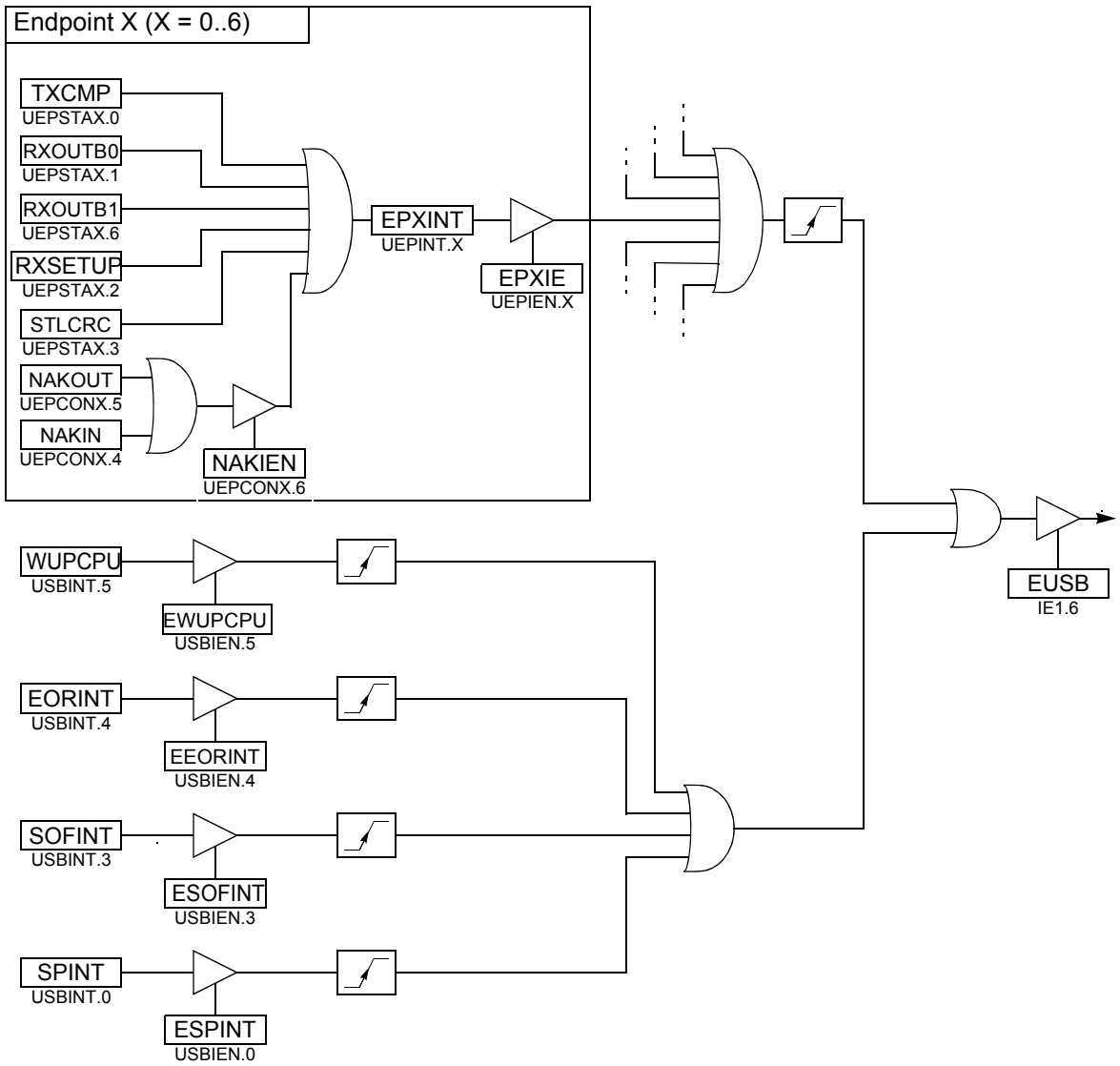


Table 66. USB Global Interrupt Enable Register - USBIEN (S:BEh)

7	6	5	4	3	2	1	0
-	-	EWUPCPU	EEORINT	ESOFINT	-	-	ESPINT

Bit Number	Bit Mnemonic	Description
7 - 6	-	**Reserved** The value read from these bits is always 0. Do not change these bits.
5	EWUPCPU	**Enable Wake-up CPU Interrupt** Set this bit to enable Wake-up CPU Interrupt. Clear this bit to disable Wake-up CPU Interrupt.
4	EEORINT	**Enable End of Reset Interrupt** Set this bit to enable End of Reset Interrupt. This bit is set after reset. Clear this bit to disable End of Reset Interrupt.
3	ESOFINT	**Enable SOF Interrupt** Set this bit to enable SOF Interrupt. Clear this bit to disable SOF Interrupt.
2-1	-	**Reserved** The value read from these bits is always 0. Do not change these bits.
0	ESPINT	**Enable Suspend Interrupt** Set this bit to enable Suspend Interrupts (See Table 65 on page 116). Clear this bit to disable Suspend Interrupts.

Reset Value = 0001 0000b

Table 67. USB Address Register - USBADDR (S:C6h)

7	6	5	4	3	2	1	0
FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0

Bit Number	Bit Mnemonic	Description
7	FEN	**Function Enable** Set this bit to enable the function. FADD is reset to 1. Cleared this bit to disable the function.
6-0	UADD[6:0]	**USB Address** This field contains the default address (0) after power-up or USB bus reset. It should be written with the value set by a SET_ADDRESS request received by the device firmware.

Reset Value = 1000 0000b

Table 68. USB Endpoint Number - UEPNUM (S:C7h)

7	6	5	4	3	2	1	0
-	-	-	-	EPNUM3	EPNUM2	EPNUM1	EPNUM0

Bit Number	Bit Mnemonic	Description
7 - 4	-	**Reserved** The value read from these bits is always 0. Do not change these bits.
3 - 0	EPNUM[3:0]	**Endpoint Number** Set this field with the number of the endpoint which should be accessed when reading or writing to, USB Byte Count Register X (X=EPNUM set in UEPNUM Register) - UBYCTX (S:E2h) or USB Endpoint X Control Register - UEPCONX (S:D4h). This value can be 0, 1, 2, 3, 4, 5 or 6.

Reset Value = 0000 0000b

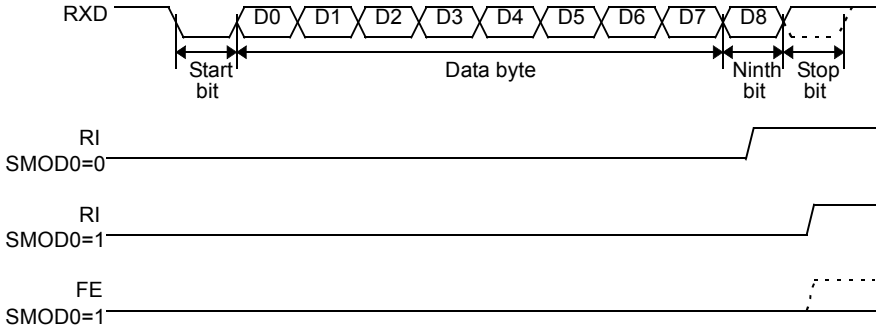
Table 69. USB Endpoint X Control Register - UEPCONX (S:D4h)

7	6	5	4	3	2	1	0
EPEN	NAKIEN	NAKOUT	NAKIN	DTGL	EPDIR	EPTYPE1	EPTYPE0

Bit Number	Bit Mnemonic	Description
7	EPEN	**Endpoint Enable** Set this bit to enable the endpoint according to the device configuration. Endpoint 0 will always be enabled after a hardware or USB bus reset and participate in the device configuration. Clear this bit to disable the endpoint according to the device configuration.
6	NAKIEN	**NAK Interrupt Enable** Set this bit to enable NAKIN and NAKOUT Interrupt. Clear this bit to disable NAKIN and NAKOUT Interrupt.
5	NAKOUT	**NAK OUT Sent** This bit is set by hardware when the a NAK handshake is sent by the USB controller to an OUT request from the Host. This generates an interrupt if the NAKIEN bit is set. This bit shall be cleared by software.
4	NAKIN	**NAK IN Sent** This bit is set by hardware when the a NAK handshake is sent by the USB controller to an IN request from the Host. This generates an interrupt if the NAKIEN bit is set. This bit shall be cleared by software.
3	DTGL	**Data Toggle (Read-only)** This bit is set by hardware when a valid DATA0 packet is received and accepted. This bit is cleared by hardware when a valid DATA1 packet is received and accepted.
2	EPDIR	**Endpoint Direction** Set this bit to configure IN direction for Bulk, Interrupt and Isochronous endpoints. Clear this bit to configure OUT direction for Bulk, Interrupt and Isochronous endpoints. This bit has no effect for Control endpoints.
1-0	EPTYPE[1:0]	**Endpoint Type** Set this field according to the endpoint configuration (Endpoint 0 will always be configured as control): 00Control endpoint 01Isochronous endpoint 10Bulk endpoint 11Interrupt endpoint

Reset Value = 1000 0000b when UEPNUM = 0
Reset Value = 0000 0000b otherwise

Figure 66. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.
To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't care bits (defined by zeros) to form the device's given address. The don't care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:SADDR1111 0001b
SADEN1111 1010b
Given1111 0X0Xb

Slave B:SADDR1111 0011b
SADEN1111 1001b
Given1111 0XX1b

Slave C:SADDR1111 0011b
SADEN1111 1101b
Given1111 00X1b

Slave Select ($\overline{SS}$)

Each Slave peripheral is selected by one Slave Select pin ($\overline{SS}$). This signal must stay low for any message for a Slave. Only one Master ($\overline{SS}$ high level) can drive the network. The Master may select each Slave device by software through port pins (Figure 82). To prevent bus conflicts on the MISO line, only one slave should be selected at a time by the Master for a transmission.

In a Master configuration, the $\overline{SS}$ line can be used in conjunction with the MODF flag in the SPI Status register (SPSTA) to prevent multiple masters from driving MOSI and SCK (see Section “Error Conditions”, page 140).

A high level on the $\overline{SS}$ pin puts the MISO line of a Slave SPI in a high-impedance state.

The $\overline{SS}$ pin could be used as a general-purpose if the following conditions are met:

- The device is configured as a Master and the SSDIS control bit in SPCON is set. This kind of configuration can be found when only one Master is driving the network and there is no way that the $\overline{SS}$ pin will be pulled low. Therefore, the MODF flag in the SPSTA will never be set (1).
- The Device is configured as a Slave with CPHA and SSDIS control bits set (2). This kind of configuration can happen when the system comprises one Master and one Slave only. Therefore, the device should always be selected and there is no reason that the Master uses the $\overline{SS}$ pin to select the communicating Slave device.

Baud Rate

In Master mode, the baud rate can be selected from a baud rate generator which is controled by three bits in the SPCON register: SPR2, SPR1 and SPR0. The Master clock is chosen from one of six clock rates resulting from the division of the internal clock by 4, 8, 16, 32, 64 or 128.

Table 83 gives the different clock rates selected by SPR2:SPR1:SPR0

Table 83. SPI Master Baud Rate Selection

SPR2:SPR1:SPR0	Clock Rate	Baud Rate Divisor (BD)
000	Reserved	N/A
001	F_{CK_SPI} /4	4
010	F_{CK_SPI} / 8	8
011	F_{CK_SPI} /16	16
100	F_{CK_SPI} /32	32
101	F_{CK_SPI} /64	64
110	F_{CK_SPI} /128	128
111	Reserved	N/A

1. Clearing SSDIS control bit does not clear MODF.
2. Special care should be taken not to set SSDIS control bit when CPHA = ’0’ because in this mode, the $\overline{SS}$ is used to start the transmission.

Interrupt Sources and Vectors

Table 108. Interrupt Vectors

Interrupt Source	Polling Priority at Same Level	Vector Address
Reset	0 (Highest Priority)	C:0000h
INT0	1	C:0003h
Timer 0	2	C:000Bh
INT1	3	C:0013h
Timer 1	4	C:001Bh
UART	6	C:0023h
Reserved	7	C:002Bh
Reserved	5	C:0033h
Keyboard Controller (1)	8	C:003Bh
Reserved	9	C:0043h
SPI Controller (1)	10	C:004Bh
Smart Card Controller	11	C:0053h
Reserved	12	C:005Bh
Reserved	13	C:0063h
USB Controller	14	C:006Bh
Reserved	15 (Lowest Priority)	C:0073h

Note: 1. Only fot AT8xC5122

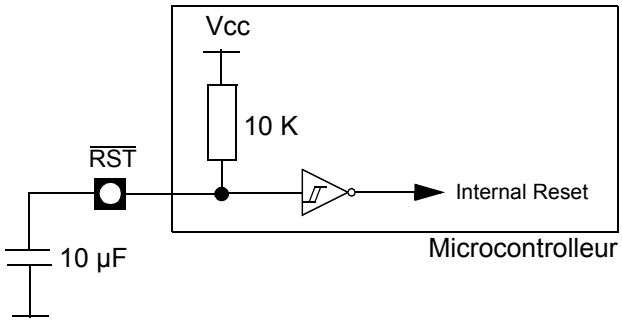
Reset pin

As explained in the POR section there is no need to use the reset pin as the internal reset function at power up is ensured by the POR. Anyway, if some applications requires a long reset, a reset controlled by the user or a reset controlled by external superviser device, the use of the reset pin is necessary.

Long Reset

As the pad integrates an internal pull-up of 10K, only an external capacitor of at least 10 µF is required to have an impact on the reset duration.

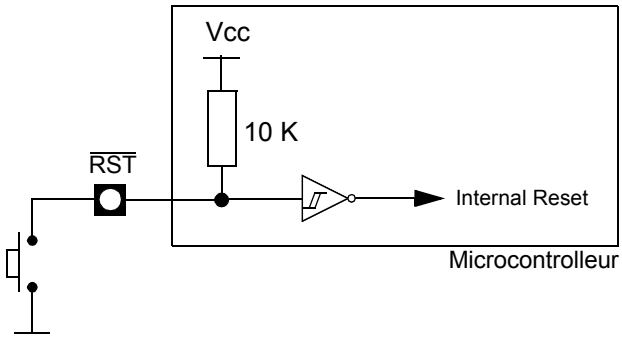
Figure 103. Long Reset



Reset Controlled by the User

The external capacitor is not needed if no long reset is required.

Figure 104. Reset Controlled by the User



Electrical Characteristics

Absolute Maximum Ratings

Ambiant Temperature Under Bias .....-25°C to 85°C
Storage Temperature ..... -65°C to + 150°C
Voltage on V_{CC} to V_{SS} .....-0.5 V to + 6.0V
Voltage on Any Pin to V_{SS}.....-0.5 V to V_{CC} + 0.5 V
Power Dissipation 1 W

Note: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
Power Dissipation value is based on the maximum allowable die temperature and the thermal resistance of the package.

DC Parameters

T_A = -40 to +85°C; V_{SS} = 0 V, F_{CK_CPU}= 0 to 24 MHz , V_{CC} = 3.0V to 5.5V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, $\overline{RST}$	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, $\overline{RST}$	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage: P0, ALE, PSEN			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage: P0, ALE, PSEN	0.9 V_{CC}			V	I_{OH} = 10 µA
V_{OL1}	Output Low Voltage: P2, P3, P4, P5, P1.2, P1.6, P1.7			0.45	V	I_{OL} = 0.8 mA
V_{OH1}	Output High Voltage: P2, P3, P4, P5, P1.2, P1.6, P1.7	0.9 V_{CC}			V	I_{OH} = -10 µA
I_{IL}	Logical 0 Input Current ports 2 to 5 and P1.2, P1.6, P1.7, if Weak pull-up enabled			-50	µA	Vin = 0.45 V
I_{LI}	Input Leakage Current			±10	µA	0.45 V < V_{IN} < V_{CC}
I_{TL}	Logical 1 to O transistion Current, Port 51 configuration			–650	µA	V_{IN} = 2 V
R_{MEDIUM}	Medium Pullup Resistor		10		kΩ	
R_{WEAK}	Weak Pullup Resistor		100		kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1MHz T_A = 25°C
DV_{CC}	Digital Supply Voltage	3	3.4	3.6	V	C_L = 470 nF
DI_{CC}	Digital Supply Output Current (DVcc pin)			10	mA	C_L = 100 nF F_{CK_CPU} = 24 MHz
V_{PFDP}	Power Fail High Level Threshold		2.8	3	V	
V_{PFDM}	Power Fail Low Level Threshold	2,5	2.6		V	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1µs		600	second	