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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.18x24.18)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c552sbaa-512

DESCRIPTION

The 87C552 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C552 has the same instruction set as the 80C51.

The 87C552 contains a 8k × 8 non-volatile EPROM, a 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, four-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I^{2}C-bus), a “watchdog” timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8xC552 can be expanded using standard TTL compatible memories and logic.

In addition, the 8xC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. Optionally, the ADC can be operated in Idle mode. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instructions require 3µs.

FEATURES

- 80C51 central processing unit
- 8k × 8 EPROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 × 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Fast 8-bit ADC option
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I^{2}C-bus serial I/O port with byte oriented master and slave functions
- On-chip watchdog timer
- Extended temperature ranges
- Full static operation – 0 to 16 MHz
- Operating voltage range: 2.7V to 5.5V (0 to 16MHz)
- Security bits:
  - OTP/EPROM – 3 bits
- Encryption array – 64 bytes
- 4 level priority interrupt
- 15 interrupt sources
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Clock can be stopped and resumed
  - Idle mode
  - Power down mode
- Second DPTR register
- ALE inhibit for EMI reduction
- Programmable I/O pins
- Wake-up from power-down by external interrupts
- Software reset
- Power-on detect reset
- ADC charge pump disable
- ONCE mode
- ADC active in Idle mode

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
P1M1	Port 1 output mode 1	92H									xx000000B
P1M2	Port 1 output mode 2	93H									xx000000B
P2M1	Port 2 output mode 1	94H									00H
P2M2	Port 2 output mode 2	95H									00H
P3M1	Port 3 output mode 1	9AH									00H
P3M2	Port 3 output mode 2	9BH									00H
P4M1	Port 4 output mode 1	9CH									00H
P4M2	Port 4 output mode 2	9DH									00H
PCON	Power control	87H	SMOD1	SMOD0	POF	WLE	GF1	GFO	PD	IDL	00x00000B
PSW	Program status word	D0H	CY	AC	FO	RS1	RS0	OV	F1	P	00H
PWMP#	PWM prescaler	FEH									00H
PWM1#	PWM register 1	FDH									00H
PWM0#	PWM register 0	FCH									00H
RTE#	Reset/toggle enable	EFH	TP47	TP46	RP45	RP44	RP43	RP42	RP41	RP40	00H
S0ADDR	Serial 0 slave address	F9H									00H
S0ADEN	Slave address mask	B9H									00H
S0BUF	Serial 0 data buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
S0CON*	Serial 0 control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
S1ADR#	Serial 1 address	DBH	SLAVE ADDRESS							GC	00H
SIDAT#	Serial 1 data	DAH									00H
S1STA#	Serial 1 status	D9H	SC4	SC3	SC2	SC1	SC0	0	0	0	F8H
			DF	DE	DD	DC	DB	DA	D9	D8	
SICON#*	Serial 1 control	D8H	CR2	ENS1	STA	ST0	SI	AA	CR1	CR0	00H
SP	Stack pointer	81H									07H
STE#	Set enable	EEH	TG47	TG46	SP45	SP44	SP43	SP42	SP41	SP40	C0H
TH1	Timer high 1	8DH									00H
TH0	Timer high 0	8CH									00H
TL1	Timer low 1	8BH									00H
TL0	Timer low 0	8AH									00H
TMH2#	Timer high 2	EDH									00H
TML2#	Timer low 2	ECH									00H
TMOD	Timer mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TM2CON#	Timer 2 control	EAH	T2IS1	T2IS0	T2ER	T2B0	T2P1	T2P0	T2MS1	T2MS0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
TM2IR#*	Timer 2 int flag reg	C8H	T20V	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0	00H
T3#	Timer 3	FFH									00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by either (1) externally holding the RST pin high for at least two machine cycles (24 oscillator periods) or (2) internally by an on-chip power-on detect (POD) circuit which detects V_{CC} ramping up from 0V.

To insure a good external power-on reset, the RST pin must be high long enough for the oscillator to start up (normally a few milliseconds) plus two machine cycles. The voltage on V_{DD} and the RST pin must come up at the same time for a proper startup.

For a successful internal power-on reset, the V_{CC} voltage must ramp up from 0V smoothly at a ramp rate greater than 5V/100 ms.

The RST line can also be pulled HIGH internally by a pull-up transistor activated by the watchdog timer T3. The length of the output pulse from T3 is 3 machine cycles. A pulse of such short duration is necessary in order to recover from a processor or system fault as fast as possible.

Note that the short reset pulse from Timer T3 cannot discharge the power-on reset capacitor (see Figure 2). Consequently, when the watchdog timer is also used to set external devices, this capacitor arrangement should not be connected to the RST pin, and a different circuit should be used to perform the power-on reset operation. A timer T3 overflow, if enabled, will force a reset condition to the 8XC554 by an internal connection, independent of the level of the RST pin.

A reset may be performed in software by setting the software reset bit, SRST (AUXR1.5).

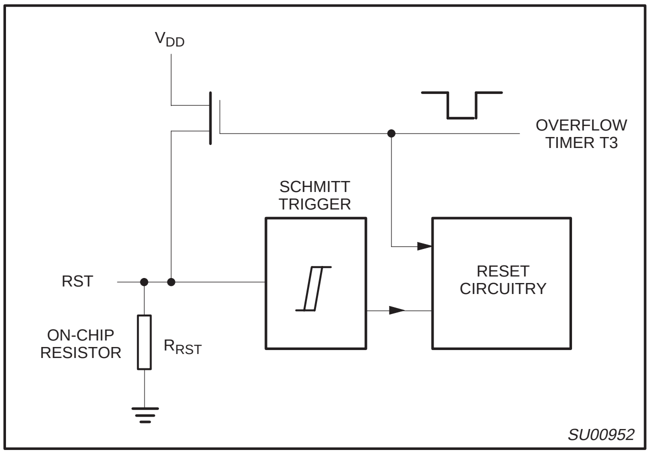

Figure 1. On-Chip Reset Configuration

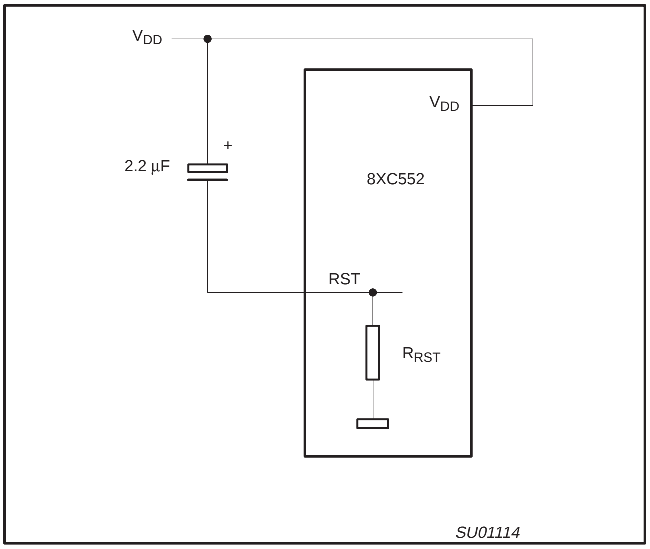

Figure 2. Power-On Reset

LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while some of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. The Wake-up from Power-down bit, WUPD (AUXR1.3) must be set in order for an external interrupt to cause a wake-up from power-down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

AUXR Address = 8EH Reset Value = xxxx x110B

Not Bit Addressable

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	**LVADC**	**–**	**AO**

Symbol	**Function**	
AO	Disable/Enable ALE	
	AO	**Operating Mode**
	0	ALE is emitted at a constant rate of 1/6 the oscillator frequency.
	1	ALE is active only during a MOVX or MOVC instruction.
LVADC	Enable A/D low voltage operation	
	LVADC	**Operating Mode**
	0	Turns off A/D charge pump.
	1	Turns on A/D charge pump. Required for operation below 4V.
—	Not implemented, reserved for future use*.	

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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Figure 4. AUXR: Auxiliary Register

Dual DPTR

The dual DPTR structure (see Figure 5) is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

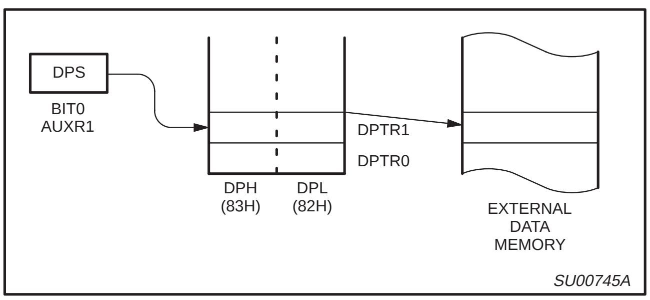

Figure 5.

Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the other bits.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR , A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

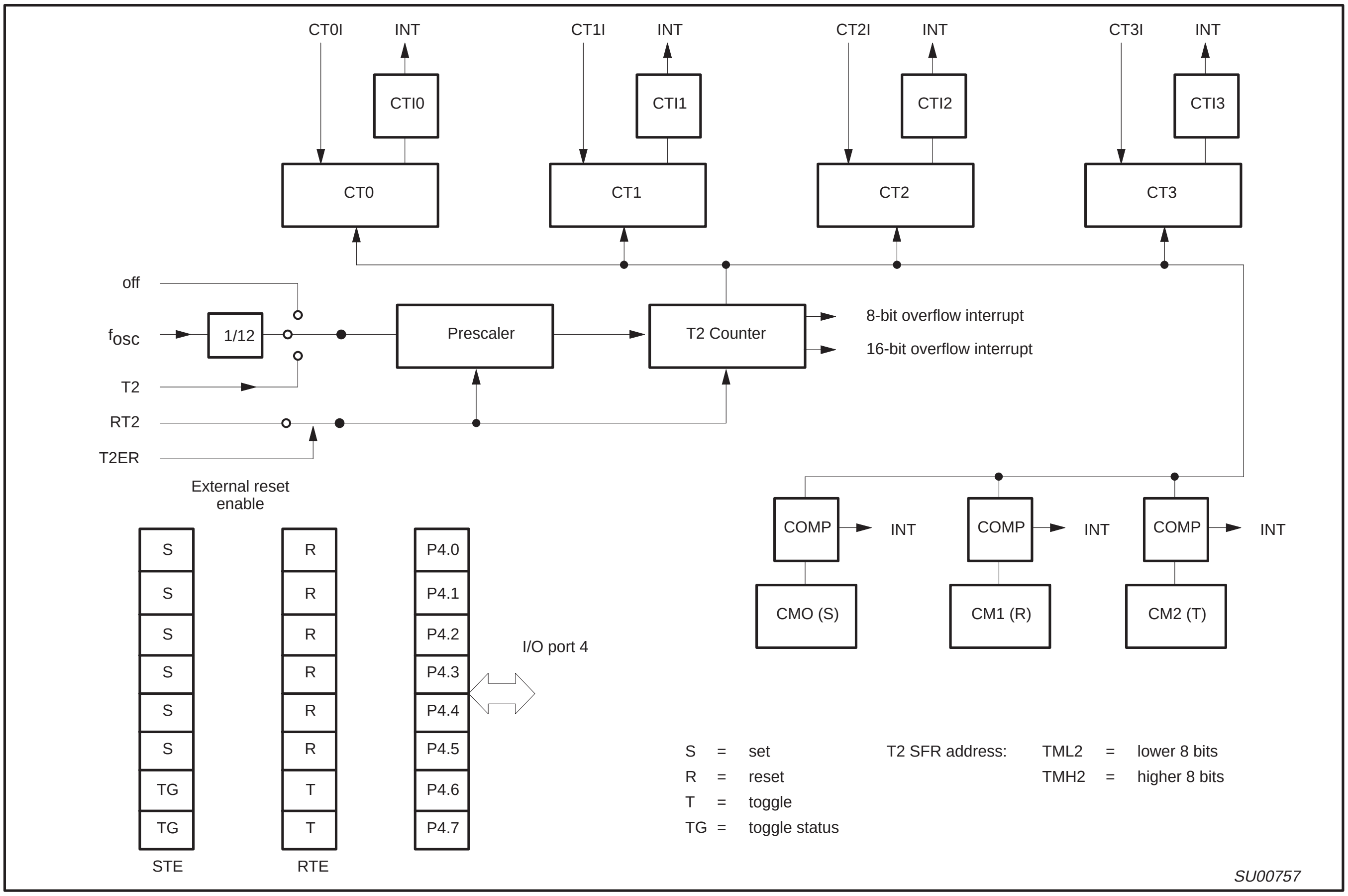

Figure 12. Block Diagram of Timer 2

Capture Logic: The four 16-bit capture registers that Timer T2 is connected to are: CT0, CT1, CT2, and CT3. These registers are loaded with the contents of Timer T2, and an interrupt is requested upon receipt of the input signals CT0I, CT1I, CT2I, or CT3I. These input signals are shared with port 1. The four interrupt flags are in the Timer T2 interrupt register (TM2IR special function register). If the capture facility is not required, these inputs can be regarded as additional external interrupt inputs.

Using the capture control register CTCON (see Figure 13), these inputs may capture on a rising edge, a falling edge, or on either a rising or falling edge. The inputs are sampled during S1P1 of each cycle. When a selected edge is detected, the contents of Timer T2 are captured at the end of the cycle.

Measuring Time Intervals Using Capture Registers: When a recurring external event is represented in the form of rising or falling edges on one of the four capture pins, the time between two events can be measured using Timer T2 and a capture register. When an event occurs, the contents of Timer T2 are copied into the relevant capture register and an interrupt request is generated. The interrupt service routine may then compute the interval time if it knows the previous contents of Timer T2 when the last event occurred. With a 12MHz oscillator, Timer T2 can be programmed to overflow every 524ms. When event interval times are shorter than this, computing the interval time is simple, and the interrupt service routine is short. For longer interval times, the Timer T2 extension routine may be used.

Compare Logic: Each time Timer T2 is incremented, the contents of the three 16-bit compare registers CM0, CM1, and CM2 are compared with the new counter value of Timer T2. When a match is found, the corresponding interrupt flag in TM2IR is set at the end of the following cycle. When a match with CM0 occurs, the controller sets bits 0-5 of port 4 if the corresponding bits of the set enable register STE are at logic 1.

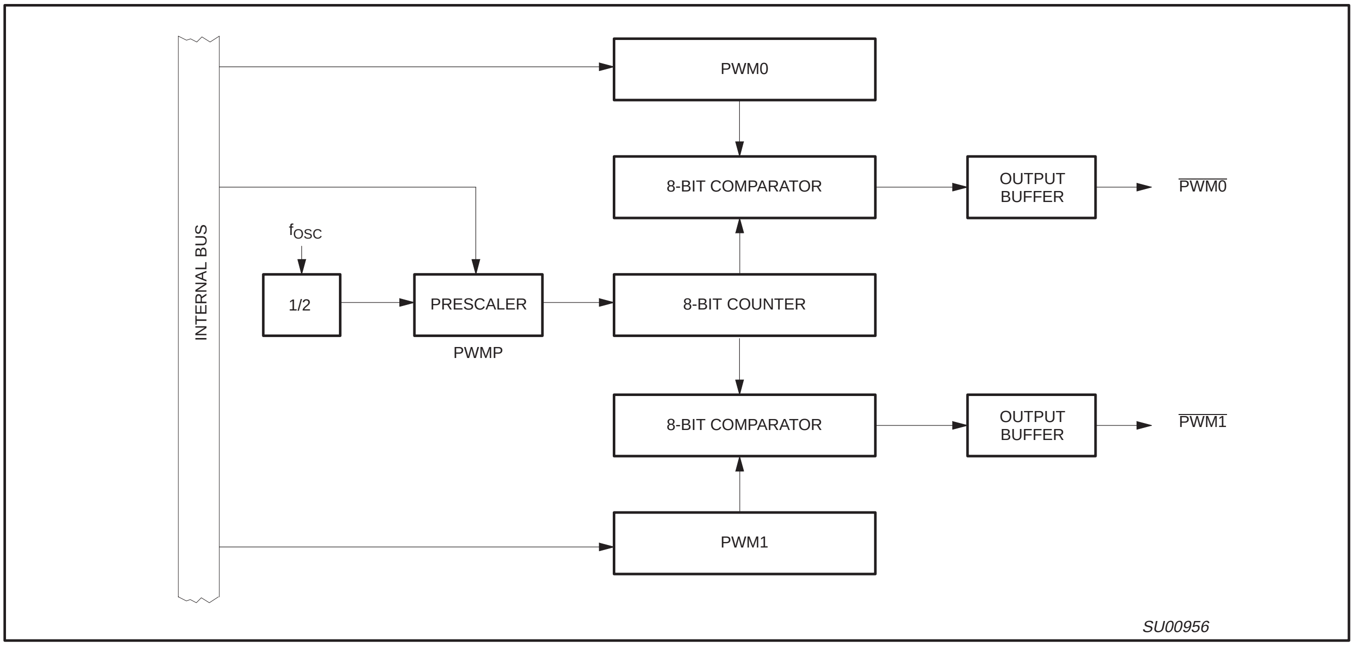

Figure 18. Functional Diagram of Pulse Width Modulated Outputs

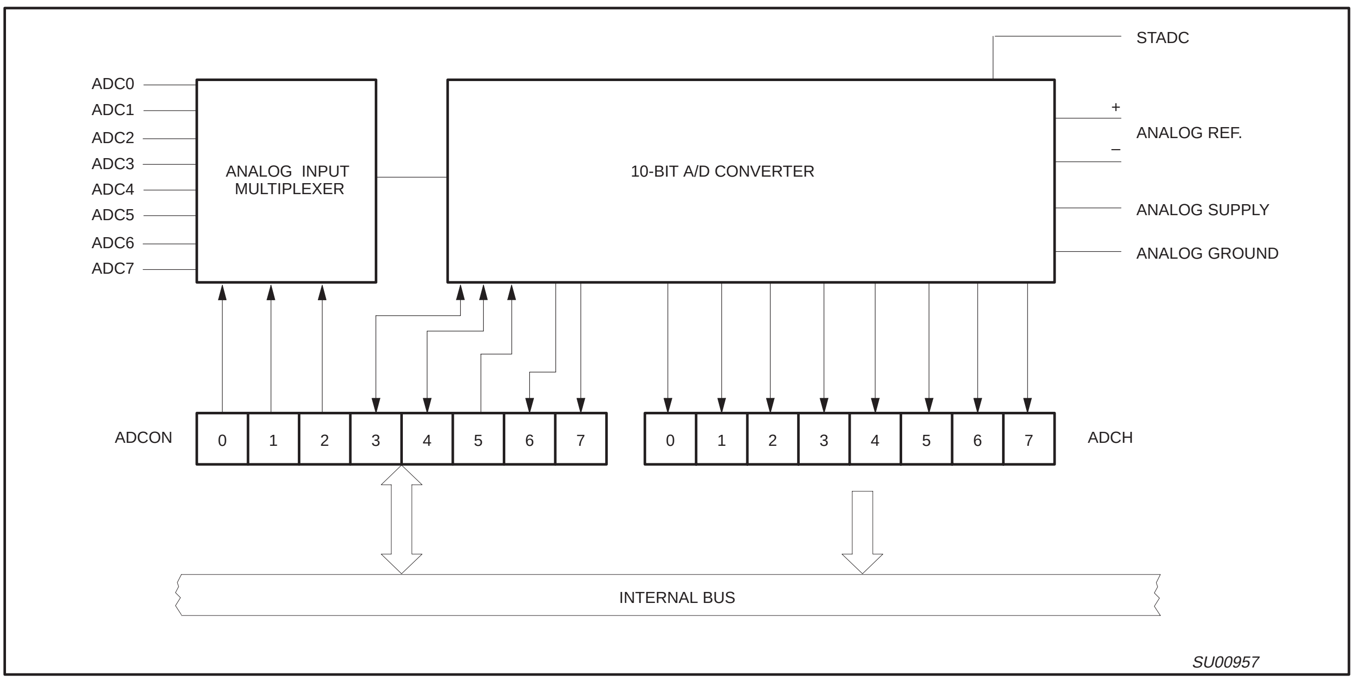

Figure 19. Functional Diagram of Analog Input Circuitry

10-Bit Analog-to-Digital Conversion: Figure 20 shows the elements of a successive approximation (SA) ADC. The ADC contains a DAC which converts the contents of a successive approximation register to a voltage (VDAC) which is compared to the analog input voltage (Vin). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. A conversion is initiated by setting ADCS in the ADCON register. ADCS can be set by software only or by either hardware or software.

The software only start mode is selected when control bit ADCON.5 (ADEX) = 0. A conversion is then started by setting control bit ADCON.3 (ADCS). The hardware or software start mode is selected when ADCON.5 = 1, and a conversion may be started by setting ADCON.3 as above or by applying a rising edge to external pin STADC. When a conversion is started by applying a rising edge, a low level must be applied to STADC for at least one machine cycle followed by a high level for at least one machine cycle.

Reset Value = xx00 0000B

	7	6	5	4	3	2	1	0
ADCON (C5H)	ADC.1	ADC.0	ADEX	ADCI	ADCS	AADR2	AADR1	AADR0
	(MSB)							(LSB)

Bit	Symbol	Function
ADCON.7	ADC.1	Bit 1 of ADC result
ADCON.6	ADC.0	Bit 0 of ADC result
ADCON.5	ADEX	Enable external start of conversion by STADC 0 = Conversion can be started by software only (by setting ADCS) 1 = Conversion can be started by software or externally (by a rising edge on STADC)
ADCON.4	ADCI	ADC interrupt flag: this flag is set when an A/D conversion result is ready to be read. An interrupt is invoked if it is enabled. The flag may be cleared by the interrupt service routine. While this flag is set, the ADC cannot start a new conversion. ADCI cannot be set by software.
ADCON.3	ADCS	ADC start and status: setting this bit starts an A/D conversion. It may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion, ADCS is reset immediately after the interrupt flag has been set. ADCS cannot be reset by software. A new conversion may not be started while either ADCS or ADCI is high.

ADCI	ADCS	ADC Status
0	0	ADC not busy; a conversion can be started
0	1	ADC busy; start of a new conversion is blocked
1	0	Conversion completed; start of a new conversion requires ADCI=0
1	1	Conversion completed; start of a new conversion requires ADCI=0

If ADCI is cleared by software while ADCS is set at the same time, a new A/D conversion with the same channel number may be started.
But it is recommended to reset ADCI ***before*** ADCS is set.

Bit	Symbol	Function
ADCON.2 ADCON.1 ADCON.0	AADR2 AADR1 AADR0	Analogue input select: this binary coded address selects one of the eight analogue port bits of P5 to be input to the converter. It can only be changed when ADCI and ADCS are both LOW.

AADR2	AADR1	AADR0	Selected Analog Channel
0	0	0	ADC0 (P5.0)
0	0	1	ADC1 (P5.1)
0	1	0	ADC2 (P5.2)
0	1	1	ADC3 (P5.3)
1	0	0	ADC4 (P5.4)
1	0	1	ADC5 (P5.5)
1	1	0	ADC6 (P5.6)
1	1	1	ADC7 (P5.7)

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Figure 22. ADC Control Register (ADCON)

10-Bit ADC Resolution and Analog Supply: Figure 23 shows how the ADC is realized. The ADC has its own supply pins (AV_{DD} and AV_{SS}) and two pins (Vref+ and Vref–) connected to each end of the DAC's resistance-ladder. The ladder has 1023 equally spaced taps, separated by a resistance of "R". The first tap is located 0.5 x R above Vref–, and the last tap is located 1.5 x R below Vref+. This gives a total ladder resistance of 1024 x R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error as shown in Figure 25.

For input voltages between Vref– and (Vref–) + 1/2 LSB, the 10-bit result of an A/D conversion will be 00 0000 0000B = 000H. For input voltages between (Vref+) – 3/2 LSB and Vref+, the result of a conversion will be 11 1111 1111B = 3FFH. AVref+ and AVref– may be between AV_{DD} + 0.2V and AV_{SS} – 0.2V. AVref+ should be positive with respect to AVref–, and the input voltage (Vin) should be between AVref+ and AVref–. If the analog input voltage range is from 2V to 4V, then 10-bit resolution can be obtained over this range if AVref+ = 4V and AVref– = 2V.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{V_{IN} - AV_{ref-}}{AV_{ref+} - AV_{ref-}}$$

Power Reduction Modes

The 8XC552 has two reduced power modes of operation: the idle mode and the power-down mode. These modes are entered by setting bits in the PCON special function register. When the 8XC552 enters the idle mode, the following functions are disabled:

CPU	(halted)
Timer T2	(halted and reset)
PWM0, PWM1	(reset; outputs are high)
ADC	(may be enabled for operation in Idle mode by setting bit AIDC (AUXR1.6)).

In idle mode, the following functions remain active:

Timer 0
Timer 1
Timer T3
SIO0 SIO1
External interrupts

When the 8XC552 enters the power-down mode, the oscillator is stopped. The power-down mode is entered by setting the PD bit in the PCON register. The PD bit can only be set if the $\overline{EW}$ input is tied HIGH.

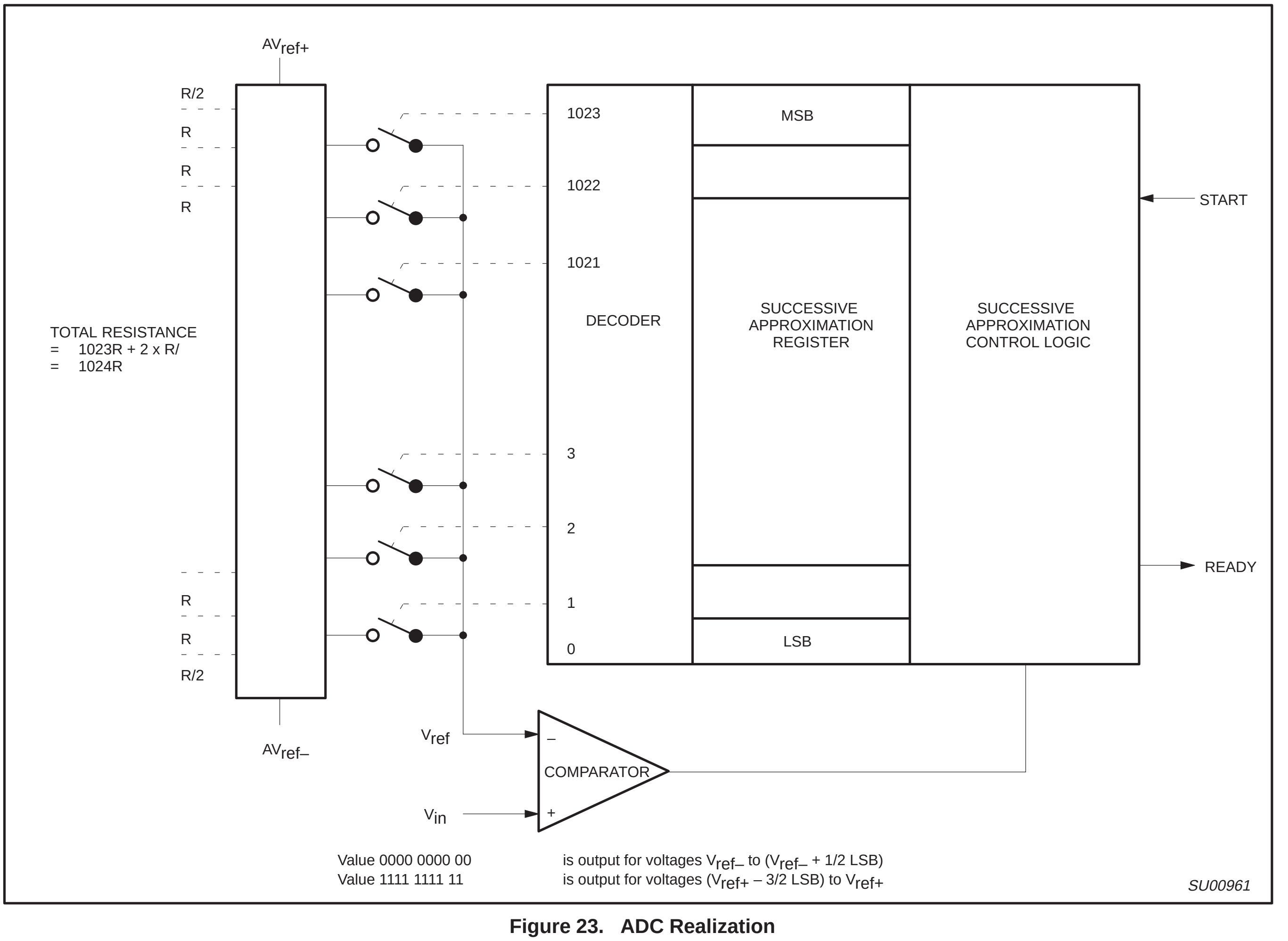

Figure 23. ADC Realization

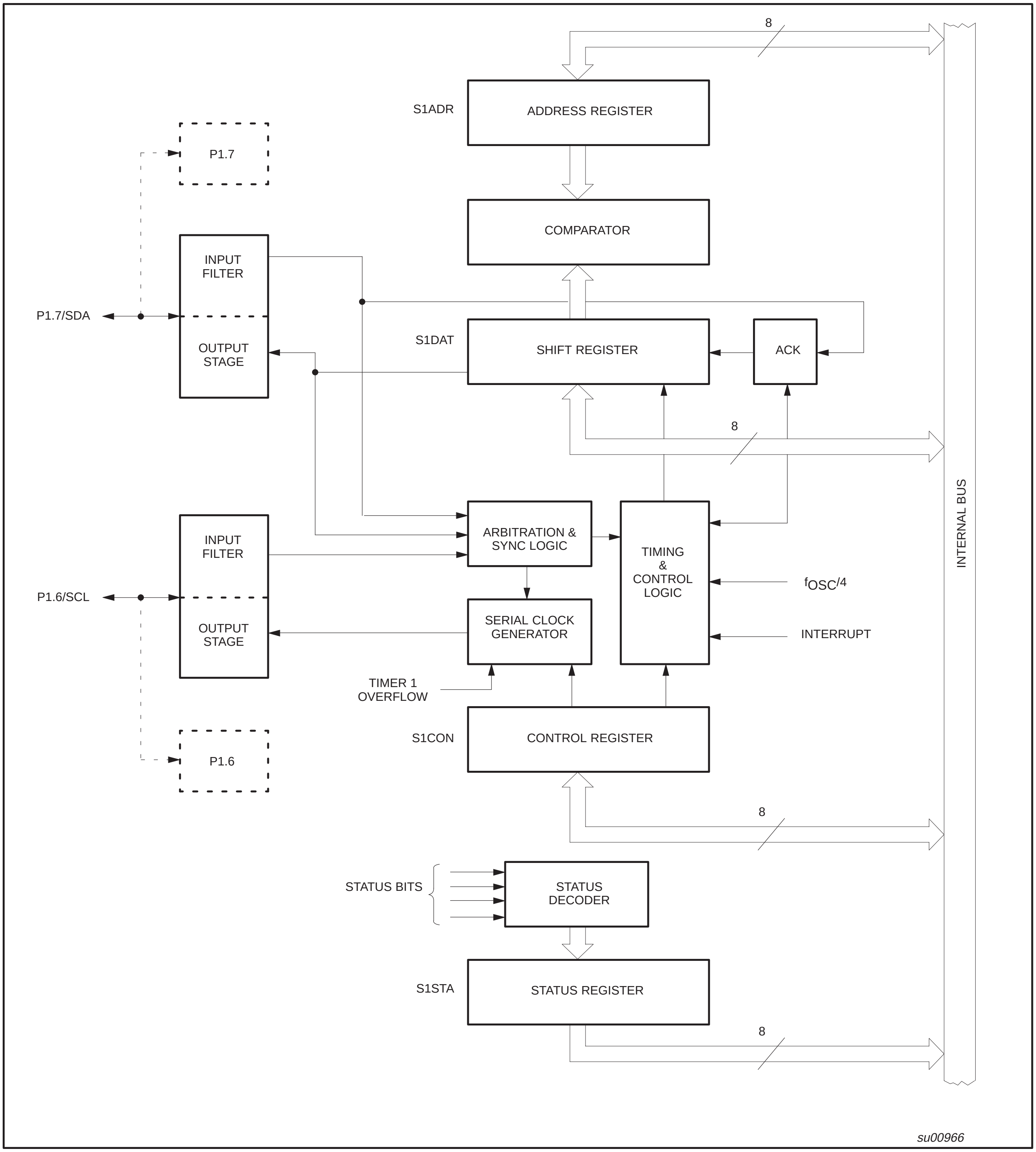

Figure 34. I^{2}C Bus Serial Interface Block Diagram

More Information on SIO1 Operating Modes: The four operating modes are:
- Master Transmitter
- Master Receiver
- Slave Receiver
- Slave Transmitter

Data transfers in each mode of operation are shown in Figures 39–42. These figures contain the following abbreviations:

Abbreviation	Explanation
S	Start condition
SLA	7-bit slave address
R	Read bit (high level at SDA)
W	Write bit (low level at SDA)
A	Acknowledge bit (low level at SDA)
$\overline{A}$	Not acknowledge bit (high level at SDA)
Data	8-bit data byte
P	Stop condition

In Figures 39-42, circles are used to indicate when the serial interrupt flag is set. The numbers in the circles show the status code held in the S1STA register. At these points, a service routine must be executed to continue or complete the serial transfer. These service routines are not critical since the serial transfer is suspended until the serial interrupt flag is cleared by software.

When a serial interrupt routine is entered, the status code in S1STA is used to branch to the appropriate service routine. For each status code, the required software action and details of the following serial transfer are given in Tables 6-10.

Master Transmitter Mode: In the master transmitter mode, a number of data bytes are transmitted to a slave receiver (see Figure 39). Before the master transmitter mode can be entered, S1CON must be initialized as follows:

	7	6	5	4	3	2	1	0
S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
	bit rate	1	0	0	0	X	bit rate	

CR0, CR1, and CR2 define the serial bit rate. ENS1 must be set to logic 1 to enable SIO1. If the AA bit is reset, SIO1 will not acknowledge its own slave address or the general call address in the event of another device becoming master of the bus. In other words, if AA is reset, SIO0 cannot enter a slave mode. STA, STO, and SI must be reset.

The master transmitter mode may now be entered by setting the STA bit using the SETB instruction. The SIO1 logic will now test the I2C bus and generate a start condition as soon as the bus becomes free. When a START condition is transmitted, the serial interrupt flag (SI) is set, and the status code in the status register (S1STA) will be 08H. This status code must be used to vector to an interrupt service routine that loads S1DAT with the slave address and the data direction bit (SLA+W). The SI bit in S1CON must then be reset before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in S1STA are possible. There are 18H, 20H, or 38H for the master mode and also 68H, 78H, or B0H if the slave mode was enabled (AA = logic 1). The appropriate action to be taken for each of these status codes is detailed in Table 6. After a repeated start condition (state 10H). SIO1 may switch to the master receiver mode by loading S1DAT with SLA+R).

Master Receiver Mode: In the master receiver mode, a number of data bytes are received from a slave transmitter (see Figure 40). The transfer is initialized as in the master transmitter mode. When the start condition has been transmitted, the interrupt service routine must load S1DAT with the 7-bit slave address and the data direction bit (SLA+R). The SI bit in S1CON must then be cleared before the serial transfer can continue.

When the slave address and the data direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in S1STA are possible. These are 40H, 48H, or 38H for the master mode and also 68H, 78H, or B0H if the slave mode was enabled (AA = logic 1). The appropriate action to be taken for each of these status codes is detailed in Table 7. ENS1, CR1, and CR0 are not affected by the serial transfer and are not referred to in Table 7. After a repeated start condition (state 10H), SIO1 may switch to the master transmitter mode by loading S1DAT with SLA+W.

Slave Receiver Mode: In the slave receiver mode, a number of data bytes are received from a master transmitter (see Figure 41). To initiate the slave receiver mode, S1ADR and S1CON must be loaded as follows:

	7	6	5	4	3	2	1	0
S1ADR (DBH)	X	X	X	X	X	X	X	GC
	own slave address							

The upper 7 bits are the address to which SIO1 will respond when addressed by a master. If the LSB (GC) is set, SIO1 will respond to the general call address (00H); otherwise it ignores the general call address.

	7	6	5	4	3	2	1	0
S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
	X	1	0	0	0	1	X	X

CR0, CR1, and CR2 do not affect SIO1 in the slave mode. ENS1 must be set to logic 1 to enable SIO1. The AA bit must be set to enable SIO1 to acknowledge its own slave address or the general call address. STA, STO, and SI must be reset.

When S1ADR and S1CON have been initialized, SIO1 waits until it is addressed by its own slave address followed by the data direction bit which must be “0” (W) for SIO1 to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag (I) is set and a valid status code can be read from S1STA. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status codes is detailed in Table 8. The slave receiver mode may also be entered if arbitration is lost while SIO1 is in the master mode (see status 68H and 78H).

If the AA bit is reset during a transfer, SIO1 will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, SIO1 does not respond to its own slave address or a general call address. However, the I2C bus is still monitored and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate SIO1 from the I2C bus.

Table 8. Slave Receiver Mode (Continued)

STATUS CODE (S1STA)	STATUS OF THE I^2C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX	No STDAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		No STDAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		No STDAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		No STDAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

Table 9. Slave Transmitter Mode

STATUS CODE (S1STA)	STATUS OF THE I^2C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
A8H	Own SLA+R has been received; ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received
B0H	Arbitration lost in SLA+R/$\overline{W}$ as master; Own SLA+R has been received, ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received
B8H	Data byte in S1DAT has been transmitted; ACK has been received	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received
C0H	Data byte in S1DAT has been transmitted; NOT ACK has been received	No S1DAT action or	0	0	0	01	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no S1DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		no S1DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no S1DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.
C8H	Last data byte in S1DAT has been transmitted (AA = 0); ACK has been received	No S1DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no S1DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		no S1DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no S1DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

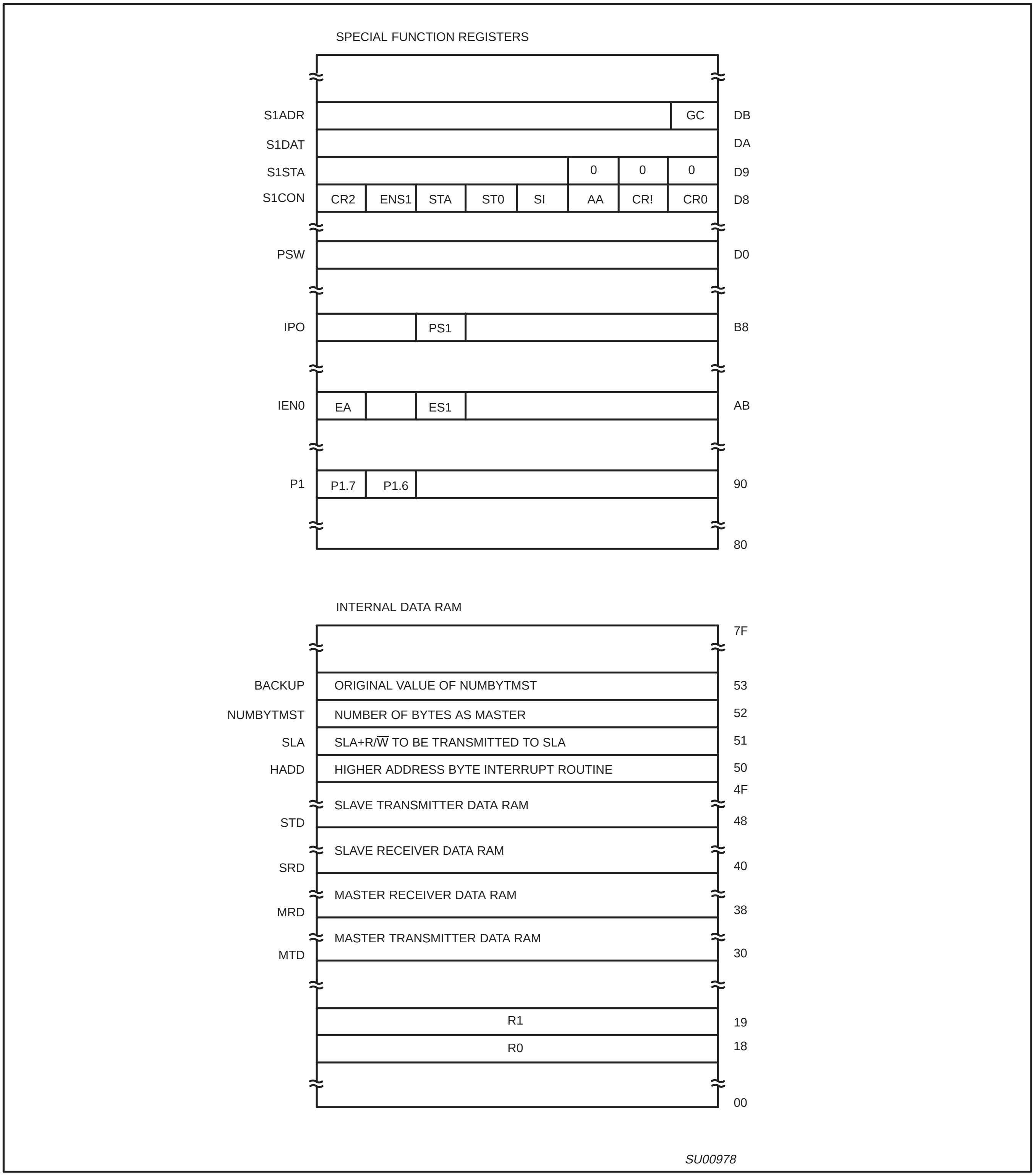

Figure 46. SIO1 Data Memory Map

```
                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  ! STATE    :  20, SLA+W have been transmitted, NOT ACK has been received
                                  ! ACTION   :  Transmit STOP condition.
                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  .sect      mts20
                                  .base      0x120

0120    75D8D5                                  mov    S1CON,#ENS1_NOTSTA_STO_NOTSI_AA_CR0
                                                                             ! set  STO, clr  SI
0123    D0D0                                    pop    psw
0125    32                                      reti

                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  ! STATE    :  28, DATA of S1DAT have been transmitted, ACK received.
                                  ! ACTION   :  If Transmitted DATA is last DATA then transmit a STOP condition,
                                  !             else transmit next DATA.
                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  .sect      mts28
                                  .base      0x128

0128    D55285                                  djnz   NUMBYTMST,NOTLDAT1          ! JMP if NOT last DATA
012B    75D8D5                                  mov    S1CON,#ENS1_NOTSTA_STO_NOTSI_AA_CR0
                                                                             ! clr  SI, set  AA
012E    01B9                                    ajmp   RETmt

                                  .sect      mts28sb
                                  .base      0x0b0
00B0    75D018                    NOTLDAT1:     mov    psw,#SELRB3
00B3    87DA                                    mov    S1DAT,@r1
00B5    75D8C5                    CON:          mov    S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                             ! clr  SI, set   AA
00B8    09                                      inc    r1
00B9    D0D0                      RETmt      :  pop    psw
00BB    32                                      reti
                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  ! STATE    :  30, DATA of S1DAT have been transmitted, NOT ACK received.
                                  ! ACTION   :  Transmit a STOP condition.
                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  .sect      mts30
                                  .base      0x130

0130    75D8D5                                  mov    S1CON,#ENS1_NOTSTA_STO_NOTSI_AA_CR0
                                                                             ! set  STO, clr  SI
0133    D0D0                                    pop    psw
0135    32                                      reti

                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  ! STATE    :  38, Arbitration lost in SLA+W or DATA.
                                  ! ACTION   :  Bus is released, not addressed SLV mode is entered.
                                  !             A new START condition is transmitted when the IIC bus is free again.
                                  !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                                  .sect      mts38
                                  .base      0x138

0138    75D8E5                                  mov    S1CON,#ENS1_STA_NOTSTO_NOTSI_AA_CR0
013B    855352                                  mov    NUMBYTMST,BACKUP
013E    01B9                                    ajmp   RETmt
```

```
                        !*************************************************************************
                        !*************************************************************************
                        ! SLAVE RECEIVER STATE SERVICE ROUTINES
                        !*************************************************************************
                        !*************************************************************************

                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        ! STATE     :  60, Own SLA+W have been received, ACK returned.
                        ! ACTION    :  DATA will be received and ACK returned.
                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        .sect       srs60
                        .base       0x160
0160    75D8C5                              mov   S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                      ! clr  SI, set  AA
0163    75D018                              mov   psw,#SELRB3
0166    01D0                                ajmp  INITSRD
                        .sect       insrd
                        .base       0xd0

00D0    7840            INITSRD:            mov   r0,#SRD
00D2    7908                                mov   r1,#8
00D4    D0D0                                pop   psw
00D6    32                                  reti

                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        ! STATE     :  68, Arbitration lost in SLA and R/W as MST
                        !              Own SLA+W have been received, ACK returned
                        ! ACTION    :  DATA will be received and ACK returned.
                        !              STA is set to restart MST mode after the bus is free again.
                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        .sect       srs68
                        .base       0x168
0168    75D8E5                              mov   S1CON,#ENS1_STA_NOTSTO_NOTSI_AA_CR0
016B    75D018                              mov   psw,#SELRB3
016E    01D0                                ajmp  INITSRD

                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        ! STATE     :  70, General call has been received, ACK returned.
                        ! ACTION    :  DATA will be received and ACK returned.
                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        .sect       srs70
                        .base       0x170
0170    75D8C5                              mov   S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                      ! clr  SI, set  AA
0173    75D018                              mov   psw,#SELRB3             ! Initialize SRD counter
0176    01D0                                ajmp  initsrd

                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        ! STATE     :  78, Arbitration lost in SLA+R/W as MST.
                        !              General call has been received, ACK returned.
                        ! ACTION    :  DATA will be received and ACK returned.
                        !              STA is set to restart MST mode after the bus is free again.
                        !–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––
                        .sect       srs78
                        .base       0x178
0178    75D8E5                              mov   S1CON,#ENS1_STA_NOTSTO_NOTSI_AA_CR0
017B    75D018                              mov   psw,#SELRB3             ! Initialize SRD counter
017E    01D0                                ajmp  INITSRD
```

```
                        !–––––––––––––––––––––––––––––––––––––––––––
                        ! STATE    :  B8, DATA has been transmitted, ACK received.
                        ! ACTION   :  DATA will be transmitted, ACK bit is received.
                        !–––––––––––––––––––––––––––––––––––––––––––
                        .sect       stsb8
                        .base       0x1b8
01B8    75D018                              mov    psw,#SELRB3
01BB    87DA                                mov    S1DAT,@r1
01BD    01F8                                ajmp   SCON

                        .sect       scn
                        .base       0xf8

00F8    75D8C5          SCON:               mov    S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                        ! clr  SI, set  AA
00FB    09                                  inc    r1
00FC    D0D0                                pop    psw
00FE    32                                  reti
                        !–––––––––––––––––––––––––––––––––––––––––––
                        ! STATE    :  C0, DATA has been transmitted, NOT ACK received.
                        ! ACTION   :  Enter not addressed SLV mode.
                        !–––––––––––––––––––––––––––––––––––––––––––
                        .sect       stsc0
                        .base       0x1c0
01C0    75D8C5                              mov    S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                        ! clr  SI, set  AA
01C3    D0D0                                pop    psw
01C5    32                                  reti

                        !–––––––––––––––––––––––––––––––––––––––––––
                        ! STATE    :  C8, Last DATA has been transmitted (AA=0), ACK received.
                        ! ACTION   :  Enter not addressed SLV mode.
                        !–––––––––––––––––––––––––––––––––––––––––––
                        .sect       stsc8
                        .base       0x1c8
01C8    75D8C5                              mov    S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                        ! clr  SI, set  AA
01CB    D0D0                                pop    psw
01CD    32                                  reti


                        !*****************************************************************
                        !*****************************************************************
                        ! END OF SI01 INTERRUPT ROUTINE
                        !*****************************************************************
                        !*****************************************************************
```

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ to V_{SS}	–0.5 to +13	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Input, output DC current on any single I/O pin	5.0	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DEVICE SPECIFICATIONS

TYPE	SUPPLY VOLTAGE (V)		FREQUENCY (MHz)		TEMPERATURE RANGE (°C)
	MIN	MAX	MIN	MAX	
P87C552 SBxx versions	2.7	5.5	0	16	0 to +70
P87C552 SFxx versions	2.7	5.5	0	16	–40 to +85

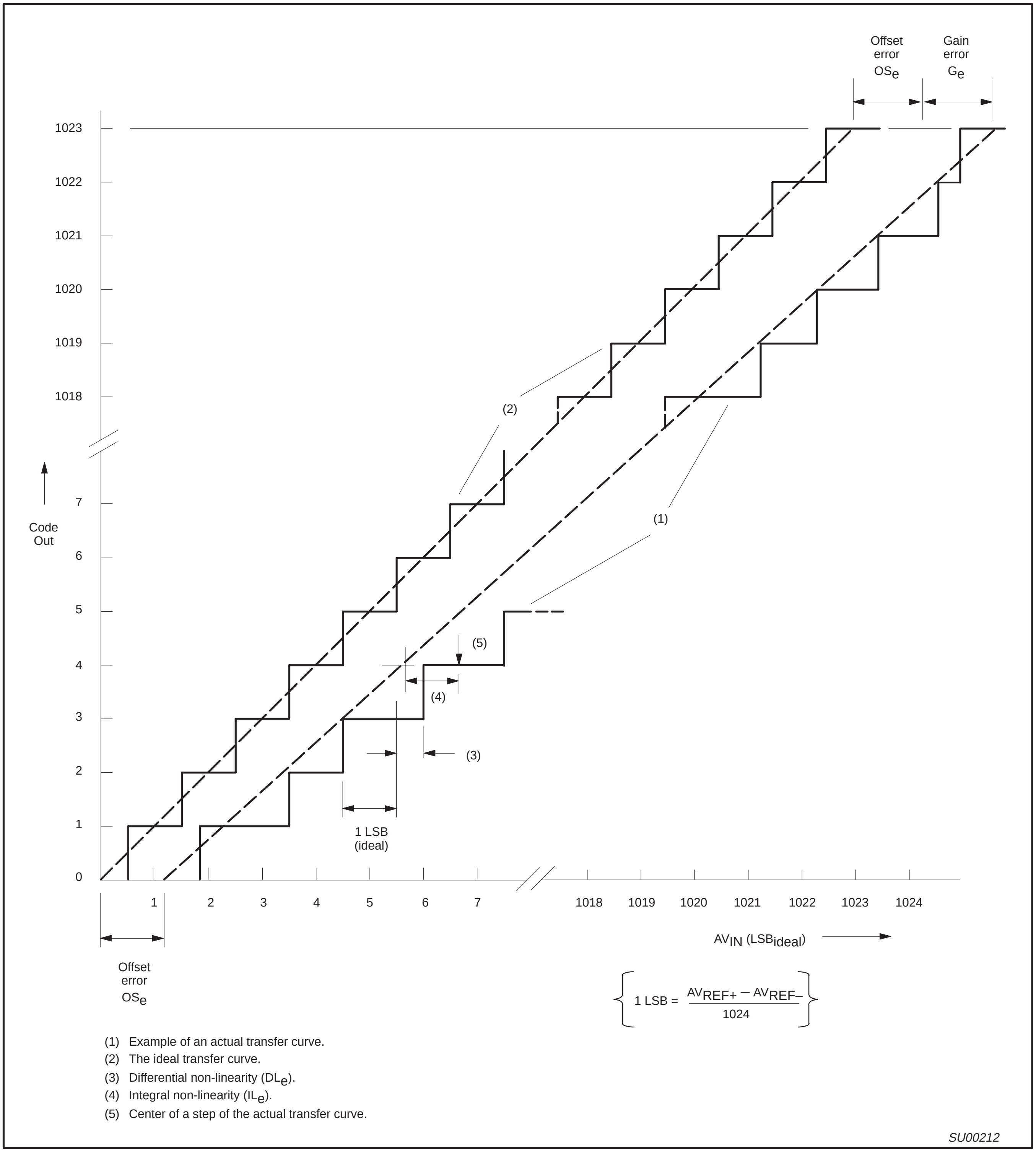

Figure 47. ADC Conversion Characteristic

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	INPUT	OUTPUT
I^2C Interface (Refer to Figure 55)[5]			
$t_{HD;STA}$	START condition hold time	$\geq$ 14 t_{CLCL}	> 4.0µs [1]
t_{LOW}	SCL low time	$\geq$ 16 t_{CLCL}	> 4.7µs [1]
t_{HIGH}	SCL high time	$\geq$ 14 t_{CLCL}	> 4.0µs [1]
t_{RC}	SCL rise time	$\leq$ 1µs	– [2]
t_{FC}	SCL fall time	$\leq$ 0.3µs	< 0.3µs [3]
$t_{SU;DAT1}$	Data set-up time	$\geq$ 250ns	> 20 t_{CLCL} – t_{RD}
$t_{SU;DAT2}$	SDA set-up time (before rep. START cond.)	$\geq$ 250ns	> 1µs [1]
$t_{SU;DAT3}$	SDA set-up time (before STOP cond.)	$\geq$ 250ns	> 8 t_{CLCL}
$t_{HD;DAT}$	Data hold time	$\geq$ 0ns	> 8 t_{CLCL} – t_{FC}
$t_{SU;STA}$	Repeated START set-up time	$\geq$ 14 t_{CLCL}	> 4.7µs [1]
$t_{SU;STO}$	STOP condition set-up time	$\geq$ 14 t_{CLCL}	> 4.0µs [1]
t_{BUF}	Bus free time	$\geq$ 14 t_{CLCL}	> 4.7µs [1]
t_{RD}	SDA rise time	$\leq$ 1µs	– [2]
t_{FD}	SDA fall time	$\leq$ 0.3µs	< 0.3µs [3]

NOTES:
1. At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3 t_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400pF.
4. $t_{CLCL} = 1/f_{OSC}$ = one oscillator clock period at pin XTAL1. For 62ns (42s) < t_{CLCL} < 285ns (16MHz > f_{OSC} > 3.5MHz) the SI01 interface meets the I^2C-bus specification for bit-rates up to 100 kbit/s.
5. These values are guaranteed but not 100% production tested.

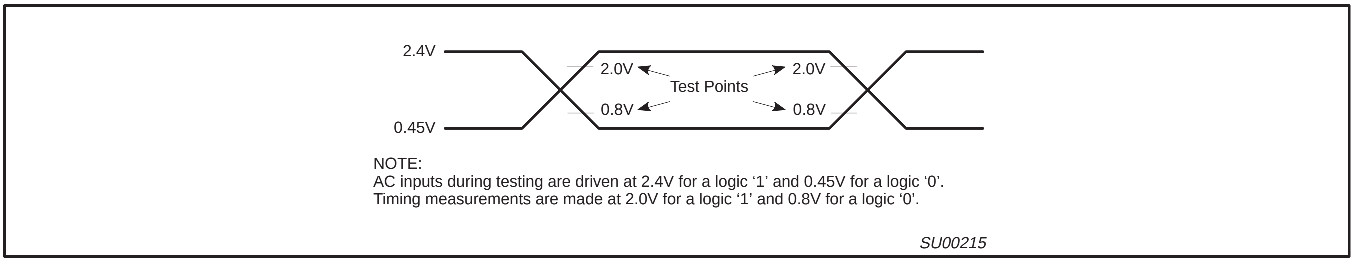

Figure 53. AC Testing Input/Output

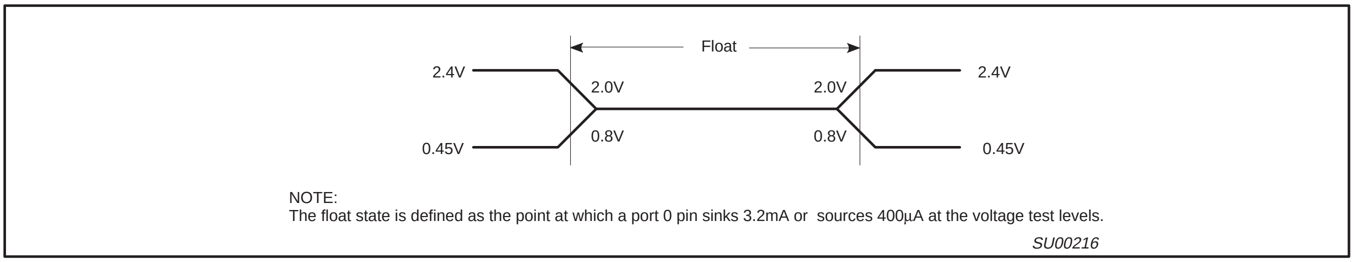

Figure 54. AC Testing Input, Float Waveform

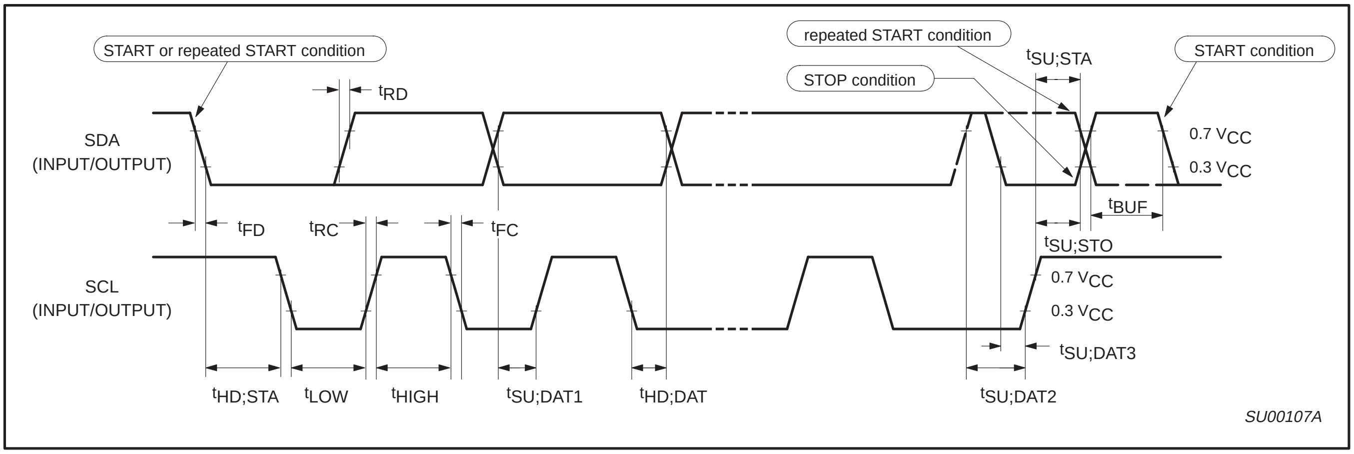

Figure 55. Timing SIO1 (I^2C) Interface

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II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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