Lattice Semiconductor Corporation - <u>LFE5U-12F-6MG285I Datasheet</u>



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3000
Number of Logic Elements/Cells	12000
Total RAM Bits	589824
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-12f-6mg285i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





Figure 2.4. Conned	tivity Supporting L	LUT5, LUT6,	LUT7, and LUT8
--------------------	---------------------	-------------	----------------

Table 2.2	. Slice	Signal	Descri	ptions
-----------	---------	--------	--------	--------

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output ¹

Notes:

2. Requires two adjacent PFUs.

^{1.} See Figure 2.3 on page 15 for connection details.



2.3. Routing

There are many resources provided in the ECP5/ECP5-5G devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The ECP5/ECP5-5G family has an enhanced routing architecture that produces a compact design. The Diamond design software tool suites take the output of the synthesis tool and places and routes the design.

2.4. Clocking Structure

ECP5/ECP5-5G clocking structure consists of clock synthesis blocks (sysCLOCK PLL); balanced clock tree networks (PCLK and ECLK trees); and efficient clock logic modules (CLOCK DIVIDER and Dynamic Clock Select (DCS), Dynamic Clock Control (DCC) and DLL). All of these functions are described below.

2.4.1. sysCLOCK PLL

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the ECP5/ECP5-5G family support two to four full-featured General Purpose PLLs. The sysCLOCK PLLs provide the ability to synthesize clock frequencies.

The architecture of the PLL is shown in Figure 2.5. A description of the PLL functionality follows.

CLKI is the reference frequency input to the PLL and its source can come from two different external CLK inputs or from internal routing. A non-glitchless 2-to-1 input multiplexor is provided to dynamically select between two different external reference clock sources. The CLKI input feeds into the input Clock Divider block.

CLKFB is the feedback signal to the PLL which can come from internal feedback path, routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLL has four clock outputs CLKOP, CLKOS, CLKOS2 and CLKOS3. Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the primary clock network. Only CLKOP and CLKOS outputs can go to the edge clock network.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the PHASESEL, PHASEDIR, PHASESTEP, and PHASELOADREG ports.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected.







Table 2.4 provides a	description of	the signals	in the PLL blocks.
----------------------	----------------	-------------	--------------------

Signal	Туре	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

Table 2.4. PLL Blocks Signal Descriptions

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.





Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).



In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	Ι

*Note: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.



ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

• Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

Bank 4 I/O only exists in the LFE5-85 device.

Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

The top and bottom side pads can be identified by the Lattice Diamond tool.

Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).



When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)	
2.4	
4.8	
9.7	
19.4	
38.8	
62	

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.



3.7. Hot Socketing Requirements

Table 3.6. Hot Socketing Requirements

Description	Min	Тур	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	_	_	8	mA
Input current per HDIN pin when device power supply is off, inputs driven ^{1, 2}	_	_	15	mA
Current per HDIN pin when device power ramps up, input driven ³	—	—	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up ⁴	_	_	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, no external AC coupling.

2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.

- Device power supplies are ramping up (V_{CCA} and V_{CCAUX}), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, internal AC coupling.
- 4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to V_{CCHTX} by the far end receiver termination of 50 Ω single ended.

3.8. ESD Performance

Refer to the ECP5 and ECP5-5G Product Family Qualification Summary for complete qualification data, including ESD performance.

3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Тур	Max	Unit
I _{IL} , I _{IH} ^{1, 4}	Input or I/O Low Leakage	$0 \leq V_{IN} \leq V_{CCIO}$	—	_	10	μA
I _{IH} ^{1, 3}	Input or I/O High Leakage	$V_{CCIO} < V_{IN} \le V_{IH(MAX)}$	—	_	100	μA
1	I/O Active Pull-up Current, sustaining logic HIGH state	$0.7 \ V_{CCIO} \! \leq \! V_{IN} \! \leq \! V_{CCIO}$	-30	_	_	μA
1PU	I/O Active Pull-up Current, pulling down from logic HIGH state	$0 \leq V_{\text{IN}} \leq 0.7 \ V_{\text{CCIO}}$	_	_	-150	μA
las	I/O Active Pull-down Current, sustaining logic LOW state	$0 \le V_{IN} \le V_{IL}$ (MAX)	30	_	_	μΑ
טקו	I/O Active Pull-down Current, pulling up from logic LOW state	$0 \leq V_{\text{IN}} \leq V_{\text{CCIO}}$	—	—	150	μΑ
C1	I/O Capacitance ²	$\begin{split} V_{CCIO} &= 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V}, \\ V_{CC} &= 1.2 \text{ V}, \text{ V}_{IO} &= 0 \text{ to } ^{V_{IH(MAX)}} \end{split}$	_	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V}, \\ V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{\text{IH}(\text{MAX})}$	_	5	7	pf
	Hysteresis for Single-Ended	V _{CCIO} = 3.3 V	—	300	—	mV
V HYST	Inputs	V _{CCI0} = 2.5 V	_	250	_	mV

Table 3.7. DC Electrical Characteristics

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25 °C, f = 1.0 MHz.

- 3. Applicable to general purpose I/Os in top and bottom banks.
- 4. When used as V_{REF} , maximum leakage= 25 μ A.



3.14. sysl/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.13. LVDS

Parameter	Description	Test Conditions	Min	Тур	Max	Unit
V _{INP} , V _{INM}	Input Voltage	-	0	—	2.4	V
V _{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V _{THD}	Differential Input Threshold	Difference between the two Inputs	±100	—	—	mV
I _{IN}	Input Current	Power On or Power Off	_	—	±10	μA
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100 \Omega$	—	1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100 \Omega$	0.9 V	1.03	_	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V _{OD} Between High and Low	_	—	—	50	mV
V _{os}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, $R_T = 100 \Omega$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I _{SAB}	Output Short Circuit Current	$V_{OD} = 0$ V Driver outputs shorted to each other	_	_	12	mA

Note: On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5$ V or 3.3 V.

3.14.2. **SSTLD**

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO} . The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.



3.14.5. BLVDS25

The ECP5/ECP5-5G devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.



Figure 3.2. BLVDS25 Multi-point Output Example

Over recommended operating conditions.

Parameter	Description	Тур	11	
	Description	Zo = 45 Ω	Zo = 90 Ω	Unit
V _{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (±1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (±1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (±1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage	1.38	1.48	V
V _{OL}	Output Low Voltage	1.12	1.02	V
V _{OD}	Output Differential Voltage	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

Table 3.15. BLVDS25 DC Conditions

Note: For input buffer, see LVDS Table 3.13 on page 55.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.

All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

Table 3.18. Input to SLVS

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.



Figure 3.5. SLVS Interface

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.

All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.





Figure 3.11. Receiver DDRX71_RX Waveforms



Figure 3.12. Transmitter DDRX71_TX Waveforms

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.



3.20. SERDES High-Speed Data Transmitter

Table 3.24. Serial Output Timing and Levels

Symbol	Description	Min	Тур	Max	Unit
V _{TX-DIFF-PP}	Peak-Peak Differential voltage on selected amplitude ^{1, 2}	-25%	—	25%	mV, p-p
V _{TX-CM-DC}	Output common mode voltage	—	V _{CCHTX} / 2	—	mV, p-p
T _{TX-R}	Rise time (20% to 80%)	50	—	—	ps
T _{TX-F}	Fall time (80% to 20%)	50	—	—	ps
T _{TX-CM-AC-P}	RMS AC peak common-mode output voltage	—	—	20	mV
7	Single ended output impedance for 50/75 $\boldsymbol{\Omega}$	-20%	50/75	20%	Ω
ZTX_SE	Single ended output impedance for 6K $\boldsymbol{\Omega}$	-25%	6K	25%	Ω
RL _{TX_DIFF}	Differential return loss (with package included) ³	—	—	-10	dB
RL _{TX_COM}	Common mode return loss (with package included) 3	—	—	-6	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at V_{CCHTx} \pm 5\%.

2. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for settings of Tx amplitude.

3. Return los = -10 dB (differential), -6 dB (common mode) for 100 MHz \leq f <= 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

Table 3.25. Channel Output Jitter

Description	Frequency	Min	Тур	Max	Unit
Deterministic	5 Gb/s	—	—	TBD	UI, p-p
Random	5 Gb/s	—	—	TBD	UI, p-p
Total	5 Gb/s	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	_	_	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	_	_	0.24	UI, p-p

Notes:

1. Values are measured with PRBS 2⁷-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

2. For ECP5-5G family devices only.



3.25. PCI Express Electrical and Timing Characteristics

3.25.1. PCIe (2.5 Gb/s) AC and DC Characteristics

Over recommended operating conditions.

Table 3.30. PCIe (2.5 Gb/s)

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
Transmit ¹						
UI	Unit interval	_	399.88	400	400.12	ps
V _{TX-DIFF_P-P}	Differential peak-to-peak output	-	0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio	_	-3	-3.5	-4	dB
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage	_	_	_	20	mV
V _{TX-RCV-DETECT}	Amount of voltage change allowed during receiver detection	_	_	_	600	mV
V _{TX-CM-DC}	Tx DC common mode voltage	_	0	-	V _{CCHTX}	V
I _{TX-SHORT}	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	_	_	90	mA
Z _{TX-DIFF-DC}	Differential output impedance	_	80	100	120	Ω
RL _{TX-DIFF}	Differential return loss	_	10	_	—	dB
RL _{TX-CM}	Common mode return loss	_	6.0	_	—	dB
T _{TX-RISE}	Tx output rise time	20% to 80%	0.125	_	—	UI
T _{TX-FALL}	Tx output fall time	20% to 80%	0.125	_	—	UI
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link	_	_	_	1.3	ns
T _{TX-EYE}	Transmitter eye width	—	0.75	_	—	UI
T _{TX-EYE-MEDIAN-TO-MAX-} JITTER	Maximum time between jitter median and maximum deviation from median	-	-	-	0.125	UI
Receive ^{1, 2}						
UI	Unit Interval	_	399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage	_	0.34 ³	_	1.2	v
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage	_	65	—	340 ³	mV
V _{RX-CM-AC_P}	RMS AC peak common-mode input voltage	_	_	_	150	mV
Z _{RX-DIFF-DC}	DC differential input impedance	_	80	100	120	Ω
Z _{RX-DC}	DC input impedance	_	40	50	60	Ω
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance	_	200K	—	-	Ω
RL _{RX-DIFF}	Differential return loss	-	10	—	-	dB
RL _{RX-CM}	Common mode return loss	—	6.0	—	_	dB

Notes:

- 1. Values are measured at 2.5 Gb/s.
- 2. Measured with external AC-coupling on the receiver.
- 3. Not in compliance with PCI Express 1.1 standard.

All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.39. Transmit

Symbol	Description Test Conditions Min		Тур	Max	Unit	
BR _{SDO}	Serial data rate	—	270	—	2975	Mb/s
T _{JALIGNMENT} ²	Serial output jitter, alignment	270 Mb/s ⁶	—	0.2	UI	
T _{JALIGNMENT} ²	Serial output jitter, alignment	1485 Mb/s	—	—	0.2	UI
T _{JALIGNMENT} ^{1, 2}	Serial output jitter, alignment	2970 Mb/s	—	—	0.3	UI
T _{JTIMING}	Serial output jitter, timing	270 Mb/s ⁶	—	—	0.2	UI
T _{JTIMING}	Serial output jitter, timing	1485 Mb/s	—	—	1	UI
T _{JTIMING}	Serial output jitter, timing	2970 Mb/s	—	—	2	UI

Notes:

1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.

- 2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
- 3. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice SERDES device configured to 50Ω output impedance connecting to the external cable driver with differential signaling.
- 4. The cable driver drives: RL=75 Ω , AC-coupled at 270, 1485, or 2970 Mb/s.
- 5. All LFE5UM/LFE5UM5G devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.
- 6. 270 Mb/s is supported with Rate Divider only.

Table 3.40. Receive

Symbol	Description	Test Conditions Min		Тур	Max	Unit
BR _{SDI}	Serial input data rate	—	270		2970	Mb/s

Table 3.41. Reference Clock

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
F _{VCLK}	Video output clock frequency	—	54	_	148.5	MHz
DCv	Duty cycle, video clock	—	45	50	55	%

Note: SD-SDI (270 Mb/s) is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.





Figure 3.23. JTAG Port Timing Waveforms

3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.



*CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards



4. Pinout Information

4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[L/R] [Group Number]_[A/B/C/D]	1/0	 [L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIO A and B are grouped as a pair, and PIO C and D are group as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer. Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω.
P[T/B][Group Number]_[A/B]	I/O	 [T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer. PIO A/B forms a pair of emulated differential output buffer.
GSRN		Global RESET signal (active low). Any I/O pin can be GSRN.
NC	_	No connect.
RESERVED	_	This pin is reserved and should not be connected to anything on the board.
GND	_	Ground. Dedicated pins.
V _{cc}	_	Power supply pins for core logic. Dedicated pins. V _{CC} = 1.1 V (ECP5), 1.2 V (ECP5UM5G)
Vccaux	-	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. $V_{CCAUX} = 2.5 V$.
V _{CCIOx}	_	Dedicated power supply pins for I/O bank x. V_{CCIO8} is used for configuration and JTAG.
VREF1_x	-	Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as VREF1 input. When not used, they may be used as I/O pins.
PLL, DLL and Clock Functions	1	
[LOC][_GPLL[T, C]_IN	I	General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not configured as GPLL input pads, they can be used as general purpose I/O pins.
GR_PCLK[Bank][num]	I	General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to ECP5 sysClock PLL/DLL Design and Usage Guide (TN1263). These pins are shared I/O pins. When not configured as GR pins, they can be used as general purpose I/O pins.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/ O pins. When not configured as PCLK pins, they can be used as general purpose I/O pins.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.

All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-85F-6BG756I	-6	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-7BG756I	-7	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	No
LFE5UM-25F-6MG285I	-6	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-7MG285I	-7	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-6BG381I	-6	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-7BG381I	-7	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-45F-6MG285I	-6	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-7MG285I	-7	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-6BG381I	-6	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-7BG381I	-7	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-6BG554I	-6	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-7BG554I	-7	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-85F-6MG285I	-6	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-7MG285I	-7	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-6BG381I	-6	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-7BG381I	-7	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-6BG554I	-6	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-7BG554I	-7	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-6BG756I	-6	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-7BG756I	-7	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	Yes
LFE5UM5G-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM5G-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM5G-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM5G-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM5G-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM5G-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM5G-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM5G-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM5G-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	Yes



Revision History

Date	Version	Section	Change Summary
March 2018	1.9	All	Updated formatting and page referencing.
		General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-45.
		Architecture	Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support. Updated footnote #1.
		DC and Switching	Updated Table 3.2. Recommended Operating Conditions.
		Characteristics	Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics.
			Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby).
			Updated Table 3.11. sysl/O Recommended Operating Conditions.
			Updated Table 3.12. Single-Ended DC Characteristics.
			Updated Table 3.13. LVDS.
			Updated Table 3.14. LVDS25E DC Conditions.
			Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed.
			Updated Table 3.28. Receiver Total Jitter Tolerance Specification.
			Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics.
			Updated header name of section 3.29 Gigabit Ethernet/(SMIII(1,25Gbps)/CPRLLVE 12 Electrical and Timing
			Characteristics
		Pinout Information	Updated table in section 4.3.2 LFE5U.
		Ordering Information	Added table rows in 5.2.1 Commercial.
			Added table rows in 5.2.2 Industrial.
		Supplemental Information	Updated For Further Information section.
November 2017	1.8	General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-12 and LFE5U-25.



(Continued)

Date	Version	Section	Change Summary
April 2017	1.7	All	Changed document number from DS1044 to FPGA-DS-02012.
		General Description	Updated Features section. Changed "1.1 V core power supply" to "1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G".
		Architecture	Updated Overview section. Change "The ECP5/ECP5-5G devices use 1.1 V as their core voltage" to "The ECP5 devices use 1.1V, ECP5UM5G devices use 1.2V as their core voltage"
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions Added ECP5-5G on VCC to be 1.2V +/- 5% Added ECP5-5G on VCCA to be 1.2V +/- 3% Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) Changed "Core Power Supply Current" for ICC on LFE5UM5G devices Changed "SERDES Power Supply Current (Per Dual)" for ICCA on LFE5UM5G devices Updated Table 3.20. Register-to-Register Performance. Remove "(DDR/SDR)" from DSP Function Changed DSP functions to 225 MHz
		Pinout Information	Update Section 4.1 Signal Description. Revised Vcc Description to "Power supply pins for core logic. Dedicated pins. VCC = 1.1 V (ECP5), 1.2 V (ECP5UM5G)"
February 2016	1.6	All	Changed document status from Preliminary to Final.
February 2016		General Description	Updated Features section. Changed "24K to 84K LUTs" to "12K to 84K LUTs". Added LFE5U-12 column to Table 1.1. ECP5 and ECP5-5G Family Selection Guide.
		DC and Switching Characteristics	Updated Power up Sequence section. Identified typical ICC current for specific devices in Table 3.8. ECP5/ECP5-5G Supply Current (Standby). Updated values in Table 3.9. ECP5. Updated values in Table 3.10. ECP5-5G. Added values to -8 Timing column of Table 3.19. Pin-to-Pin Performance. Added values to -8 Timing column of Table 3.20. Register-to-Register Performance. Changed LFE5-45 to All Devices in Table 3.22. ECP5/ECP5-5G External Switching Characteristics. Added table notes to Table 3.31. PCIe (5 Gb/s). Added table note to Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics.
		Pinout Information	Added LFE5U-12 column to the table in LFE5U section.
		Ordering Information	Updated LFE5U in ECP5/ECP5-5G Part Number Description section: added 12 F = 12K LUTs to Logic Capacity. Added LFE5U-12F information to Ordering Part Numbers section.