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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

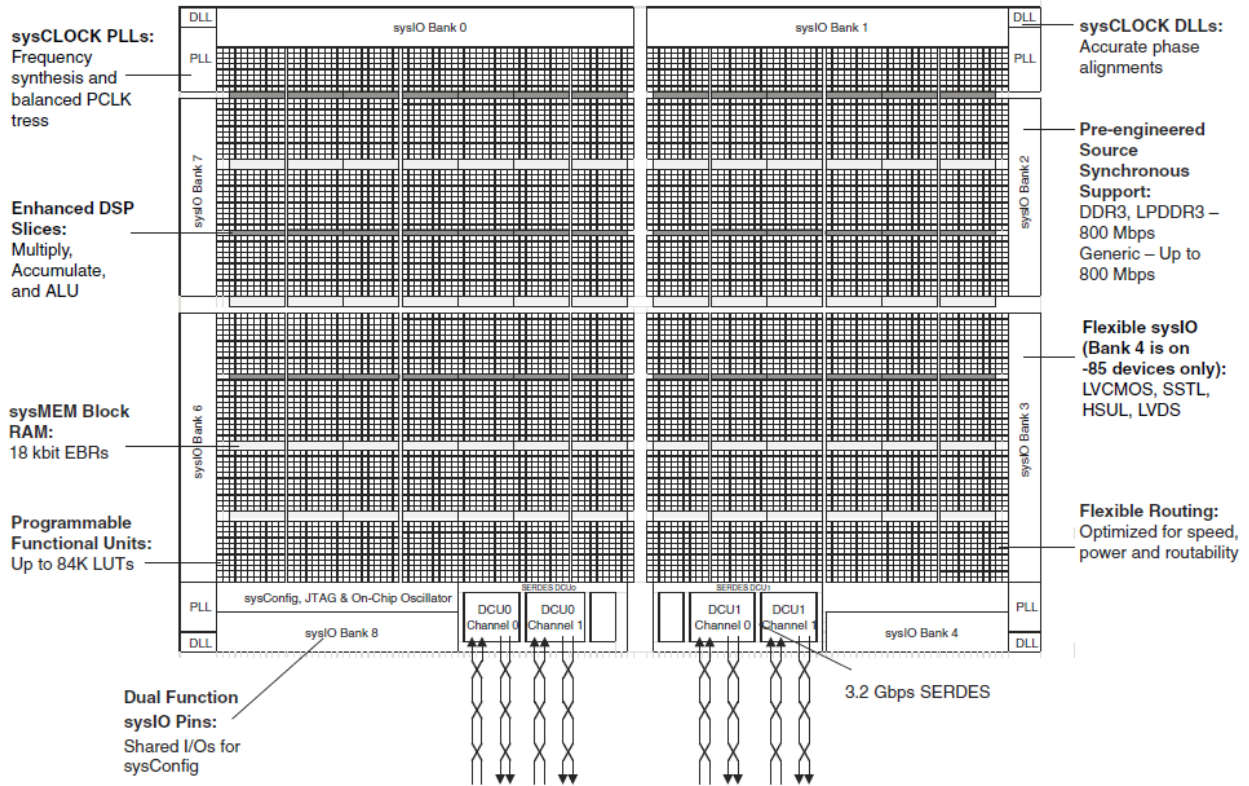
Details

Product Status	Active
Number of LABs/CLBs	3000
Number of Logic Elements/Cells	12000
Total RAM Bits	589824
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-12f-7bg381c

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay-Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLL	Phase-Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SERDES	Serializer/Deserializer
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing



Note: There is no Bank 4 in -25 and -45 devices.
There are no PLL and DLL on the top corners in -25 devices.

Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.

A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. [Table 2.3](#) lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#).

2.3. Routing

There are many resources provided in the ECP5/ECP5-5G devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments. The ECP5/ECP5-5G family has an enhanced routing architecture that produces a compact design. The Diamond design software tool suites take the output of the synthesis tool and places and routes the design.

2.4. Clocking Structure

ECP5/ECP5-5G clocking structure consists of clock synthesis blocks (sysCLOCK PLL); balanced clock tree networks (PCLK and ECLK trees); and efficient clock logic modules (CLOCK DIVIDER and Dynamic Clock Select (DCS), Dynamic Clock Control (DCC) and DLL). All of these functions are described below.

2.4.1. sysCLOCK PLL

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the ECP5/ECP5-5G family support two to four full-featured General Purpose PLLs. The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The architecture of the PLL is shown in Figure 2.5. A description of the PLL functionality follows.

CLKI is the reference frequency input to the PLL and its source can come from two different external CLK inputs or from internal routing. A non-glitchless 2-to-1 input multiplexer is provided to dynamically select between two different external reference clock sources. The CLKI input feeds into the input Clock Divider block.

CLKFB is the feedback signal to the PLL which can come from internal feedback path, routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLL has four clock outputs CLKOP, CLKOS, CLKOS2 and CLKOS3. Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the primary clock network. Only CLKOP and CLKOS outputs can go to the edge clock network.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the PHASESEL, PHASEDIR, PHASESTEP, and PHASELOADREG ports.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected.

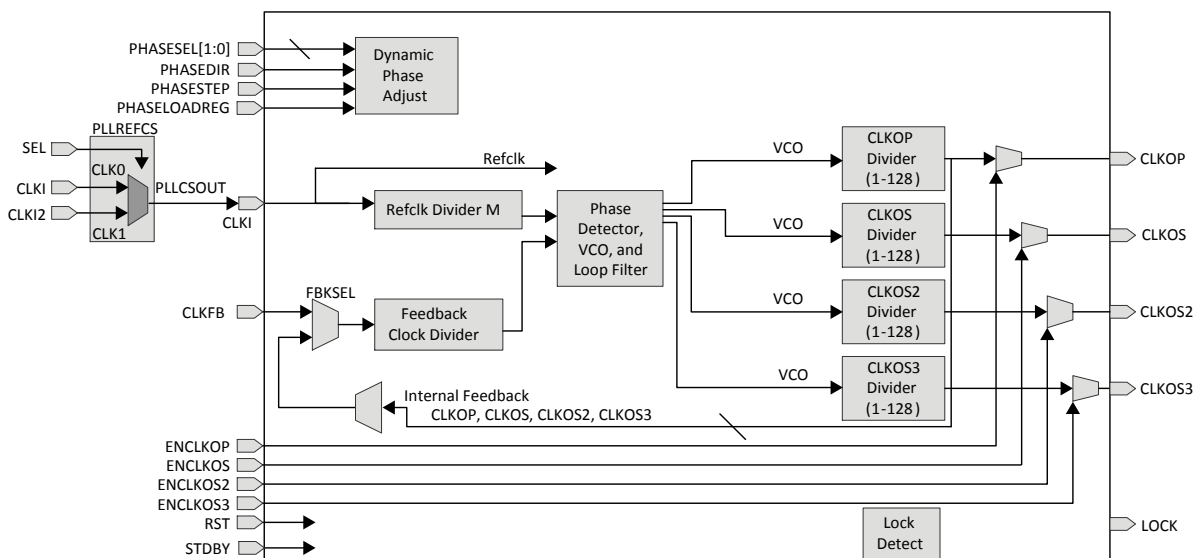


Figure 2.5. General Purpose PLL Diagram

2.7. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. [Figure 2.10](#) shows DDRDLL functional diagram.

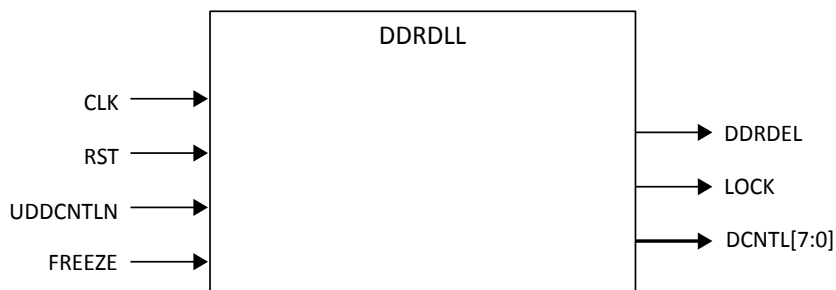


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. [Figure 2.11](#) shows the DDRDLL and the slave DLLs on the top level view.

Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36
True Dual Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36
Pseudo Dual Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36

2.8.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.8.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.8.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.8.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- **Read-Before-Write** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

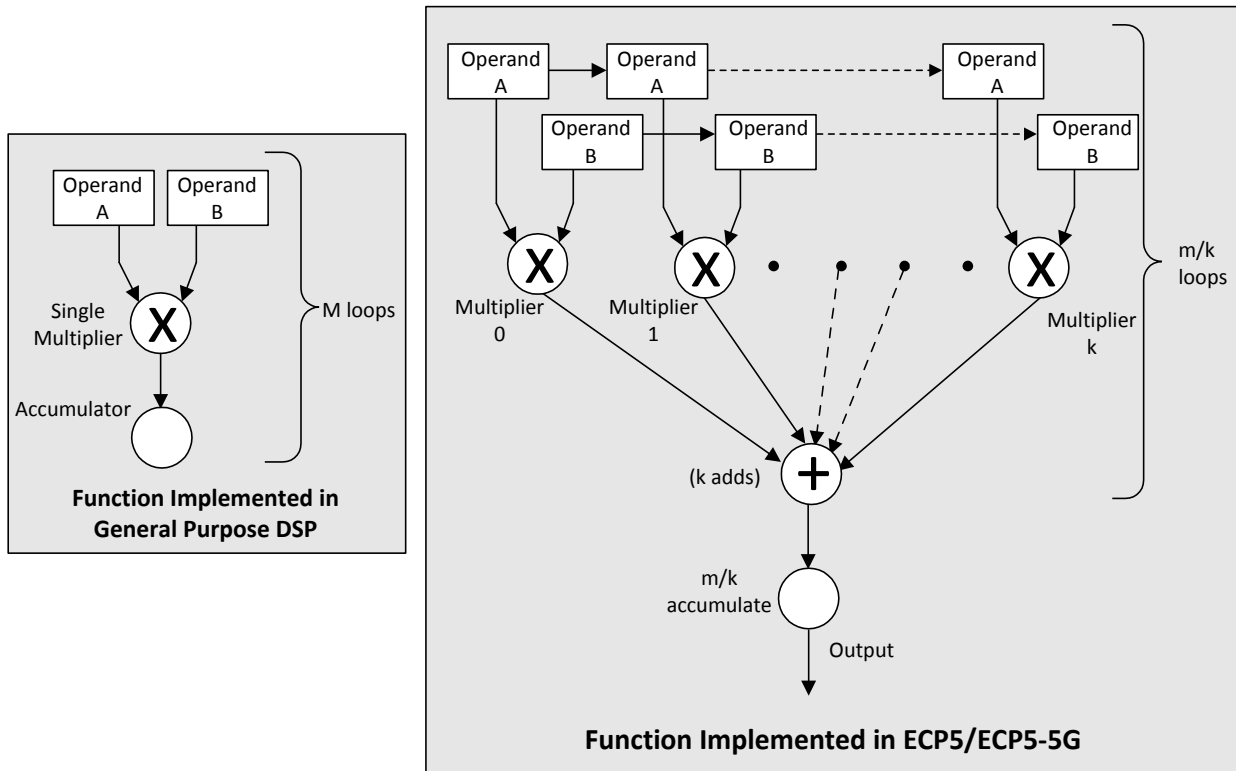


Figure 2.13. Comparison of General DSP and ECP5/ECP5-5G Approaches

2.9.2. sysDSP Slice Architecture Features

The ECP5/ECP5-5G sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The ECP5/ECP5-5G sysDSP Slice supports many functions that include the following:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
 - Odd mode – Filter with Odd number of taps
 - Even mode – Filter with Even number of taps
 - Two dimensional (2D) symmetry mode – supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture
- Fully cascadable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)
- Multiply (36x36 by cascading across two sysDSP slices)
- Multiply Accumulate (supports one 18x36 multiplier result accumulation or two 18x18 multiplier result accumulation)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
 - Odd mode – Filter with Odd number of taps
 - Even mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
 - 3*3 and 3*5 – Internal DSP Slice support

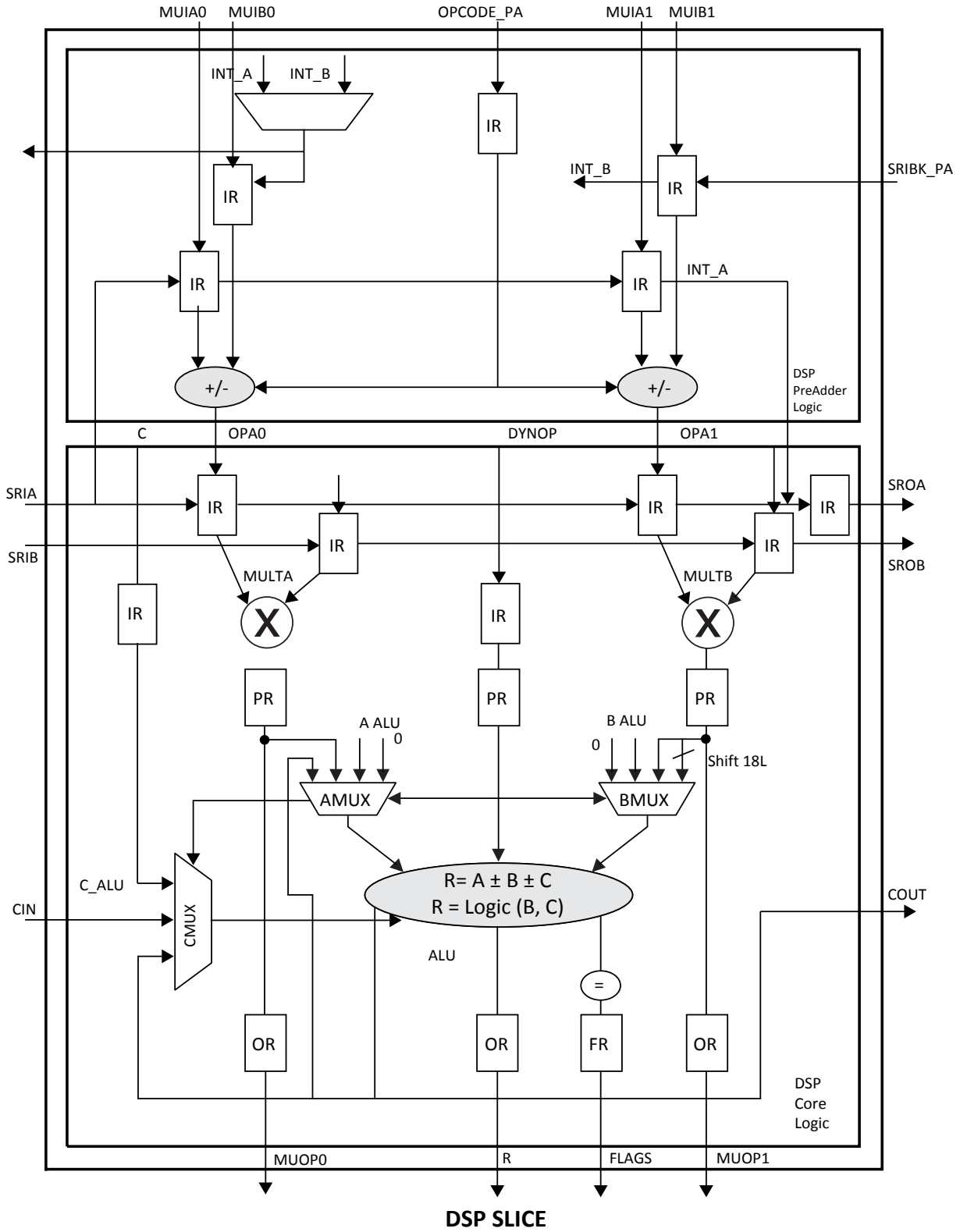


Figure 2.15. Detailed sysDSP Slice Diagram

In [Figure 2.15](#), note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

[Table 2.7](#) shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note:** One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.

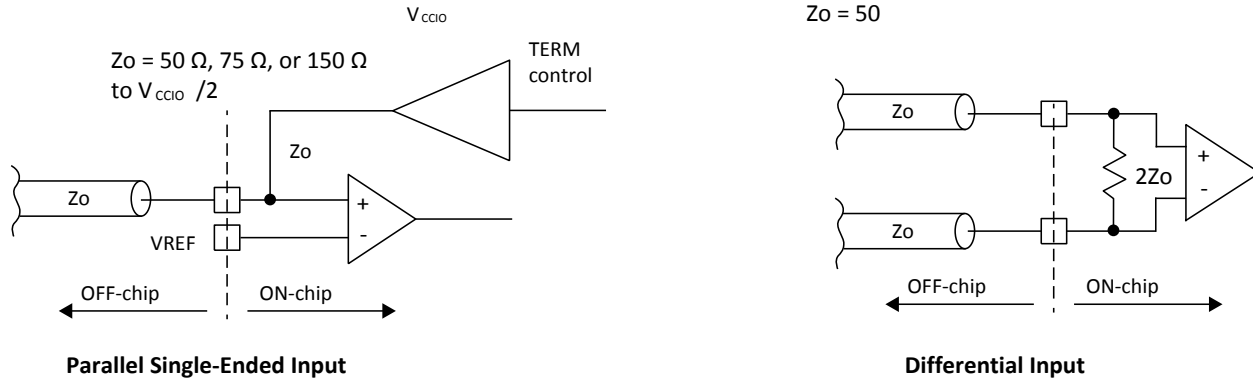


Figure 2.26. On-Chip Termination

See [Table 2.12](#) for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2^*$	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Notes:**

TERMINATE to $V_{CCIO}/2$ (Single-Ended) and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance $\pm 20\%$.

Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for on-chip termination usage and value ranges.

2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the [Hot Socketing Specifications](#) section on page 48.

2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. [Figure 2.27](#) shows the position of the dual blocks for the LFE5-85. [Table 2.13](#) shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to [LatticeECP3, ECP5 and ECP5-5G Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide \(TN1184\)](#).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. [Table 2.16](#) lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#) and [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.5	1.32	V
V _{CCA}	Supply Voltage	-0.5	1.32	V
V _{CCAUX} , V _{CCAUXA}	Supply Voltage	-0.5	2.75	V
V _{CCIO}	Supply Voltage	-0.5	3.63	V
—	Input or I/O Transient Voltage Applied	-0.5	3.63	V
V _{CCHRX} , V _{CCHTX}	SERDES RX/TX Buffer Supply Voltages	-0.5	1.32	V
—	Voltage Applied on SERDES Pins	-0.5	1.80	V
T _A	Storage Temperature (Ambient)	-65	150	°C
T _J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V _{CC} ²	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
V _{CCAUX} ^{2,4}	Auxiliary Supply Voltage	—	2.375	2.625	V
V _{CCIO} ^{2,3}	I/O Driver Supply Voltage	—	1.14	3.465	V
V _{REF} ¹	Input Reference Voltage	—	0.5	1.0	V
t _{JCOM}	Junction Temperature, Commercial Operation	—	0	85	°C
t _{JIND}	Junction Temperature, Industrial Operation	—	-40	100	°C
SERDES External Power Supply⁵					
V _{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V _{CCAUXA}	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
V _{CCHRX} ⁶	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V _{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in [Table 3.4](#) on page 48.
4. V_{CCAUX} ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
5. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to V_{cm} if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

Table 3.20. Register-to-Register Performance

Function	-8 Timing	Unit
Basic Functions		
16-Bit Decoder	441	MHz
32-Bit Decoder	441	MHz
64-Bit Decoder	332	MHz
4:1 Mux	441	MHz
8:1 Mux	441	MHz
16:1 Mux	441	MHz
32:1 Mux	441	MHz
8-Bit Adder	441	MHz
16-Bit Adder	441	MHz
64-Bit Adder	441	MHz
16-Bit Counter	384	MHz
32-Bit Counter	317	MHz
64-Bit Counter	263	MHz
64-Bit Accumulator	288	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	214	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	441	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	441	MHz
DSP Functions		
9 x 9 Multiplier (All Registers)	225	MHz
18 x 18 Multiplier (All Registers)	225	MHz
36 x 36 Multiplier (All Registers)	225	MHz
18 x 18 Multiply-Add/Sub (All Registers)	225	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	225	MHz

Notes:

1. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks									
Primary Clock									
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
Edge Clock									
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
t_{SKEW_EDGE}	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
Generic SDR Input									
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL									
t_{CO}	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
t_H	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL									
t_{COPLL}	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
t_{SU_DEPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns

3.25. PCI Express Electrical and Timing Characteristics

3.25.1. PCIe (2.5 Gb/s) AC and DC Characteristics

Over recommended operating conditions.

Table 3.30. PCIe (2.5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit¹						
UI	Unit interval	—	399.88	400	400.12	ps
V _{TX-DIFF_P-P}	Differential peak-to-peak output	—	0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio	—	-3	-3.5	-4	dB
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage	—	—	—	20	mV
V _{TX-RCV-DETECT}	Amount of voltage change allowed during receiver detection	—	—	—	600	mV
V _{TX-CM-DC}	Tx DC common mode voltage	—	0	—	V _{CCHTX}	V
I _{TX-SHORT}	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	—	—	90	mA
Z _{TX-DIFF-DC}	Differential output impedance	—	80	100	120	Ω
RL _{TX-DIFF}	Differential return loss	—	10	—	—	dB
RL _{TX-CM}	Common mode return loss	—	6.0	—	—	dB
T _{TX-RISE}	Tx output rise time	20% to 80%	0.125	—	—	UI
T _{TX-FALL}	Tx output fall time	20% to 80%	0.125	—	—	UI
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link	—	—	—	1.3	ns
T _{TX-EYE}	Transmitter eye width	—	0.75	—	—	UI
T _{TX-EYE-MEDIAN-TO-MAX-JITTER}	Maximum time between jitter median and maximum deviation from median	—	—	—	0.125	UI
Receive^{1,2}						
UI	Unit Interval	—	399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage	—	0.34 ³	—	1.2	V
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage	—	65	—	340 ³	mV
V _{RX-CM-AC_P}	RMS AC peak common-mode input voltage	—	—	—	150	mV
Z _{RX-DIFF-DC}	DC differential input impedance	—	80	100	120	Ω
Z _{RX-DC}	DC input impedance	—	40	50	60	Ω
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance	—	200K	—	—	Ω
RL _{RX-DIFF}	Differential return loss	—	10	—	—	dB
RL _{RX-CM}	Common mode return loss	—	6.0	—	—	dB

Notes:

1. Values are measured at 2.5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express 1.1 standard.

3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit						
UI	Unit Interval	—	203.43	203.45	203.47	ps
T _{DCD}	Duty Cycle Distortion	—	—	—	0.05	UI
J _{UBHPJ}	Uncorrelated Bounded High Probability Jitter	—	—	—	0.15	UI
J _{TOTAL}	Total Jitter	—	—	—	0.3	UI
Z _{RX-DIFF-DC}	DC differential Impedance	—	80	—	120	Ω
T _{SKEW}	Skew between differential signals	—	—	—	9	ps
R _{LTX-DIFF}	Tx Differential Return Loss (S22), including package and silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R _{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	—	—	dB
I _{TX-SHORT}	Transmitter short-circuit current	—	—	—	100	mA
T _{RISE_FALL-DIFF}	Differential Rise and Fall Time	—	—	—	—	ps
L _{TX-SKEW}	Lane-to-lane output skew	—	—	—	—	ps
Receive						
UI	Unit Interval	—	203.43	203.45	203.47	ps
V _{RX-DIFF-PP}	Differential Rx peak-peak voltage	—	—	—	1.2	V, p-p
V _{RX-EYE_Y1_Y2}	Receiver eye opening mask, Y1 and Y2	—	62.5	—	375	mV, diff
V _{RX-EYE_X1}	Receiver eye opening mask, X1	—	—	—	0.3	UI
T _{RX-TJ}	Receiver total jitter tolerance (not including sinusoidal)	—	—	—	0.6	UI
R _{LRX-DIFF}	Receiver differential Return Loss, package plus silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R _{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z _{RX-DIFF-DC}	Receiver DC differential impedance	—	80	100	120	Ω

Note: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

Table 3.36. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J _{RX_DJ} ^{2, 3, 4}	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J _{RX_RJ} ^{2, 3, 4}	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J _{RX_SJ} ^{2, 3, 4}	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T _{RX_EYE}	Receiver eye opening	—	0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.29. Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics

3.29.1. AC and DC Characteristics

Table 3.37. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T _{RF}	Differential rise/fall time	20% to 80%	—	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance	—	80	100	120	Ω
J _{TX_DDJ} ^{2, 3}	Output data deterministic jitter	—	—	—	0.10	UI
J _{TX_TJ} ^{1, 2, 3}	Total output data jitter	—	—	—	0.24	UI

Notes:

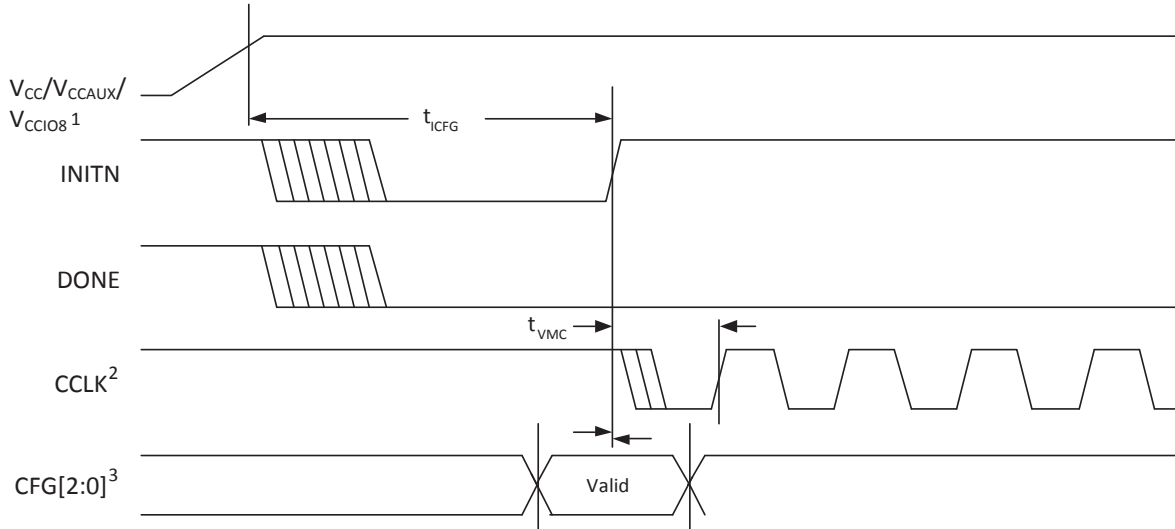
1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.38. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J _{RX_DJ} ^{1, 2, 3, 4}	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.34	UI
J _{RX_RJ} ^{1, 2, 3, 4}	Random jitter tolerance (peak-to-peak)	—	—	—	0.26	UI
J _{RX_SJ} ^{1, 2, 3, 4}	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.11	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total jitter tolerance (peak-to-peak)	—	—	—	0.71	UI
T _{RX_EYE}	Receiver eye opening	—	0.29	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.



1. Time taken from V_{CC} , V_{CCAUX} or V_{CCIOB} , whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPI_m).
3. The CFG pins are normally static (hardwired).

Figure 3.18. Power-On-Reset (POR) Timing

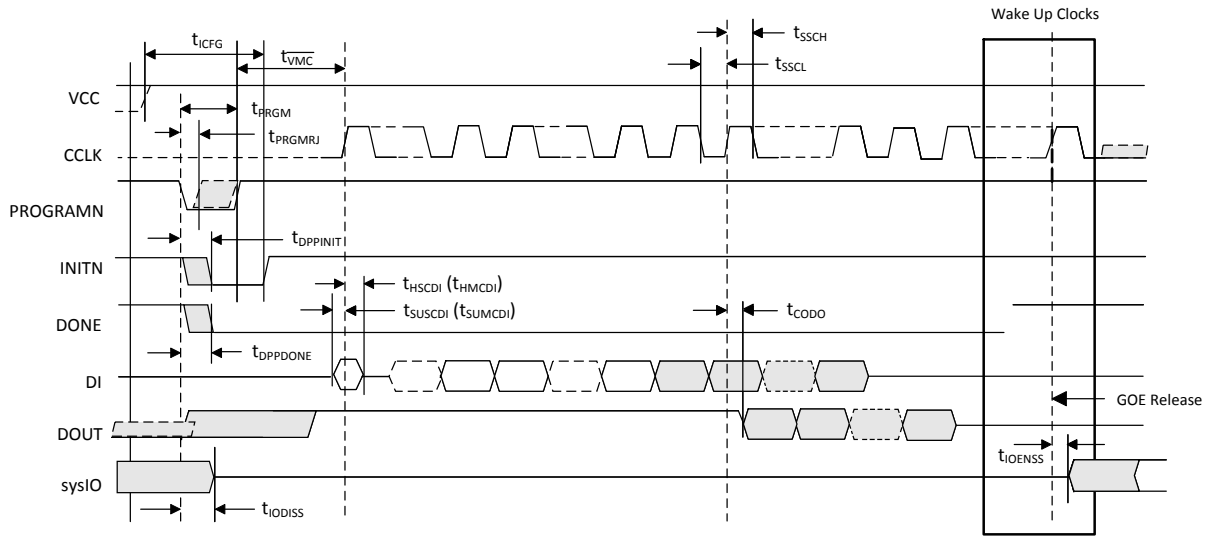


Figure 3.19. sysCONFIG Port Timing



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