# **E** Lattice Semiconductor Corporation - <u>LFE5U-12F-7MG285I Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	3000
Number of Logic Elements/Cells	12000
Total RAM Bits	589824
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-12f-7mg285i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



## Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay-Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLL	Phase-Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SERDES	Serializer/Deserializer
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
ТАР	Test Access Port
TDM	Time Division Multiplexing

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### 2.3. Routing

There are many resources provided in the ECP5/ECP5-5G devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The ECP5/ECP5-5G family has an enhanced routing architecture that produces a compact design. The Diamond design software tool suites take the output of the synthesis tool and places and routes the design.

### 2.4. Clocking Structure

ECP5/ECP5-5G clocking structure consists of clock synthesis blocks (sysCLOCK PLL); balanced clock tree networks (PCLK and ECLK trees); and efficient clock logic modules (CLOCK DIVIDER and Dynamic Clock Select (DCS), Dynamic Clock Control (DCC) and DLL). All of these functions are described below.

### 2.4.1. sysCLOCK PLL

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the ECP5/ECP5-5G family support two to four full-featured General Purpose PLLs. The sysCLOCK PLLs provide the ability to synthesize clock frequencies.

The architecture of the PLL is shown in Figure 2.5. A description of the PLL functionality follows.

CLKI is the reference frequency input to the PLL and its source can come from two different external CLK inputs or from internal routing. A non-glitchless 2-to-1 input multiplexor is provided to dynamically select between two different external reference clock sources. The CLKI input feeds into the input Clock Divider block.

CLKFB is the feedback signal to the PLL which can come from internal feedback path, routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLL has four clock outputs CLKOP, CLKOS, CLKOS2 and CLKOS3. Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the primary clock network. Only CLKOP and CLKOS outputs can go to the edge clock network.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the PHASESEL, PHASEDIR, PHASESTEP, and PHASELOADREG ports.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected.









Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

### 2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

#### 2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).



### 2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.



Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

### 2.9. sysDSP<sup>™</sup> Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### 2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.



In Figure 2.15, note that A\_ALU, B\_ALU and C\_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

#### Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	Ι

\*Note: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

### 2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.





\*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

#### Figure 2.20. Output Register Block on Left and Right Sides

Name	Туре	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

#### Table 2.9. Output Block Port Description

### 2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).



Figure 2.21. Tristate Register Block on Top Side



ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

• Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the  $V_{CCIO}$  voltage in the bank. When used as emulated differential outputs, the pair can be used together.

The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

Bank 4 I/O only exists in the LFE5-85 device.

Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

The top and bottom side pads can be identified by the Lattice Diamond tool.

Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

### 2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when  $V_{CC}$ ,  $V_{CCIO8}$  and  $V_{CCAUX}$  have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V<sub>CC</sub> and V<sub>CCAUX</sub> supply the power to the FPGA core fabric, whereas the V<sub>CCIO</sub> supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V<sub>CCIO</sub> supplies should be powered-up before or together with the V<sub>CC</sub> and V<sub>CCAUX</sub> supplies.

### 2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).



### 3.7. Hot Socketing Requirements

#### **Table 3.6. Hot Socketing Requirements**

Description	Min	Тур	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	_	_	8	mA
Input current per HDIN pin when device power supply is off, inputs driven <sup>1, 2</sup>	_	_	15	mA
Current per HDIN pin when device power ramps up, input driven <sup>3</sup>	—	—	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up <sup>4</sup>	_	_	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V<sub>CCHTX</sub>, 8b/10b data, no external AC coupling.

2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA \* 4 channels \* 2 input pins per channel = 120 mA.

- Device power supplies are ramping up (V<sub>CCA</sub> and V<sub>CCAUX</sub>), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V<sub>CCHTX</sub>, 8b/10b data, internal AC coupling.
- 4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to  $V_{CCHTX}$  by the far end receiver termination of 50  $\Omega$  single ended.

### 3.8. ESD Performance

Refer to the ECP5 and ECP5-5G Product Family Qualification Summary for complete qualification data, including ESD performance.

### 3.9. DC Electrical Characteristics

**Over Recommended Operating Conditions** 

Symbol	Parameter	Condition	Min	Тур	Max	Unit
I <sub>IL</sub> , I <sub>IH</sub> <sup>1, 4</sup>	Input or I/O Low Leakage	$0 \leq V_{IN} \leq V_{CCIO}$	—	_	10	μA
I <sub>IH</sub> <sup>1, 3</sup>	Input or I/O High Leakage	$V_{CCIO} < V_{IN} \le V_{IH(MAX)}$	—	_	100	μA
1	I/O Active Pull-up Current, sustaining logic HIGH state	$0.7 \ V_{CCIO} \leq V_{IN} \leq V_{CCIO}$	-30	_	_	μA
1PU	I/O Active Pull-up Current, pulling down from logic HIGH state	$0 \leq V_{\text{IN}} \leq 0.7 \ V_{\text{CCIO}}$	_	_	-150	μA
las	I/O Active Pull-down Current, sustaining logic LOW state	$0 \le V_{IN} \le V_{IL}$ (MAX)	30	_	_	μΑ
I <sub>PD</sub>	I/O Active Pull-down Current, pulling up from logic LOW state	$0 \leq V_{\text{IN}} \leq V_{\text{CCIO}}$	—	—	150	μA
C1	I/O Capacitance <sup>2</sup>	$\begin{split} V_{CCIO} &= 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V}, \\ V_{CC} &= 1.2 \text{ V}, \text{ V}_{IO} &= 0 \text{ to } ^{V_{IH(MAX)}} \end{split}$	_	5	8	pf
C2	Dedicated Input Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V}, \\ V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{\text{IH}(\text{MAX})}$	_	5	7	pf
N	Hysteresis for Single-Ended	V <sub>CCIO</sub> = 3.3 V	—	300	—	mV
V HYST	Inputs	V <sub>CCI0</sub> = 2.5 V	_	250	_	mV

#### **Table 3.7. DC Electrical Characteristics**

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T<sub>A</sub> 25 °C, f = 1.0 MHz.

- 3. Applicable to general purpose I/Os in top and bottom banks.
- 4. When used as  $V_{REF}$ , maximum leakage= 25  $\mu$ A.



### 3.11. SERDES Power Supply Requirements<sup>1,2,3</sup>

Over recommended operating conditions.

#### Table 3.9. ECP5UM

Symbol	Description	Тур	Max	Unit
Standby (Power	Down)			
I <sub>CCA-SB</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	4	9.5	mA
I <sub>CCHRX-SB</sub> <sup>4</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	—	0.1	mA
I <sub>CCHTX-SB</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	—	0.9	mA
<b>Operating</b> (Data	Rate = 3.125 Gb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	43	54	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
І <sub>сснтх-ор</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data	Rate = 2.5 Gb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	40	50	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
І <sub>сснтх-ор</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data	Rate = 1.25 Gb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	34	43	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
<b>Operating</b> (Data	Rate = 270 Mb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	28	38	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled

2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.

3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.

4. For ICCHRX-SB, during Standby, input termination on Rx are disabled.

5. For ICCHRX-OP, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

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#### Table 3.10. ECP5-5G

Symbol	Description	Тур	Max	Unit
Standby (Power	Down)			
I <sub>CCA-SB</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	4	9.5	mA
I <sub>CCHRX-SB</sub> <sup>4</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	_	0.1	mA
I <sub>CCHTX-SB</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	_	0.9	mA
Operating (Data	Rate = 5 Gb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	58	67	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data	Rate = 3.2 Gb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	48	57	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data	Rate = 2.5 Gb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	44	53	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data	Rate = 1.25 Gb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	36	46	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data	Rate = 270 Mb/s)			
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	30	40	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled

2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.

3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.

4. For ICCHRX-SB, during Standby, input termination on Rx are disabled.

5. For ICCHRX-OP, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.



### 3.15. Typical Building Block Function Performance

#### Table 3.19. Pin-to-Pin Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	5.06	ns
32-Bit Decoder	6.08	ns
64-Bit Decoder	5.06	ns
4:1 Mux	4.45	ns
8:1 Mux	4.63	ns
16:1 Mux	4.81	ns
32:1 Mux	4.85	ns

Notes:

1. I/Os are configured with LVCMOS25 with V<sub>CCIO</sub>=2.5, 12 mA drive.

2. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

3. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.



	<b>.</b>	_	1	-8		-7	-6		
Parameter	Description	Device	Min	Max	Min	Max	Min	Max	Unit
t <sub>h_delpll</sub>	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	_	0	_	0	_	ns
Generic DDR Input							•		
Generic DDRX1 Inp	uts With Clock and Data Centere	d at Pin (GDDI	RX1_RX.	SCLK.Cent	tered) Us	ing PCLK	Clock In	put - Fig	ure 3.6
t <sub>SU_GDDRX1_centered</sub>	Data Setup Before CLK Input	All Devices	0.52	-	0.52	-	0.52	_	ns
t <sub>HD_GDDRX1_centered</sub>	Data Hold After CLK Input	All Devices	0.52	_	0.52	_	0.52	_	ns
f <sub>DATA_GDDRX1_centered</sub>	GDDRX1 Data Rate	All Devices	_	500	_	500	_	500	Mb/s
f <sub>MAX_GDDRX1_centered</sub>	GDDRX1 CLK Frequency (SCLK)	All Devices	_	250	-	250	_	250	MHz
Generic DDRX1 Inp	uts With Clock and Data Aligned	at Pin (GDDR)	(1_RX.SC	LK.Aligne	ed) Using	PCLK Cl	ock Input	- Figure	3.7
$t_{su\_GDDRX1\_aligned}$	Data Setup from CLK Input	All Devices	-	-0.55	-	-0.55	-	-0.55	ns + 1/2 UI
$t_{HD_GDDRX1_aligned}$	Data Hold from CLK Input	All Devices	0.55	_	0.55	-	0.55	-	ns + 1/2 UI
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	-	500	—	500	Mb/s
f <sub>MAX_GDDRX1_aligned</sub>	GDDRX1 CLK Frequency (SCLK)	All Devices	_	250	_	250	_	250	MHz
Generic DDRX2 Inp	uts With Clock and Data Centere	d at Pin (GDDI	RX2_RX.I	ECLK.Cen	tered) Us	ing PCLK	Clock In	put, Left	and
Right sides Only - F	igure 3.6	1	T		T	1	1	1	1
$t_{SU_GDDRX2_centered}$	Data Setup before CLK Input	All Devices	0.321	. –	0.403	—	0.471	—	ns
$t_{HD_GDDRX2\_centered}$	Data Hold after CLK Input	All Devices	0.321	. —	0.403	_	0.471	_	ns
$f_{\text{DATA}_{GDDRX2}_{centered}}$	GDDRX2 Data Rate	All Devices	_	800	_	700	_	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	-	400	—	350	—	312	MHz
Generic DDRX2 Inp	uts With Clock and Data Aligned	at Pin (GDDR)	(2_RX.EC	LK.Aligne	ed) Using	PCLK Cl	ock Input	, Left an	d Right
sides Only - Figure	3.7								1
t <sub>SU_GDDRX2_aligned</sub>	Data Setup from CLK Input	All Devices	—	-0.344	—	-0.42	_	-0.495	ns + 1/2 UI
$t_{HD_GDDRX2_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	_	0.495	-	ns + 1/2 UI
$f_{DATA_GDDRX2_aligned}$	GDDRX2 Data Rate	All Devices	_	800	—	700	—	624	Mb/s
f <sub>MAX_GDDRX2_aligned</sub>	GDDRX2 CLK Frequency	All Devices	—	400	—	350	_	312	MHz
Video DDRX71 Inpu	uts With Clock and Data Aligned a	t Pin (GDDRX	71_RX.E	CLK) Usin	g PLL Clo	ck Input	, Left and	Right si	des Only
Figure 3.11									
t <sub>su_lvds71_i</sub>	Data Setup from CLK Input (bit i)	All Devices	_	-0.271	—	-0.39	_	-0.41	ns+(1/2+i) * UI
t <sub>HD_LVDS71_i</sub>	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	_	0.41	_	ns+(1/2+i) * UI
f <sub>DATA_LVDS71</sub>	DDR71 Data Rate	All Devices	_	756	—	620	—	525	Mb/s
f <sub>MAX_LVDS71</sub>	DDR71 CLK Frequency (ECLK)	All Devices	_	378	—	310	—	262.5	MHz

#### Table 3.22. ECP5/ECP5-5G External Switching Characteristics (Continued)





Figure 3.9. Transmit TX.CLK.Aligned Waveforms

#### Receiver – Shown for one LVDS Channel



#### Transmitter - Shown for one LVDS Channel



Figure 3.10. DDRX71 Video Timing Waveforms

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### 3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

#### Table 3.31. PCIe (5 Gb/s)

Symbol	Description		Min	Тур	Max	Unit
Transmit <sup>1</sup>						
UI	Unit Interval	—	199.94	200	200.06	ps
B <sub>WTX-PKG-PLL2</sub>	Tx PLL bandwidth corresponding to PKGTX-PLL2	-	5	_	16	MHz
P <sub>KGTX-PLL2</sub>	Tx PLL Peaking	-	_	—	1	dB
V <sub>TX-DIFF-PP</sub>	Differential p-p Tx voltage swing	-	0.8	—	1.2	V, p-р
V <sub>TX-DIFF-PP-LOW</sub>	Low power differential p-p Tx voltage swing	-	0.4	_	1.2	V, p-p
V <sub>TX-DE-RATIO-3.5dB</sub>	Tx de-emphasis level ratio at 3.5dB	-	3	—	4	dB
V <sub>TX-DE-RATIO-6dB</sub>	Tx de-emphasis level ratio at 6dB	-	5.5	_	6.5	dB
T <sub>MIN-PULSE</sub>	Instantaneous lone pulse width	_		_	_	UI
T <sub>TX-RISE-FALL</sub>	Transmitter rise and fall time	_		_	_	UI
T <sub>TX-EYE</sub>	Transmitter Eye, including all jitter sources	_	0.75	_	_	UI
T <sub>TX-DJ</sub>	Tx deterministic jitter > 1.5 MHz	_	_	_	0.15	UI
T <sub>TX-RJ</sub>	Tx RMS jitter < 1.5 MHz	-	-	_	3	ps, RMS
T <sub>RF-MISMATCH</sub>	Tx rise/fall time mismatch	-	_	—		UI
B	Tx Differential Return Loss, including	50 MHz < freq < 1.25 GHz	10	_	_	dB
INLTX-DIFF	package and silicon	1.25 GHz < freq < 2.5 GHz	8	_	_	dB
R <sub>LTX-CM</sub>	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	_	-	dB
Z <sub>TX-DIFF-DC</sub>	DC differential Impedance	-	_	—	120	Ω
V <sub>TX-CM-AC-PP</sub>	Tx AC peak common mode voltage, peak-peak	-	-	—		mV, p-p
I <sub>TX-SHORT</sub>	Transmitter short-circuit current	_	_	_	90	mA
V <sub>TX-DC-CM</sub>	Transmitter DC common-mode voltage	_	0	_	1.2	v
V <sub>TX-IDLE-DIFF-DC</sub>	Electrical Idle Output DC voltage	-	0	_	5	mV
V <sub>TX-IDLE-DIFF-AC-p</sub>	Electrical Idle Differential Output peak voltage	_	_	_		mV
V <sub>TX-RCV-DETECT</sub>	Voltage change allowed during Receiver Detect	_	_	_	600	mV
T <sub>TX-IDLE-MIN</sub>	Min. time in Electrical Idle	-	20	—	_	ns
T <sub>TX-IDLE-SET-TO-IDLE</sub>	Max. time from El Order Set to valid Electrical Idle	_	_	_	8	ns
T <sub>TX-IDLE-TO-DIFF-DATA</sub>	Max. time from Electrical Idle to valid differential output	_	_	_	8	ns
L <sub>TX-SKEW</sub>	Lane-to-lane output skew	—	_	—		ps



### 3.27. XAUI/CPRI LV E.30 Electrical and Timing Characteristics

### 3.27.1. AC and DC Characteristics

Over recommended operating conditions.

#### Table 3.33. Transmit

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
T <sub>RF</sub>	Differential rise/fall time	20% to 80%	_	80	—	ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance	—	80	100	120	Ω
J <sub>TX_DDJ</sub> <sup>2, 3</sup>	Output data deterministic jitter	—	_	—	0.17	UI
J <sub>TX_TJ</sub> <sup>1, 2, 3</sup>	Total output data jitter	-	_	—	0.35	UI

Notes:

- 1. Total jitter includes both deterministic jitter and random jitter.
- 2. Jitter values are measured with each CML output AC coupled into a 50  $\Omega$  impedance (100  $\Omega$  differential impedance).
- 3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Over recommended operating conditions.

#### Table 3.34. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 3.125 GHz	10	-	_	dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 3.125 GHz	6	-	_	dB
Z <sub>RX_DIFF</sub>	Differential termination resistance	—	80	100	120	Ω
J <sub>RX_DJ</sub> <sup>1, 2, 3</sup>	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J <sub>RX_RJ</sub> 1, 2, 3	Random jitter tolerance (peak-to-peak)	—	—	-	0.18	UI
J <sub>RX_SJ</sub> <sup>1, 2, 3</sup>	Sinusoidal jitter tolerance (peak-to-peak)	—	_		0.10	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3</sup>	Total jitter tolerance (peak-to-peak)	—	_	—	0.65	UI
T <sub>RX_EYE</sub>	Receiver eye opening	_	0.35	_	_	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.

2. Jitter values are measured with each high-speed input AC coupled into a 50  $\Omega$  impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

### 3.28. CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics

#### 3.28.1. AC and DC Characteristics

#### Table 3.35. Transmit

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
T <sub>RF</sub> <sup>1</sup>	Differential rise/fall time	20% to 80%	-	80	—	ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance	_	80	100	120	Ω
J <sub>TX_DDJ</sub> <sup>3, 4</sup>	Output data deterministic jitter	_	_	—	0.17	UI
J <sub>TX_TJ</sub> <sup>2, 3, 4</sup>	Total output data jitter	_	_	—	0.35	UI

Notes:

1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.

- 2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
- 3. Jitter values are measured with each CML output AC coupled into a 50  $\Omega$  impedance (100  $\Omega$  differential impedance).
- 4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.





- 1. Time taken from  $V_{CC}$ ,  $V_{CCAUX}$  or  $V_{CCIO8}$ , whichever is the last to cross the POR trip point.
- 2. Device is in a Master Mode (SPI, SPIm).
- 3. The CFG pins are normally static (hardwired).





Figure 3.19. sysCONFIG Port Timing

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\*The CFG pins are normally static (hardwired).









Signal Name	I/O	Description			
PLL, DLL and Clock Functions (Continued)					
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.			
[T/R]]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.			
Test and Programming (Dedicated Pin	s)				
TMC		Test Mode Select input, used to control the 1149.1 state machine. Pull-up is			
1015	1	enabled during configuration. This is a dedicated input pin.			
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.			
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.			
TDO	0	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.			
Configuration Pads (Used during sysC	ONFIG)				
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.			
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.			
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.			
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.			
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes (Master SPI, Master Serial). This is a dedicated pin.			
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPIm mode data output. This is a shared I/O pin. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.			
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.			
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.			
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.			
DOUT/CSON	0	Serial data output. Chip select output. SPI/SPIm mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O			
D0/MOSI/IO0	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.			

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#### (Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.



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