Lattice Semiconductor Corporation - <u>LFE5U-12F-8MG285I Datasheet</u>



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3000
Number of Logic Elements/Cells	12000
Total RAM Bits	589824
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-12f-8mg285i

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1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, highspeed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance. The Lattice Diamond[™] design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
 - 12K to 84K LUTs
 - 197 to 365 user programmable I/Os
- Embedded SERDES
 - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
 - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
 - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
 - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
 - Fully cascadable slice architecture
 - 12 to 160 slices for high performance multiply and accumulate
 - Powerful 54-bit ALU operations
 - Time Division Multiplexing MAC Sharing
 - Rounding and truncation
 - Each slice supports
 - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
 - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
 - Up to 3.744 Mb sysMEM[™] Embedded Block RAM (EBR)
 - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs



2.7. **DDRDLL**

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.



Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Туре	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.





Figure 2.15. Detailed sysDSP Slice Diagram





Figure 2.24. DQS Control and Delay Block (DQSBUF)

Name	Туре	Description
DQS	Input	DDR memory DQS strobe
READ[1:0]	Input	Read Input from DDR Controller
READCLKSEL[1:0]	Input	Read pulse selection
SCLK	Input	Slow System Clock
ECLK	Input	High Speed Edge Clock (same frequency as DDR memory)
DQSDEL	Input	90° Delay Code from DDRDLL
RDLOADN, RDMOVE, RDDIRECTION	Input	Dynamic Margin Control ports for Read delay
WRLOADN, WRMOVE, WRDIRECTION	Input	Dynamic Margin Control ports for Write delay
PAUSE	Input	Used by DDR Controller to Pause write side signals during DDRDLL Code update or Write Leveling
DYNDELAY[7:0]	Input	Dynamic Write Leveling Delay Control
DQSR90	Output	90° delay DQS used for Read
DQSW270	Output	90° delay clock used for DQ Write
DQSW	Output	Clock used for DQS Write
RDPNTR[2:0]	Output	Read Pointer for IFIFO module
WRPNTR[2:0]	Output	Write Pointer for IFIFO module
DATAVALID	Output	Signal indicating start of valid data
BURSTDET	Output	Burst Detect indicator
RDFLAG	Output	Read Dynamic Margin Control output to indicate max value
WRFLAG	Output	Write Dynamic Margin Control output to indicate max value

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ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

• Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

Bank 4 I/O only exists in the LFE5-85 device.

Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

The top and bottom side pads can be identified by the Lattice Diamond tool.

Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).



Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-85	
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	-	2	2
756 caBGA	-	-	2

Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).



Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

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2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to Minimizing System Interruption During Configuration Using TransFR Technology (TN1087) for details.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED Soft Error Detect
- SEC Soft Error Correction
- SEI Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

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When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)				
2.4				
4.8				
9.7				
19.4				
38.8				
62				

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.



Deveryoten	Description	Davias	_	-8	-7		-6		11
Parameter	Description Devi		Min	Мах	Min	Max	Min	Max	Unit
fdata_ddr2 fdata_ddr3 fdata_ddr3l fdata_ddr3l fdata_lpddr2 fdata_lpddr3	DDR Memory Data Rate	All Devices	_	800	_	700	_	624	Mb/s
fmax_ddr2 fmax_ddr3 fmax_ddr3l fmax_lpddr2 fmax_lpddr3	DDR Memory CLK Frequency (ECLK)	All Devices	_	400	_	350	_	312	MHz
DDR2/DDR3/DDR	3L/LPDDR2/LPDDR3 WRITE (DO	Q Output Data	are Cente	ered to DC	QS)				
tDQVBS_DDR2 tDQVBS_DDR3 tDQVBS_DDR3L tDQVBS_LPDDR2 tDQVBS_LPDDR3 tDQVAS_DDR2	Data Output Valid before DQS Output	All Devices	_	-0.25	_	-0.25	_	-0.25	UI
t _{DQVAS_DDR3} t _{DQVAS_DDR3L} t _{DQVAS_LPDDR2} t _{DQVAS_LPDDR3}	Data Output Valid after DQS Output	All Devices	0.25	_	0.25	_	0.25	_	UI
fdata_ddr2 fdata_ddr3 fdata_ddr3 fdata_ddr3l fdata_lpddr2 fdata_lpddr3	DDR Memory Data Rate	All Devices	_	800	_	700	_	624	Mb/s
fmax_ddr2 fmax_ddr3 fmax_ddr3l fmax_lpddr2 fmax_lpddr3	DDR Memory CLK Frequency (ECLK)	All Devices	_	400	_	350	_	312	MHz

Notes:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.

 General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load. Generic DDR timing are numbers based on LVDS I/O. DDR2 timing numbers are based on SSTL18. DDR3 timing numbers are based on SSTL15. LPDDR2 and LPDDR3 timing numbers are based on HSUL12.

- 3. Uses LVDS I/O standard for measurements.
- 4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- 5. All numbers are generated with the Diamond software.

FPGA-DS-02012-1.9





Figure 3.9. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter - Shown for one LVDS Channel



Figure 3.10. DDRX71 Video Timing Waveforms

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Table 3.31. PCIe (5 Gb/s) (Continued)

Symbol	Description	Test Conditions	Min	Тур	Мах	Unit
Receive ^{1, 2}		' 				
UI	Unit Interval	—	199.94	200	200.06	ps
V _{RX-DIFF-PP}	Differential Rx peak-peak voltage	—	0.34 ³	_	1.2	V, p-p
T _{RX-RJ-RMS}	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	_	Ι	4.2	ps, RMS
T _{RX-DJ}	Receiver deterministic jitter tolerance	—	—	_	88	ps
V _{RX-CM-AC}	Common mode noise from Rx	_	_	Ι		тV <i>,</i> p-р
D	Receiver differential Return Loss,	50 MHz < freq < 1.25 GHz	10	Ι	Ι	dB
NLRX-DIFF	package plus silicon	1.25 GHz < freq < 2.5 GHz	8	Ι	Ι	dB
R _{LRX-CM}	Receiver common mode Return Loss, package plus silicon	_	6	Ι	Ι	dB
Z _{RX-DC}	Receiver DC single ended impedance	—	40		60	Ω
Z _{RX-HIGH-IMP-DC}	Receiver DC single ended impedance when powered down	_	200K		I	Ω
V _{RX-CM-AC-P}	Rx AC peak common mode voltage	_	_	_		mV <i>,</i> peak
V _{RX-IDLE-DET-DIFF-PP}	Electrical Idle Detect Threshold	_	65	-	340 ³	mv,
L _{RX-SKEW}	Receiver lane-lane skew	_	_	_	8	ns

Notes:

1. Values are measured at 5 Gb/s.

2. Measured with external AC-coupling on the receiver.

3. Not in compliance with PCI Express standard.

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3.31. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications

Symbol	Parameter		Min	Max	Unit
POR, Config	uration Initialization, and Wakeup				
t _{ICFG}	Time from the Application of V_{CC} , V_{CCAUX} or V_{CCI08} (whichever is the last) to the rising edge of INITN	-	_	33	ms
t _{VMC}	Time from t _{ICFG} to the valid Master CCLK	_	_	5	us
t _{cz}	CCLK from Active to High-Z	_	_	300	ns
Master CCL	K		1	1	
f _{MCLK}	Frequency	All selected frequencies	-20	20	%
t _{MCLK-DC}	Duty Cycle	All selected frequencies	40	60	%
All Configur	ation Modes				
t _{PRGM}	PROGRAMN LOW pulse accepted	-	110	_	ns
t _{PRGMRJ}	PROGRAMN LOW pulse rejected	_	_	50	ns
t _{INITL}	INITN LOW time	_	—	55	ns
t _{dppint}	PROGRAMN LOW to INITN LOW	_	—	70	ns
t _{dppdone}	PROGRAMN LOW to DONE LOW	_	_	80	ns
t _{IODISS}	PROGRAMN LOW to I/O Disabled	_	—	150	ns
Slave SPI			'	'	
f _{CCLK}	CCLK input clock frequency	-	_	60	MHz
t _{CCLKH}	CCLK input clock pulsewidth HIGH	-	6	_	ns
t _{CCLKL}	CCLK input clock pulsewidth LOW	_	6	_	ns
t _{stsu}	CCLK setup time	-	1	_	ns
t _{sth}	CCLK hold time	-	1	_	ns
t _{sтсо}	CCLK falling edge to valid output	-	_	10	ns
t _{stoz}	CCLK falling edge to valid disable	-	_	10	ns
t _{stov}	CCLK falling edge to valid enable	-	_	10	ns
t _{scs}	Chip Select HIGH time —		25	_	ns
t _{scss}	Chip Select setup time	-	3	_	ns
t _{scsн}	Chip Select hold time	-	3	_	ns
Master SPI			,		
f _{CCLK}	Max selected CCLK output frequency	_	—	62	MHz
t _{CCLKH}	CCLK output clock pulse width HIGH	_	3.5	—	ns
t _{CCLKL}	CCLK output clock pulse width LOW	_	3.5	—	ns
t _{stsu}	CCLK setup time	_	5	—	ns
t _{sтн}	CCLK hold time	_	1	—	ns
t _{CSSPI}	INITN HIGH to Chip Select LOW	_	100	200	ns
t _{CFGX}	INITN HIGH to first CCLK edge	_	—	150	ns
Slave Serial					
f _{CCLK}	CCLK input clock frequency	-	_	66	MHz
t _{ssch}	CCLK input clock pulse width HIGH	_	5	_	ns
t _{SSCL}	CCLK input clock pulse width LOW	_	5	-	ns
t _{suscdi}	CCLK setup time	_	0.5	_	ns
t _{HSCDI}	CCLK hold time	_	1.5	—	ns

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*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3.16. sysCONFIG Parallel Port Write Cycle



Figure 3.17. sysCONFIG Slave Serial Port Timing





*The CFG pins are normally static (hardwired).









Signal Name	I/O	Description				
PLL, DLL and Clock Functions (Continued)						
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_ num = ball number associated with DQS[T] pin.				
[T/R]]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.				
Test and Programming (Dedicated Pin	s)					
TMC		Test Mode Select input, used to control the 1149.1 state machine. Pull-up is				
1015	I	enabled during configuration. This is a dedicated input pin.				
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.				
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.				
TDO	0	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.				
Configuration Pads (Used during sysC	ONFIG)					
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.				
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.				
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.				
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.				
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes (Master SPI, Master Serial). This is a dedicated pin.				
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPIm mode data output. This is a shared I/O pin. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.				
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.				
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.				
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.				
DOUT/CSON	0	Serial data output. Chip select output. SPI/SPIm mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O				
D0/MOSI/IO0	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.				

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Pin Information Summary		LFE5UM/ LFE5UM5G-25		M5G-45	LFE5UM/LFE5UM5G-85					
Pin Type		285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA
ТАР		4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated Pins		7	7	7	7	7	7	7	7	7
GND		83	59	83	59	113	83	59	113	166
NC		1	8	1	2	33	1	0	17	29
Reserved		0	2	0	2	4	0	2	4	4
SERDES		14	28	14	28	28	14	28	28	28
VCCA (SERDES)	VCCA0	2	2	2	2	6	2	2	6	8
	VCCA1	0	2	0	2	6	0	2	6	9
	VCCAUXA0	2	2	2	2	2	2	2	2	2
VCCAUX (SERDES)	VCCAUXA1	0	2	0	2	2	0	2	2	2
GNDA (SERDES)		26	26	26	26	49	26	26	49	60
Total Balls		285	381	285	381	554	285	381	554	756
	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	10/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8	24/12
High Speed Differential Input / Output Pairs	Bank 3	14/7	16/8	14/7	16/8	24/12	14/7	16/8	24/12	32/16
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	13/6	16/8	13/6	16/8	24/12	13/6	16/8	24/12	32/16
	Bank 7	8/6	16/8	8/6	16/8	16/8	8/6	16/8	16/8	24/12
	Bank 8	0	0	0	0	0	0	0	0	0
Total High Speed Differential I/O Pairs		45/2	64/32	45/27	64/3	80/40	45/27	65/3	80/40	112/5
DQS Groups (> 11 pins in group)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	1	2	1	2	2	1	2	2	3
	Bank 3	2	2	2	2	3	2	2	3	4
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	2	2	2	2	3	2	2	3	4
	Bank 7	1	2	1	2	2	1	2	2	3
	Bank 8	0	0	0	0	0	0	0	0	0
Total DQS Groups		6	8	6	8	10	6	8	10	14



5. Ordering Information

5.1. ECP5/ECP5-5G Part Number Description





Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	-8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	-8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	-8	Lead free caBGA	756	Commercial	84	Yes

5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	-6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	-7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	-8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	-6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	-7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	-8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	-6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	-7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	-8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	-6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	-7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	-8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	-6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	-7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	-6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	-7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	-6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	-7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	-8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	-6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	-7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	-6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	-7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	-6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	-7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	-6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	-7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	-6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	-7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	-6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	-7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	No