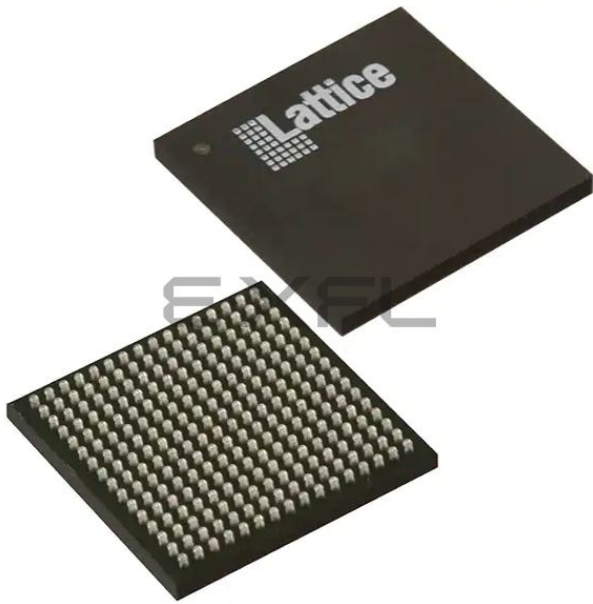




Welcome to [E·XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-25f-6bg256i

Copyright Notice

Copyright © 2014-2018 Lattice Semiconductor Corporation. All rights reserved. The contents of these materials contain proprietary and confidential information (including trade secrets, copyright, and other Intellectual Property interests) of Lattice Semiconductor Corporation and/or its affiliates. All rights are reserved. You are permitted to use this document and any information contained therein expressly and only for bona fide non-commercial evaluation of products and/or services from Lattice Semiconductor Corporation or its affiliates; and only in connection with your bona fide consideration of purchase or license of products or services from Lattice Semiconductor Corporation or its affiliates, and only in accordance with the terms and conditions stipulated. Contents, (in whole or in part) may not be reproduced, downloaded, disseminated, published, or transferred in any form or by any means, except with the prior written permission of Lattice Semiconductor Corporation and/or its affiliates. Copyright infringement is a violation of federal law subject to criminal and civil penalties. You have no right to copy, modify, create derivative works of, transfer, sublicense, publicly display, distribute or otherwise make these materials available, in whole or in part, to any third party. You are not permitted to reverse engineer, disassemble, or decompile any device or object code provided herewith. Lattice Semiconductor Corporation reserves the right to revoke these permissions and require the destruction or return of any and all Lattice Semiconductor Corporation proprietary materials and/or data.

Patents

The subject matter described herein may contain one or more inventions claimed in patents or patents pending owned by Lattice Semiconductor Corporation and/or its affiliates.

Trademark Acknowledgment

Lattice Semiconductor Corporation®, the Lattice Semiconductor logo, Silicon Image®, the Silicon Image logo, Instaport®, the Instaport logo, InstaPrevue®, Simplay®, Simplay HD®, the Simplay HD logo, Simplay Labs™, the Simplay Labs logo, the SiBEAM Snap™, the SiBEAM Snap logo, UltraGig™, the UltraGig logo are trademarks or registered trademarks of Lattice Semiconductor Corporation in the United States and/or other countries. HDMI® and the HDMI logo with High-Definition Multimedia Interface are trademarks or registered trademarks of, and are used under license from, HDMI Licensing, LLC. in the United States or other countries. MHL® and the MHL logo with Mobile High-Definition Link are trademarks or registered trademarks of, and are used under license from, MHL, LLC. in the United States and/or other countries. WirelessHD®, the WirelessHD logo, WiHD® and the WiHD logo are trademarks, registered trademarks or service marks of SiBeam, Inc. in the United States or other countries. HDMI Licensing, LLC; MHL, LLC; Simplay Labs, LLC; and SiBeam, Inc. are wholly owned subsidiaries of Lattice Semiconductor Corporation.

All other trademarks and registered trademarks are the property of their respective owners in the United States or other countries. The absence of a trademark symbol does not constitute a waiver of Lattice Semiconductor's trademarks or other intellectual property rights with regard to a product name, logo or slogan.

Export Controlled Document

This document contains materials that are subject to the U.S. Export Administration Regulations and may also be subject to additional export control laws and regulations (collectively "Export Laws") and may be used only in compliance with such Export Laws. Unless otherwise authorized by an officer of Lattice Semiconductor Corporation in writing, this document and the information contained herein (a) may not be used in relation to nuclear, biological or chemical weapons, or missiles capable of delivering these weapons, and (b) may not be re-exported or otherwise transferred to a third party who is known or suspected to be involved in relation to nuclear, biological or chemical weapons, or missiles capable of delivering these weapons, or to any sanctioned persons or entities.

Further Information

To request other materials, documentation, and information, contact your local Lattice Semiconductor sales office or visit the Lattice Semiconductor web site at www.latticesemi.com.

Disclaimers

These materials are provided on an "AS IS" basis. Lattice Semiconductor Corporation and its affiliates disclaim all representations and warranties (express, implied, statutory or otherwise), including but not limited to: (i) all implied warranties of merchantability, fitness for a particular purpose, and/or non-infringement of third party rights; (ii) all warranties arising out of course-of-dealing, usage, and/or trade; and (iii) all warranties that the information or results provided in, or that may be obtained from use of, the materials are accurate, reliable, complete, up-to-date, or produce specific outcomes. Lattice Semiconductor Corporation and its affiliates assume no liability or responsibility for any errors or omissions in these materials, makes no commitment or warranty to correct any such errors or omissions or update or keep current the information contained in these materials, and expressly disclaims all direct, indirect, special, incidental, consequential, reliance and punitive damages, including WITHOUT LIMITATION any loss of profits arising out of your access to, use or interpretation of, or actions taken or not taken based on the content of these materials. Lattice Semiconductor Corporation and its affiliates reserve the right, without notice, to periodically modify the information in these materials, and to add to, delete, and/or change any of this information.

Products and Services

The products and services described in these materials, and any other information, services, designs, know-how and/or products provided by Lattice Semiconductor Corporation and/or its affiliates are provided on "AS IS" basis, except to the extent that Lattice Semiconductor Corporation and/or its affiliates provides an applicable written limited warranty in its standard form license agreements, standard Terms and Conditions of Sale and Service or its other applicable standard form agreements, in which case such limited warranty shall apply and shall govern in lieu of all other warranties (express, statutory, or implied). EXCEPT FOR SUCH LIMITED WARRANTY, LATTICE SEMICONDUCTOR CORPORATION AND ITS AFFILIATES DISCLAIM ALL REPRESENTATIONS AND WARRANTIES (EXPRESS, IMPLIED, STATUTORY OR OTHERWISE), REGARDING THE INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS PROVIDED BY LATTICE SEMICONDUCTOR CORPORATION AND/OR ITS AFFILIATES, INCLUDING BUT NOT LIMITED TO, ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND/OR NON-INFRINGEMENT OF THIRD PARTY RIGHTS. YOU ACKNOWLEDGE AND AGREE THAT SUCH INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS HAVE NOT BEEN DESIGNED, TESTED, OR MANUFACTURED FOR USE OR RESALE IN SYSTEMS WHERE THE FAILURE, MALFUNCTION, OR ANY INACCURACY OF THESE ITEMS CARRIES A RISK OF DEATH OR SERIOUS BODILY INJURY, INCLUDING, BUT NOT LIMITED TO, USE IN NUCLEAR FACILITIES, AIRCRAFT NAVIGATION OR COMMUNICATION, EMERGENCY SYSTEMS, OR OTHER SYSTEMS WITH A SIMILAR DEGREE OF POTENTIAL HAZARD. NO PERSON IS AUTHORIZED TO MAKE ANY OTHER WARRANTY OR REPRESENTATION CONCERNING THE PERFORMANCE OF THE INFORMATION, PRODUCTS, KNOW-HOW, DESIGNS OR SERVICES OTHER THAN AS PROVIDED IN THESE TERMS AND CONDITIONS.

3.1.	Absolute Maximum Ratings	47
3.2.	Recommended Operating Conditions	47
3.3.	Power Supply Ramp Rates.....	48
3.4.	Power-On-Reset Voltage Levels	48
3.5.	Power up Sequence.....	48
3.6.	Hot Socketing Specifications	48
3.7.	Hot Socketing Requirements.....	49
3.8.	ESD Performance.....	49
3.9.	DC Electrical Characteristics	49
3.10.	Supply Current (Standby)	50
3.11.	SERDES Power Supply Requirements ^{1,2,3}	51
3.12.	sysI/O Recommended Operating Conditions	53
3.13.	sysI/O Single-Ended DC Electrical Characteristics	54
3.14.	sysI/O Differential Electrical Characteristics	55
3.14.1.	LVDS.....	55
3.14.2.	SSTLD	55
3.14.3.	LVC MOS33D.....	55
3.14.4.	LVDS25E	56
3.14.5.	BLVDS25.....	57
3.14.6.	LVPECL33	58
3.14.7.	MLVDS25	59
3.14.8.	SLVS	60
3.15.	Typical Building Block Function Performance	61
3.16.	Derating Timing Tables.....	62
3.17.	Maximum I/O Buffer Speed	63
3.18.	External Switching Characteristics	64
3.19.	sysCLOCK PLL Timing.....	71
3.20.	SERDES High-Speed Data Transmitter.....	72
3.21.	SERDES/PCS Block Latency	73
3.22.	SERDES High-Speed Data Receiver	74
3.23.	Input Data Jitter Tolerance.....	74
3.24.	SERDES External Reference Clock.....	75
3.25.	PCI Express Electrical and Timing Characteristics.....	76
3.25.1.	PCIe (2.5 Gb/s) AC and DC Characteristics.....	76
3.25.2.	PCIe (5 Gb/s) – Preliminary AC and DC Characteristics	77
3.26.	CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary.....	79
3.27.	XAUI/CPRI LV E.30 Electrical and Timing Characteristics	80
3.27.1.	AC and DC Characteristics	80
3.28.	CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics	80
3.28.1.	AC and DC Characteristics	80
3.29.	Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics	81
3.29.1.	AC and DC Characteristics	81
3.30.	SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics	82
3.30.1.	AC and DC Characteristics	82
3.31.	sysCONFIG Port Timing Specifications	83
3.32.	JTAG Port Timing Specifications	88
3.33.	Switching Test Conditions	89
4.	Pinout Information	91
4.1.	Signal Descriptions	91
4.2.	PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin	94
4.3.	Pin Information Summary	94
4.3.1.	LFE5UM/LFE5UM5G	94
4.3.2.	LFE5U	96
5.	Ordering Information.....	97

Figures

Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)	13
Figure 2.2. PFU Diagram	14
Figure 2.3. Slice Diagram	15
Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8	16
Figure 2.5. General Purpose PLL Diagram.....	18
Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking.....	20
Figure 2.7. DCS Waveforms	21
Figure 2.8. Edge Clock Sources per Bank	22
Figure 2.9. ECP5/ECP5-5G Clock Divider Sources	22
Figure 2.10. DDRDLL Functional Diagram	23
Figure 2.11. ECP5/ECP5-5G DLL Top Level View (For LFE-45 and LFE-85)	24
Figure 2.12. Memory Core Reset	26
Figure 2.13. Comparison of General DSP and ECP5/ECP5-5G Approaches	27
Figure 2.14. Simplified sysDSP Slice Block Diagram	28
Figure 2.15. Detailed sysDSP Slice Diagram	29
Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Sides	31
Figure 2.17. Input Register Block for PIO on Top Side of the Device	32
Figure 2.18. Input Register Block for PIO on Left and Right Side of the Device.....	32
Figure 2.19. Output Register Block on Top Side	33
Figure 2.20. Output Register Block on Left and Right Sides	34
Figure 2.21. Tristate Register Block on Top Side.....	34
Figure 2.22. Tristate Register Block on Left and Right Sides.....	35
Figure 2.23. DQS Grouping on the Left and Right Edges	36
Figure 2.24. DQS Control and Delay Block (DQSBUF)	37
Figure 2.25. ECP5/ECP5-5G Device Family Banks	38
Figure 2.26. On-Chip Termination	40
Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)	42
Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block	43
Figure 3.1. LVDS25E Output Termination Example	56
Figure 3.2. BLVDS25 Multi-point Output Example.....	57
Figure 3.3. Differential LVPECL33	58
Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)	59
Figure 3.5. SLVS Interface	60
Figure 3.6. Receiver RX.CLK.Centered Waveforms	68
Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms.....	68
Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms.....	68
Figure 3.9. Transmit TX.CLK.Aligned Waveforms.....	69
Figure 3.10. DDRX71 Video Timing Waveforms.....	69
Figure 3.11. Receiver DDRX71_RX Waveforms.....	70
Figure 3.12. Transmitter DDRX71_TX Waveforms.....	70
Figure 3.13. Transmitter and Receiver Latency Block Diagram	73
Figure 3.14. SERDES External Reference Clock Waveforms.....	75
Figure 3.15. sysCONFIG Parallel Port Read Cycle.....	84
Figure 3.16. sysCONFIG Parallel Port Write Cycle.....	85
Figure 3.17. sysCONFIG Slave Serial Port Timing	85
Figure 3.18. Power-On-Reset (POR) Timing	86
Figure 3.19. sysCONFIG Port Timing	86
Figure 3.20. Configuration from PROGRAMN Timing	87
Figure 3.21. Wake-Up Timing	87
Figure 3.22. Master SPI Configuration Waveforms	88
Figure 3.23. JTAG Port Timing Waveforms	89
Figure 3.24. Output Test Load, LVTTTL and LVCMOS Standards	89

Tables

Table 1.1. ECP5 and ECP5-5G Family Selection Guide	11
Table 2.1. Resources and Modes Available per Slice	14
Table 2.2. Slice Signal Descriptions	16
Table 2.3. Number of Slices Required to Implement Distributed RAM	17
Table 2.4. PLL Blocks Signal Descriptions	19
Table 2.5. DDRDLL Ports List	23
Table 2.6. sysMEM Block Configurations	25
Table 2.7. Maximum Number of Elements in a Slice	30
Table 2.8. Input Block Port Description	33
Table 2.9. Output Block Port Description	34
Table 2.10. Tristate Block Port Description	35
Table 2.11. DQSBUF Port List Description	37
Table 2.12. On-Chip Termination Options for Input Modes	40
Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support	42
Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices	43
Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support	44
Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)	46
Table 3.1. Absolute Maximum Ratings	47
Table 3.2. Recommended Operating Conditions	47
Table 3.3. Power Supply Ramp Rates	48
Table 3.4. Power-On-Reset Voltage Levels	48
Table 3.5. Hot Socketing Specifications	48
Table 3.6. Hot Socketing Requirements	49
Table 3.7. DC Electrical Characteristics	49
Table 3.8. ECP5/ECP5-5G Supply Current (Standby)	50
Table 3.9. ECP5UM	51
Table 3.10. ECP5-5G	52
Table 3.11. sysI/O Recommended Operating Conditions	53
Table 3.12. Single-Ended DC Characteristics	54
Table 3.13. LVDS	55
Table 3.14. LVDS25E DC Conditions	56
Table 3.15. BLVDS25 DC Conditions	57
Table 3.16. LVPECL33 DC Conditions	58
Table 3.17. MLVDS25 DC Conditions	59
Table 3.18. Input to SLVS	60
Table 3.19. Pin-to-Pin Performance	61
Table 3.20. Register-to-Register Performance	62
Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed	63
Table 3.22. ECP5/ECP5-5G External Switching Characteristics	64
Table 3.23. sysCLOCK PLL Timing	71
Table 3.24. Serial Output Timing and Levels	72
Table 3.25. Channel Output Jitter	72
Table 3.26. SERDES/PCS Latency Breakdown	73
Table 3.27. Serial Input Data Specifications	74
Table 3.28. Receiver Total Jitter Tolerance Specification	74
Table 3.29. External Reference Clock Specification (refclkp/refclkn)	75
Table 3.30. PCIe (2.5 Gb/s)	76
Table 3.31. PCIe (5 Gb/s)	77
Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics	79
Table 3.33. Transmit	80
Table 3.34. Receive and Jitter Tolerance	80
Table 3.35. Transmit	80

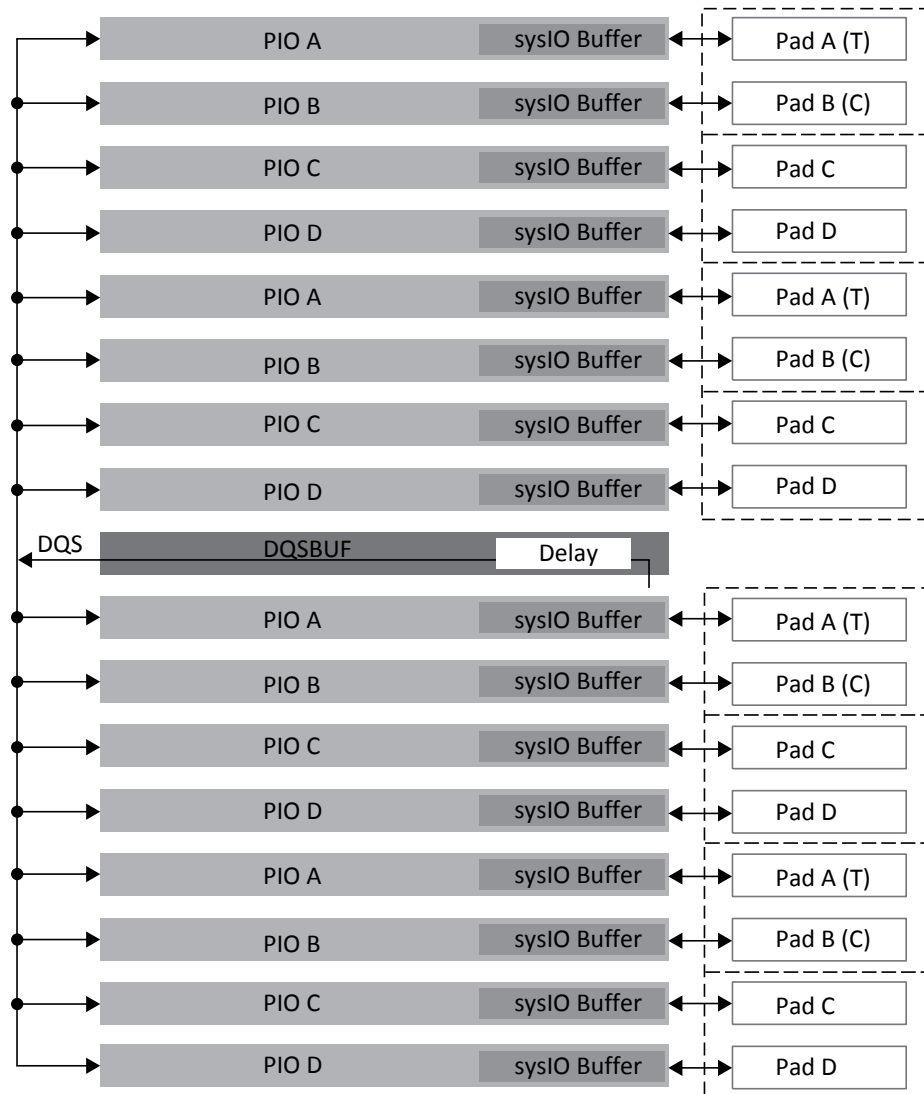


Figure 2.23. DQS Grouping on the Left and Right Edges

2.13.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR2/3, LPDDR2/3), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifted is achieved by using DQSDEL programmable delay line in the DQS Delay Block (DQS read circuit). The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block shown in [Figure 2.24](#) generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTTL, LVPECL, and MIPI.

2.14.1. sysI/O Buffer Banks

ECP5/ECP5-5G devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank (Bank 8) is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O. For LFE5-85 devices, there is an additional I/O bank (Bank 4) that is not available in other device in the family.

In ECP5/ECP5-5G devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, the banks on the Left and Right sides of the device, have voltage reference input (shared I/O pin), V_{REF1} per bank, which allow it to be completely independent of each other. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5/ECP5-5G devices, single-ended output buffers and ratioed input buffers (LVTTTL, and LVCMOS) are powered using V_{CCIO} . LVTTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

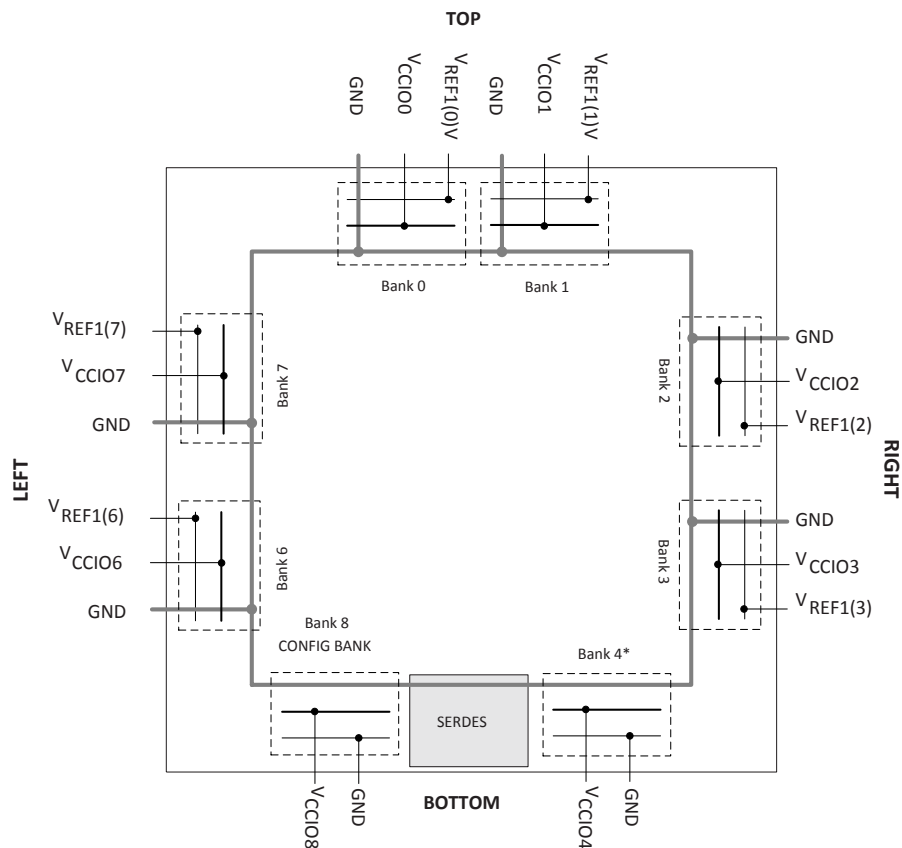


Figure 2.25. ECP5/ECP5-5G Device Family Banks

2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω , 75 Ω , or 150 Ω .
- Common mode termination of 100 Ω for differential inputs.

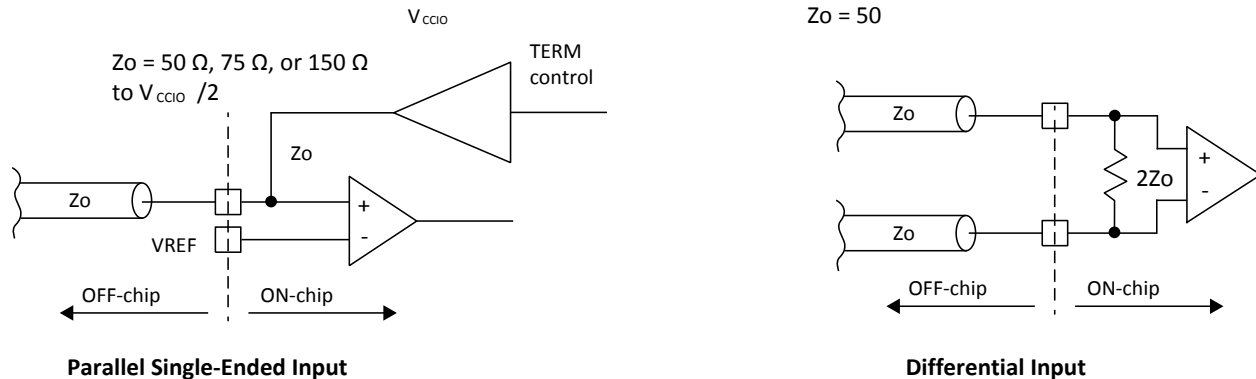


Figure 2.26. On-Chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2^*$	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Notes:**

TERMINATE to $V_{CCIO}/2$ (Single-Ended) and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance $\pm 20\%$.

Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for on-chip termination usage and value ranges.

2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the [Hot Socketing Specifications](#) section on page 48.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	−0.5	1.32	V
V _{CCA}	Supply Voltage	−0.5	1.32	V
V _{CCAUX} , V _{CCAUXA}	Supply Voltage	−0.5	2.75	V
V _{CCIO}	Supply Voltage	−0.5	3.63	V
—	Input or I/O Transient Voltage Applied	−0.5	3.63	V
V _{CCHRX} , V _{CCHTX}	SERDES RX/TX Buffer Supply Voltages	−0.5	1.32	V
—	Voltage Applied on SERDES Pins	−0.5	1.80	V
T _A	Storage Temperature (Ambient)	−65	150	°C
T _J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V _{CC} ²	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
V _{CCAUX} ^{2,4}	Auxiliary Supply Voltage	—	2.375	2.625	V
V _{CCIO} ^{2,3}	I/O Driver Supply Voltage	—	1.14	3.465	V
V _{REF} ¹	Input Reference Voltage	—	0.5	1.0	V
t _{JCOM}	Junction Temperature, Commercial Operation	—	0	85	°C
t _{JIND}	Junction Temperature, Industrial Operation	—	−40	100	°C
SERDES External Power Supply⁵					
V _{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V _{CCAUXA}	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
V _{CCHRX} ⁶	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V _{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in [Table 3.4](#) on page 48.
4. V_{CCAUX} ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
5. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to V_{cm} if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

3.7. Hot Socketing Requirements

Table 3.6. Hot Socketing Requirements

Description	Min	Typ	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA
Input current per HDIN pin when device power supply is off, inputs driven ^{1, 2}	—	—	15	mA
Current per HDIN pin when device power ramps up, input driven ³	—	—	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up ⁴	—	—	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V_{CCHTX} , 8b/10b data, no external AC coupling.
2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.
3. Device power supplies are ramping up (V_{CCA} and V_{CCAUX}), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V_{CCHTX} , 8b/10b data, internal AC coupling.
4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to V_{CCHTX} by the far end receiver termination of 50 Ω single ended.

3.8. ESD Performance

Refer to the [ECP5 and ECP5-5G Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{IL}, I_{IH}^{1, 4}$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	10	μA
$I_{IH}^{1, 3}$	Input or I/O High Leakage	$V_{CCIO} < V_{IN} \leq V_{IH(MAX)}$	—	—	100	μA
I_{PU}	I/O Active Pull-up Current, sustaining logic HIGH state	$0.7 V_{CCIO} \leq V_{IN} \leq V_{CCIO}$	–30	—	—	μA
	I/O Active Pull-up Current, pulling down from logic HIGH state	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	—	—	–150	μA
I_{PD}	I/O Active Pull-down Current, sustaining logic LOW state	$0 \leq V_{IN} \leq V_{IL(MAX)}$	30	—	—	μA
	I/O Active Pull-down Current, pulling up from logic LOW state	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	150	μA
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 \text{ to } V_{IH(MAX)}$	—	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 \text{ to } V_{IH(MAX)}$	—	5	7	pf
V_{HYST}	Hysteresis for Single-Ended Inputs	$V_{CCIO} = 3.3 V$	—	300	—	mV
		$V_{CCIO} = 2.5 V$	—	250	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, $f = 1.0$ MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as V_{REF} , maximum leakage = 25 μA .

3.13. sysI/O Single-Ended DC Electrical Characteristics

Table 3.12. Single-Ended DC Characteristics

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max (V)	V _{OH} Min (V)	I _{OL} ¹ (mA)	I _{OH} ¹ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVC MOS33	−0.3	0.8	2.0	3.465	0.4	V _{CCIO} − 0.4	16, 12, 8, 4	−16, −12, −8, −4
LVC MOS25	−0.3	0.7	1.7	3.465	0.4	V _{CCIO} − 0.4	12, 8, 4	−12, −8, −4
LVC MOS18	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	12, 8, 4	−12, −8, −4
LVC MOS15	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	8, 4	−8, −4
LVC MOS12	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	8, 4	−8, −4
LVTTL33	−0.3	0.8	2.0	3.465	0.4	V _{CCIO} − 0.4	16, 12, 8, 4	−16, −12, −8, −4
SSTL18_I (DDR2 Memory)	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	3.465	0.4	V _{CCIO} − 0.4	6.7	−6.7
SSTL18_II	−0.3	V _{REF} −	V _{REF} + 0.125	3.465	0.28	V _{CCIO} − 0.28	13.4	−13.4
SSTL15_I (DDR3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} − 0.31	7.5	−7.5
SSTL15_II (DDR3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} − 0.31	8.8	−8.8
SSTL135_I (DDR3L Memory)	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} − 0.27	7	−7
SSTL135_II (DDR3L Memory)	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} − 0.27	8	−8
MIPI D-PHY (LP) ³	−0.3	0.55	0.88	3.465	—	—	—	—
HSUL12 (LPDDR2/3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.3	V _{CCIO} − 0.3	4	−4

Notes:

1. For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O (All I/Os used in the same V_{CCIO}).
2. Not all IO types are supported in all banks. Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for details.
3. MIPI D-PHY LP input can be implemented by powering V_{CCIO} to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVC MOS12 with V_{CCIO} at 1.2V, which would meet V_{IH}/V_{IL} spec on LVC MOS12.

3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

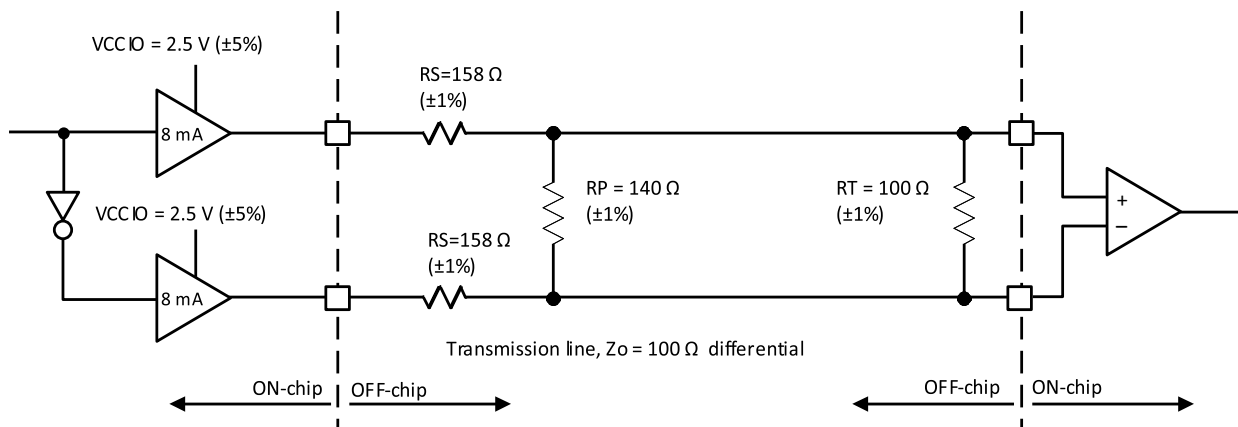


Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V _{CCIO}	Output Driver Supply (±5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (±1%)	158	Ω
R _P	Driver Parallel Resistor (±1%)	140	Ω
R _T	Receiver Termination (±1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
f _{DATA_DDR2} f _{DATA_DDR3} f _{DATA_DDR3L} f _{DATA_LPDDR2} f _{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	800	—	700	—	624	Mb/s
f _{MAX_DDR2} f _{MAX_DDR3} f _{MAX_DDR3L} f _{MAX_LPDDR2} f _{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS)									
t _{DQVBS_DDR2} t _{DQVBS_DDR3} t _{DQVBS_DDR3L} t _{DQVBS_LPDDR2} t _{DQVBS_LPDDR3}	Data Output Valid before DQS Output	All Devices	—	–0.25	—	–0.25	—	–0.25	UI
t _{DQVAS_DDR2} t _{DQVAS_DDR3} t _{DQVAS_DDR3L} t _{DQVAS_LPDDR2} t _{DQVAS_LPDDR3}	Data Output Valid after DQS Output	All Devices	0.25	—	0.25	—	0.25	—	UI
f _{DATA_DDR2} f _{DATA_DDR3} f _{DATA_DDR3L} f _{DATA_LPDDR2} f _{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	800	—	700	—	624	Mb/s
f _{MAX_DDR2} f _{MAX_DDR3} f _{MAX_DDR3L} f _{MAX_LPDDR2} f _{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz

Notes:

- Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.
- General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load.
Generic DDR timing are numbers based on LVDS I/O.
DDR2 timing numbers are based on SSTL18.
DDR3 timing numbers are based on SSTL15.
LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
- Uses LVDS I/O standard for measurements.
- Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- All numbers are generated with the Diamond software.

3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit ³
Transmit Data Latency¹							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + $\Delta 1$	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + $\Delta 1$	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + $\Delta 2$	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + $\Delta 3$	—	UI + ps
Receive Data Latency²							
R1	Equalization ON	—	—	—	$\Delta 1$	—	UI + ps
	Equalization OFF	—	—	—	$\Delta 2$	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + $\Delta 3$	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + $\Delta 3$	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. $\Delta 1 = -245$ ps, $\Delta 2 = +88$ ps, $\Delta 3 = +112$ ps.
2. $\Delta 1 = +118$ ps, $\Delta 2 = +132$ ps, $\Delta 3 = +700$ ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

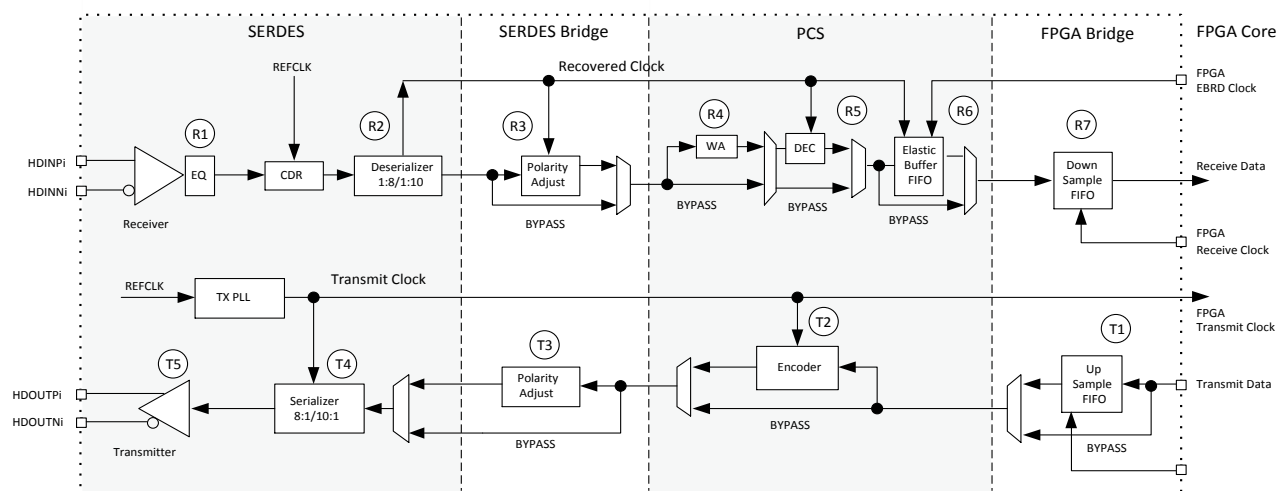


Figure 3.13. Transmitter and Receiver Latency Block Diagram

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	$V_{CCA} + 0.5^2$	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode) ²	0.1	—	$V_{CCA} + 0.2$	V
$T_{RX-RELOCK}$	SCDR re-lock time ¹	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	-20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss (without package)	—	—	-10	dB

Notes:

1. This is the typical number of bit times to re-lock to a new phase or frequency within ± 300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Notes:

1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

Table 3.31. PCIe (5 Gb/s) (Continued)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Receive^{1, 2}						
UI	Unit Interval	—	199.94	200	200.06	ps
V _{RX-DIFF-PP}	Differential Rx peak-peak voltage	—	0.34 ³	—	1.2	V, p-p
T _{RX-RJ-RMS}	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	—	—	4.2	ps, RMS
T _{RX-DJ}	Receiver deterministic jitter tolerance	—	—	—	88	ps
V _{RX-CM-AC}	Common mode noise from Rx	—	—	—		mV, p-p
R _{LRX-DIFF}	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R _{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z _{RX-DC}	Receiver DC single ended impedance	—	40	—	60	Ω
Z _{RX-HIGH-IMP-DC}	Receiver DC single ended impedance when powered down	—	200K	—	—	Ω
V _{RX-CM-AC-P}	Rx AC peak common mode voltage	—	—	—		mV, peak
V _{RX-IDLE-DET-DIFF-PP}	Electrical Idle Detect Threshold	—	65	—	340 ³	mv,
L _{RX-SKEW}	Receiver lane-lane skew	—	—	—	8	ns

Notes:

1. Values are measured at 5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express standard.

4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device Only		
P[L/R] [n-6]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n-3]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n]	A	DQS (P)
	B	DQS (N)
	C	DQ
	D	DQ
P[L/R] [n+3]	A	DQ
	B	DQ
	C	DQ
	D	DQ

Note: "n" is a row PIC number.

4.3. Pin Information Summary

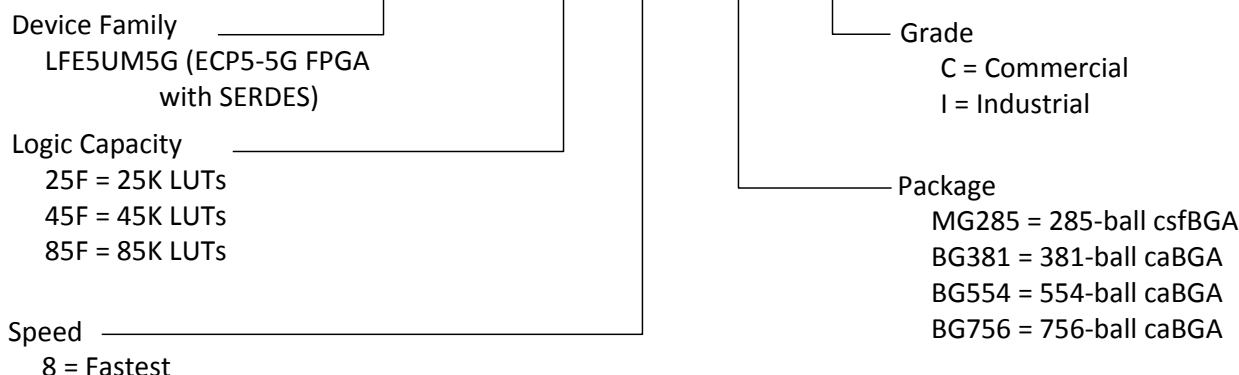
4.3.1. LFE5UM/LFE5UM5G

Pin Information Summary		LFE5UM/ LFE5UM5G-25		LFE5UM/LFE5UM5G-45			LFE5UM/LFE5UM5G-85			
Pin Type		285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA
General Purpose Inputs/Outputs per Bank	Bank 0	6	24	6	27	32	6	27	32	56
	Bank 1	6	32	6	33	40	6	33	40	48
	Bank 2	21	32	21	32	32	21	34	32	48
	Bank 3	28	32	28	33	48	28	33	48	64
	Bank 4	0	0	0	0	0	0	0	14	24
	Bank 6	26	32	26	33	48	26	33	48	64
	Bank 7	18	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13
Total Single-Ended User I/O		118	197	118	203	245	118	205	259	365
VCC		13	20	13	20	24	13	20	24	36
VCCAUX (Core)		3	4	3	4	9	3	4	9	8
VCCIO	Bank 0	1	2	1	2	3	1	2	3	4
	Bank 1	1	2	1	2	3	1	2	3	4
	Bank 2	2	3	2	3	4	2	3	4	4
	Bank 3	2	3	2	3	3	2	3	3	4
	Bank 4	0	0	0	0	0	0	0	2	2
	Bank 6	2	3	2	3	4	2	3	4	4
	Bank 7	2	3	2	3	3	2	3	3	4
	Bank 8	2	2	2	2	2	2	2	2	2

4.3.2. LFE5U

Pin Information Summary		LFE5U-12			LFE5U-25			LFE5U-45				LFE5U-85			
Pin Type		256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	554 caBGA	285 csfBGA	381 caBGA	554 caBGA	756 caBGA
General Purpose Inputs/Outputs per Bank	Bank 0	24	6	24	24	6	24	24	6	27	32	6	27	32	56
	Bank 1	32	6	32	32	6	32	32	6	33	40	6	33	40	48
	Bank 2	32	21	32	32	21	32	32	21	32	32	21	34	32	48
	Bank 3	32	28	32	32	28	32	32	28	33	48	28	33	48	64
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	14	24
	Bank 6	32	26	32	32	26	32	32	26	33	48	26	33	48	64
	Bank 7	32	18	32	32	18	32	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13	13	13	13	13	13
Total Single-Ended User		197	118	197	197	118	197	197	118	203	245	118	205	259	365
VCC		6	13	20	6	13	20	6	13	20	24	13	20	24	36
VCCAUX (Core)		2	3	4	2	3	4	2	3	4	9	3	4	9	8
VCCIO	Bank 0	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 1	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 2	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 3	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	2	2
	Bank 6	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 7	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 8	1	2	2	1	2	2	1	2	2	2	2	2	2	2
TAP		4	4	4	4	4	4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated		7	7	7	7	7	7	7	7	7	7	7	7	7	7
GND		27	123	99	27	123	99	27	123	99	198	123	99	198	267
NC		0	1	26	0	1	26	0	1	26	33	1	26	33	29
Reserved		0	4	6	0	4	6	0	4	6	12	4	6	12	12
Total Balls		256	285	381	256	285	381	256	285	381	554	285	381	554	756
High Speed Differential Input / Output Pairs	Bank 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 2	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	16/8	16/8	16/8	10/8	17/9	16/8
	Bank 3	16/8	14/7	16/8	16/8	14/7	16/8	16/8	14/7	16/8	24/12	14/7	16/8	24/1	
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 5	16/8	13/6	16/8	16/8	13/6	16/8	16/8	13/6	16/8	24/12	13/6	16/8	24/1	
	Bank 6	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8	
	Bank 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Total High Speed		64/32	45/27	64/32	64/32	45/27	64/32	64/32	45/27	64/32	80/40	45/27	65/33	80/40	112/
DQS Groups (> 11 pins in group)	Bank 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 2	2	1	2	2	1	2	2	1	2	2	2	1	2	2
	Bank 3	2	2	2	2	2	2	2	2	2	2	3	2	2	3
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 5	2	2	2	2	2	2	2	2	2	2	3	2	2	3
	Bank 6	2	1	2	2	1	2	2	1	2	2	2	1	2	2
	Bank 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Total DQS Groups		8	6	8	8	6	8	8	6	8	10	6	8	10	14

LFE5UM5G - XX - X XXXXX X



5.2. Ordering Part Numbers

5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	-6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	-7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	-8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	-6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	-7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	-8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	-6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	-7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	-8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	-6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	-7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	-8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	-6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	-7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	-8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	No

Revision History

Date	Version	Section	Change Summary
March 2018	1.9	All	Updated formatting and page referencing.
		General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide . Added caBGA256 package in LFE5U-45.
		Architecture	Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support . Updated footnote #1.
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions .
			Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics .
			Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) .
			Updated Table 3.11. sys/O Recommended Operating Conditions .
			Updated Table 3.12. Single-Ended DC Characteristics .
			Updated Table 3.13. LVDS .
			Updated Table 3.14. LVDS25E DC Conditions .
			Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed .
			Updated Table 3.28. Receiver Total Jitter Tolerance Specification .
			Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics .
			Updated header name of section 3.29 Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics .
		Pinout Information	Updated table in section 4.3.2 LFE5U .
		Ordering Information	Added table rows in 5.2.1 Commercial .
			Added table rows in 5.2.2 Industrial .
		Supplemental Information	Updated For Further Information section.
November 2017	1.8	General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide . Added caBGA256 package in LFE5U-12 and LFE5U-25.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclk).
			Modified section heading to XXAU/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.