Lattice Semiconductor Corporation - LFE5U-25F-6BG381C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-25f-6bg381c

Figures

Tables

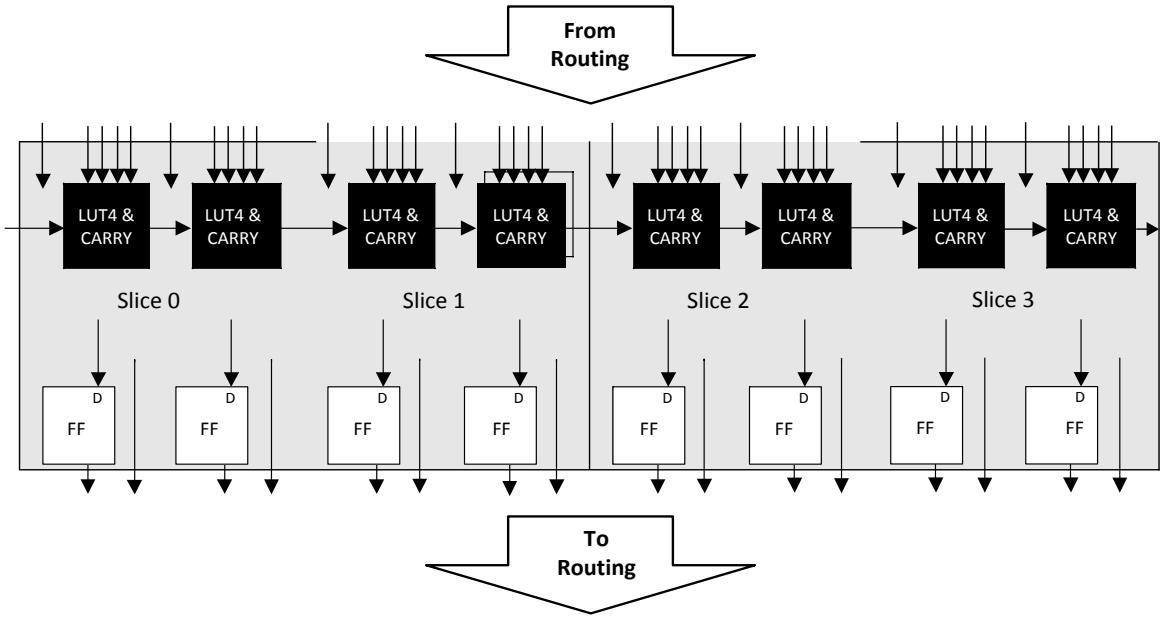


Figure 2.2. PFU Diagram

2.2.1. Slice

Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals, 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are five outputs, four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/ PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7 and LUT8. Table 2.2 and Figure 2.3 list the signals associated with all the slices. Figure 2.4 on page 16 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7 and LUT8.

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

2.8.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.8.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.8.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.8.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- **Read-Before-Write** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note**: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

2.11. PIO

The PIO contains three blocks: an input register block, output register block, and tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

2.11.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers to shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers samples the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The top side of the device supports IDDRX1 gearing function. For more information on gearing function, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

Figure 2.17 shows the input register block for the PIOs on the top edge.

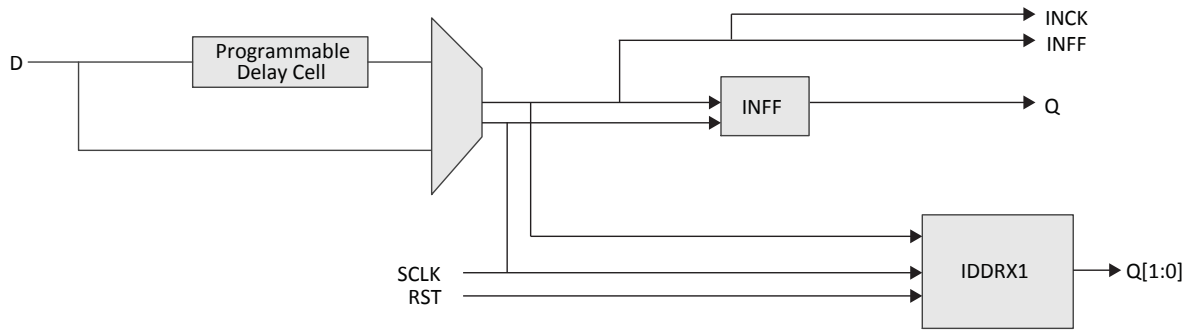
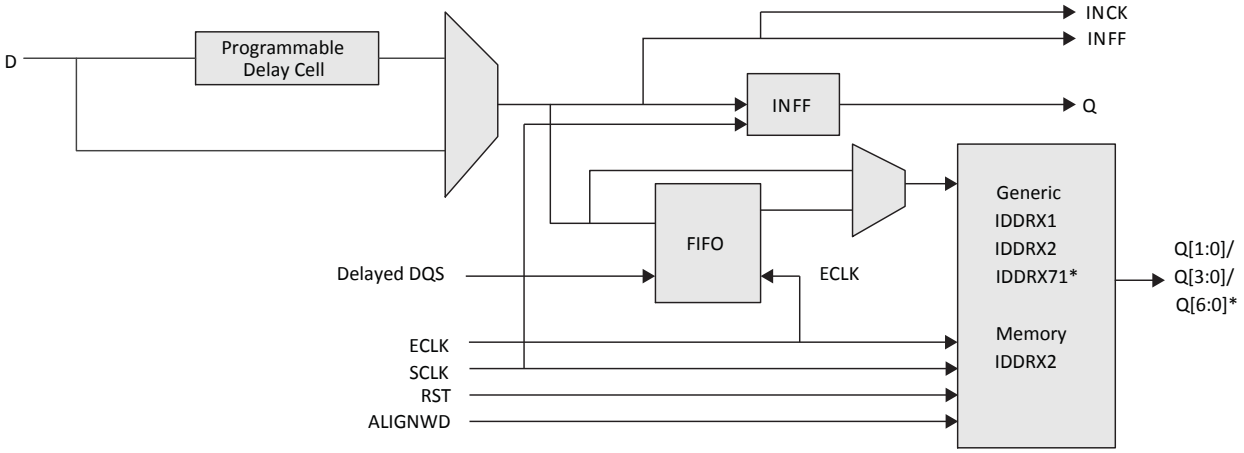


Figure 2.17. Input Register Block for PIO on Top Side of the Device

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

Figure 2.18. Input Register Block for PIO on Left and Right Side of the Device

2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.

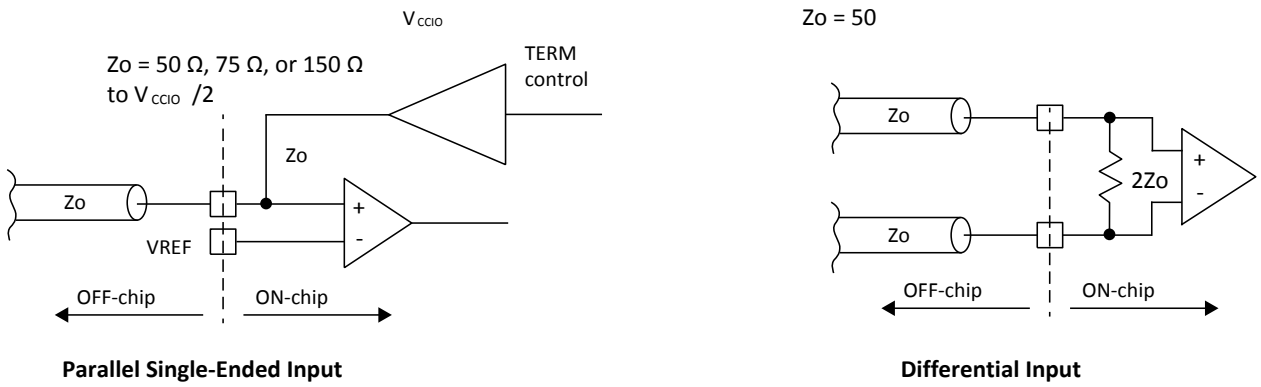


Figure 2.26. On-Chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2$*	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Notes**:

TERMINATE to $V_{CCIO}/2$ (Single-Ended) and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance ±20%.

Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for on-chip termination usage and value ranges.

2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the Hot Socketing Specifications section on page 48.

Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).

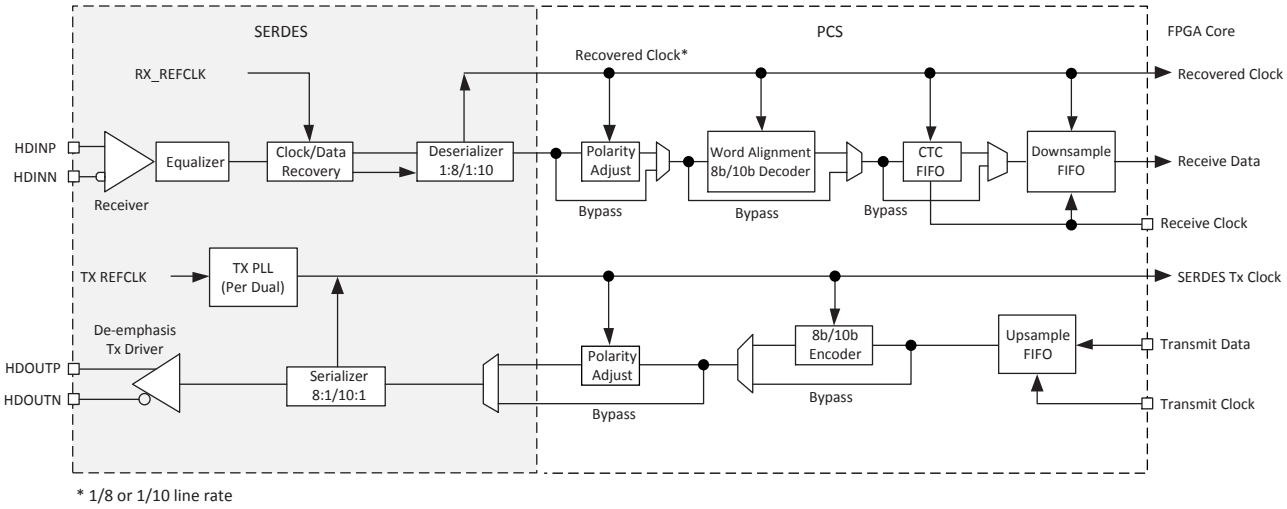


Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter			Min	Typ	Max	Unit
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC}, and V_{CCAUX}	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIOs} do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC}, V_{CCAUX}, and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash.

For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA}, before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \le V_{IN} \le V_{IH}$ (Max)	—	—	±1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \le V_{IN} < V_{CCIO}$	—	—	±1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5$ V	—	18	—	mA

Notes:

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ±1 mA.

3.14. sysI/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.13. LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	±100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	±10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver outputs shorted to each other	—	—	12	mA

Note: On the left and right sides of the device, this specification is valid only for V_{CCIO} = 2.5 V or 3.3 V.

3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

3.14.7. **MLVDS25**

The ECP5/ECP5-5G devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.

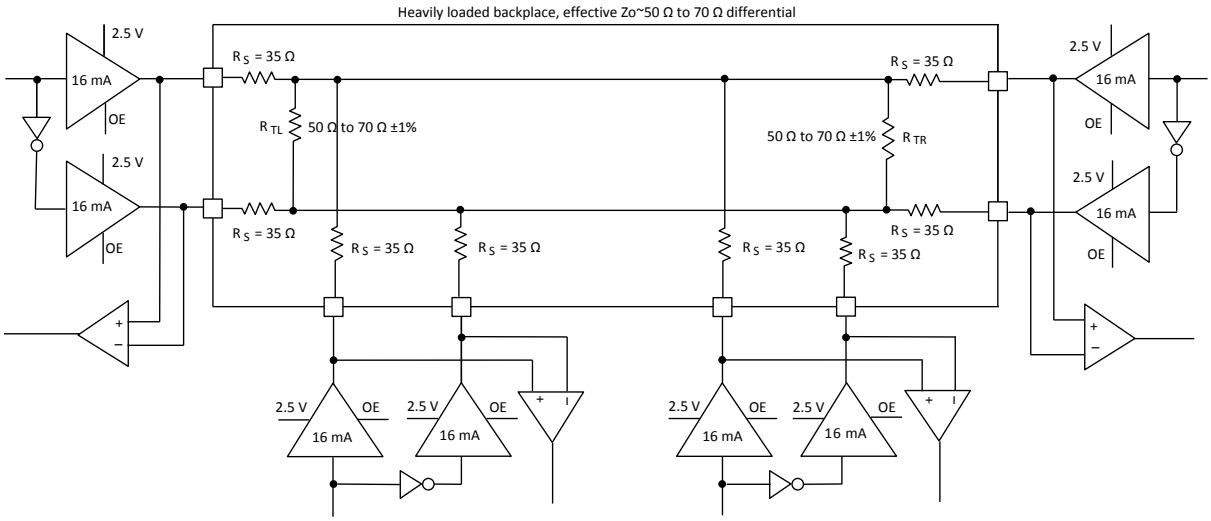


Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Table 3.17. MLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo=50 Ω	Zo=70 Ω	
V_{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (±1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (±1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

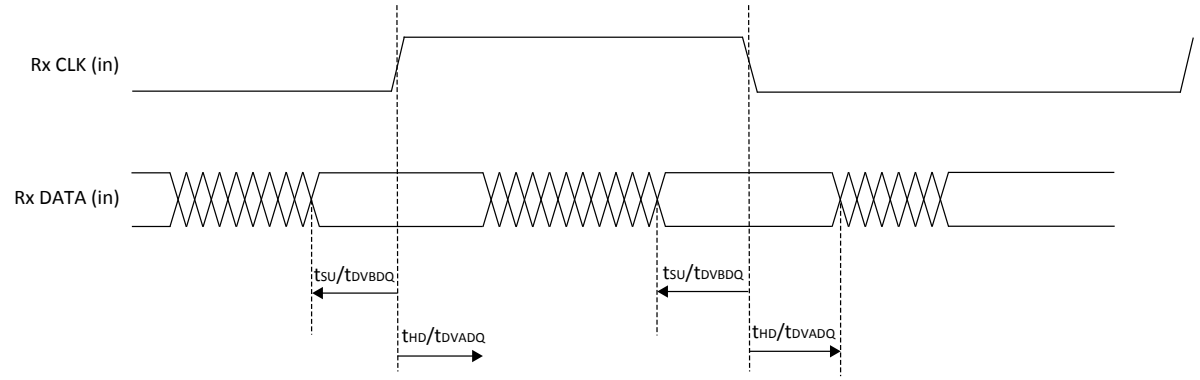


Figure 3.6. Receiver RX.CLK.Centered Waveforms

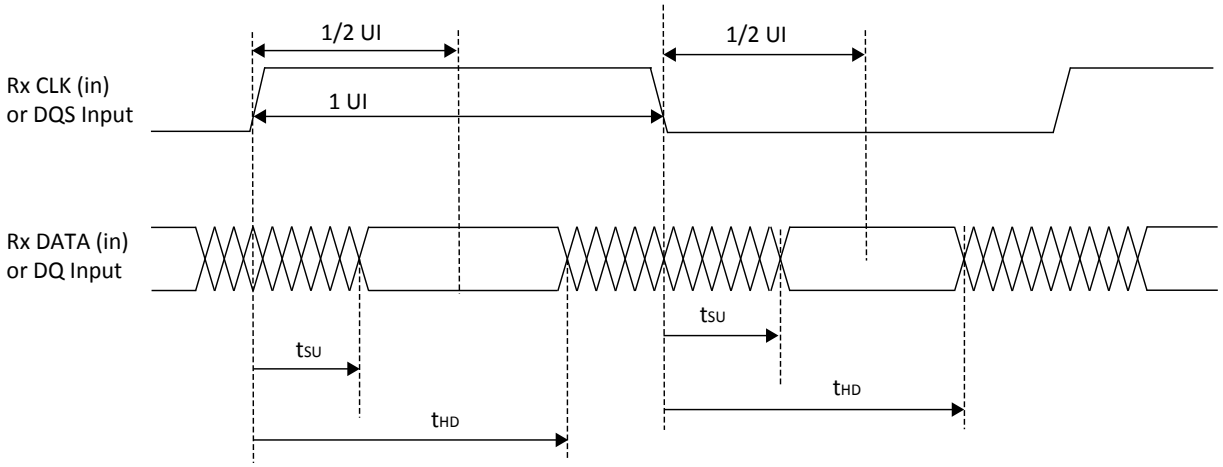


Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

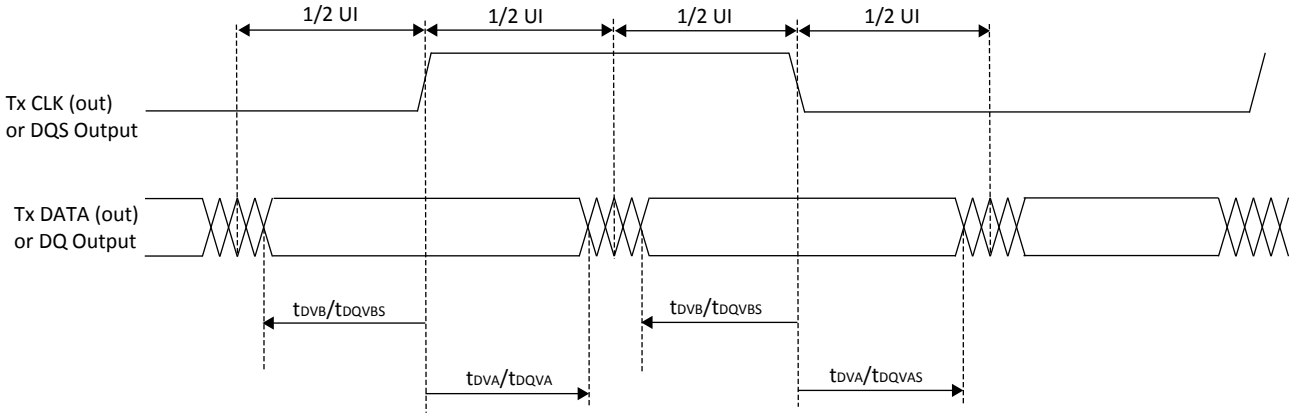


Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 3.23. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
f_{VCO}	PLL VCO Frequency	—	400	800	MHz
f_{PFD}[3]	Phase Detector Input Frequency	—	10	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_W	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
t_{LOCK}[2]	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST/ Pulse Width	—	1	—	ms
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{LOAD_REG}	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain “0” or	—	4	—	VCO cycles

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

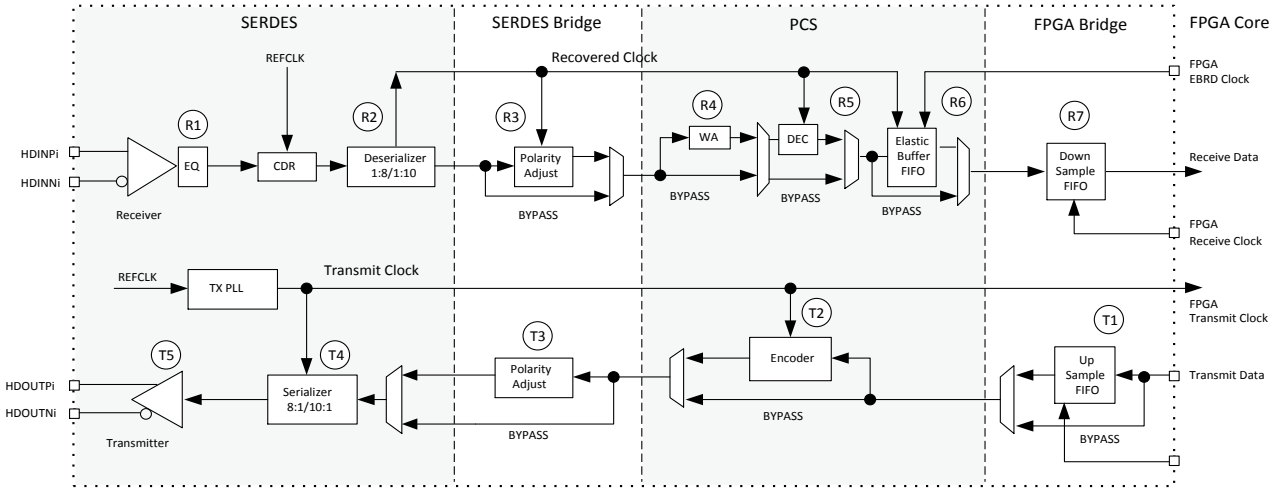


Figure 3.13. Transmitter and Receiver Latency Block Diagram

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss (without package)	—	—	–10	dB

Notes:
1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

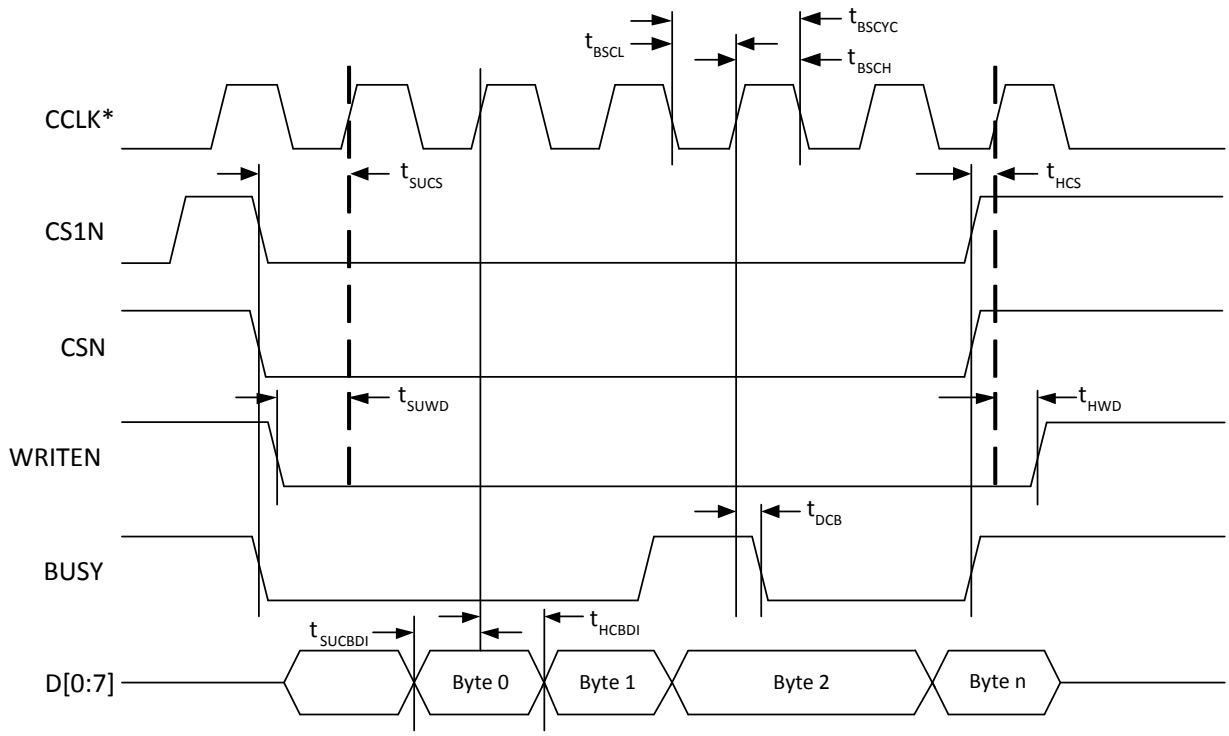
3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Notes:
1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.



*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3.16. sysCONFIG Parallel Port Write Cycle

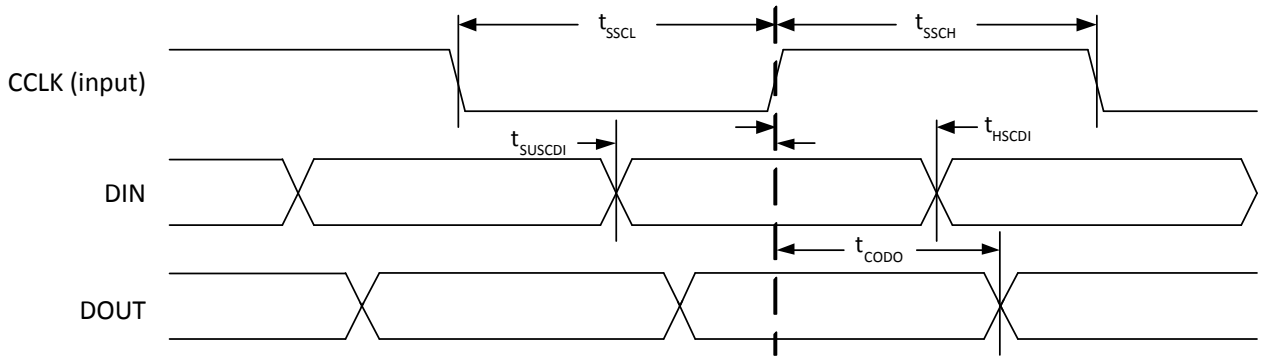


Figure 3.17. sysCONFIG Slave Serial Port Timing

Revision History

Date	Version	Section	Change Summary
March 2018	1.9	All	Updated formatting and page referencing.
		General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-45.
		Architecture	Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support. Updated footnote #1.
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions.
			Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics.
			Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby).
			Updated Table 3.11. sysI/O Recommended Operating Conditions.
			Updated Table 3.12. Single-Ended DC Characteristics.
			Updated Table 3.13. LVDS.
			Updated Table 3.14. LVDS25E DC Conditions.
			Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed.
			Updated Table 3.28. Receiver Total Jitter Tolerance Specification.
			Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics.
			Updated header name of section 3.29 Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics
		Pinout Information	Updated table in section 4.3.2 LFE5U.
		Ordering Information	Added table rows in 5.2.1 Commercial.
			Added table rows in 5.2.2 Industrial.
		Supplemental Information	Updated For Further Information section.
November 2017	1.8	General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-12 and LFE5U-25.

(Continued)

Date	Version	Section	Change Summary
November 2015	1.5	All	Added ECP5-5G device family.
			Changed document title to ECP5 and ECP5-5G Family Data Sheet.
	1.4	General Description	Updated Features section. Added support for eDP in RDR and HDR.
		Architecture	Updated Overview section. Revised Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level). Modified Flexible sysIO description and Note.
			Updated SERDES and Physical Coding Sublayer section. • Changed E.24.V in CPRI protocol to E.24.LV. • Removed "1.1 V" from paragraph on unused Dual.
		DC and Switching Characteristics	Updated Hot Socketing Requirements section. Revised V_{CCHTX} in table notes 1 and 3. Indicated V_{CCHTX} in table note 4.
			Updated SERDES High-Speed Data Transmitter section. Revised V_{CCHTX} in table note 1.
		Ordering Information	Updated ECP5/ECP5-5G Part Number Description section. Changed "LFE5 FPGA" under Device Family to "ECP5 FPGA".
August 2015	1.3	General Description	Updated Features section. • Removed SMPTE3G under Embedded SERDES. • Added Single Event Upset (SEU) Mitigation Support. Removed SMPTE protocol in fifth paragraph.
		Architecture	General update.
		DC and Switching Characteristics	General update.
		Pinout Information	Updated Signal Descriptions section. Revised the descriptions of the following signals: • P[L/R] [Group Number]_[A/B/C/D] • P[T/B][Group Number]_[A/B] • D4/IO4 (Previously named D4/MOSI2/IO4) • D5/IO5 (Previously named D5/MISO/IO5) • VCCHRX_D[dual_num]CH[chan_num] • VCCHTX_D[dual_num]CH[chan_num]
		Supplemental Information	Added TN1184 reference.