Lattice Semiconductor Corporation - LFE5U-25F-6MG285C Datasheet

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-25f-6mg285c

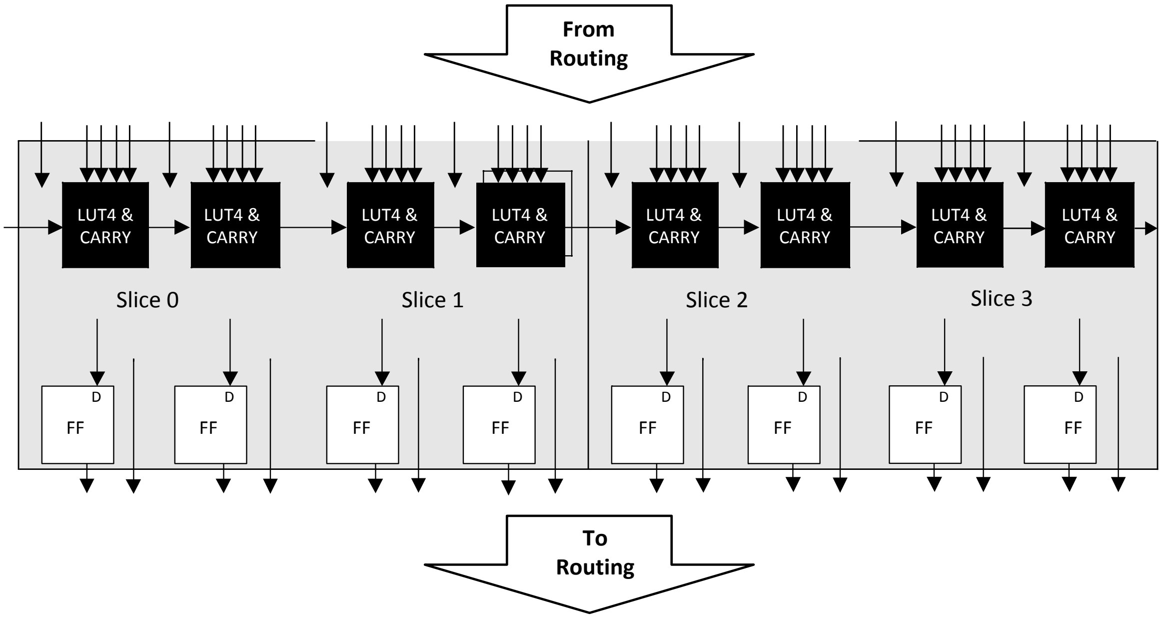


Figure 2.2. PFU Diagram

2.2.1. Slice

Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals, 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are five outputs, four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/ PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7 and LUT8. Table 2.2 and Figure 2.3 list the signals associated with all the slices. Figure 2.4 on page 16 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7 and LUT8.

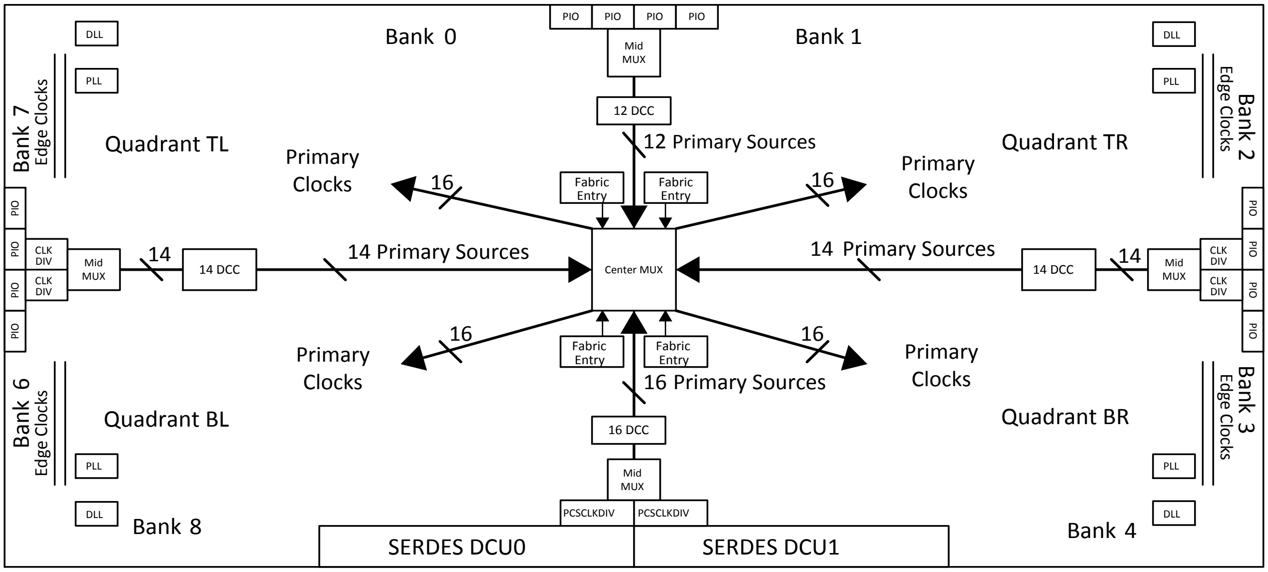


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

2.8.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.8.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.8.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.8.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- **Read-Before-Write** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

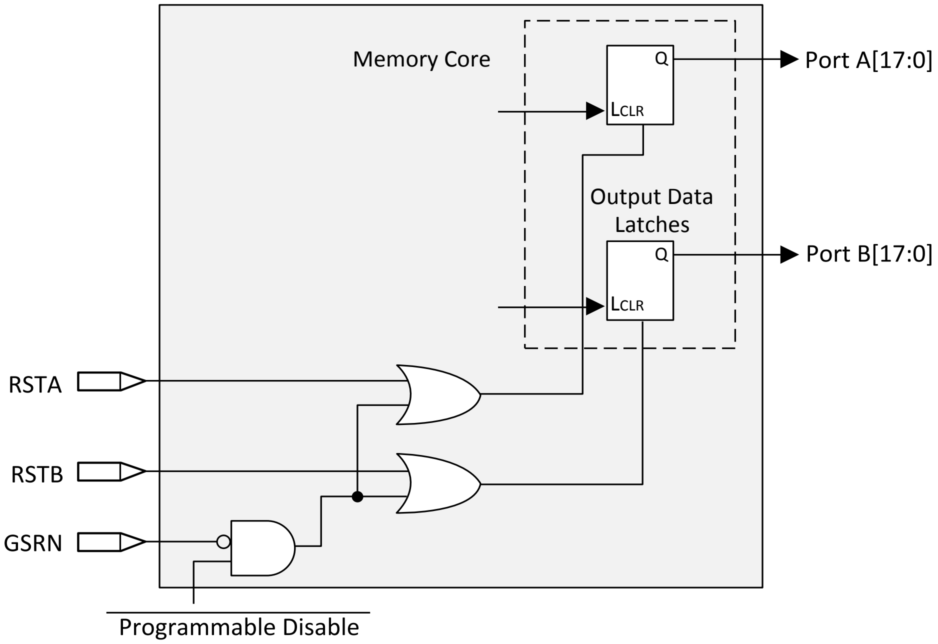


Figure 2.12. Memory Core Reset

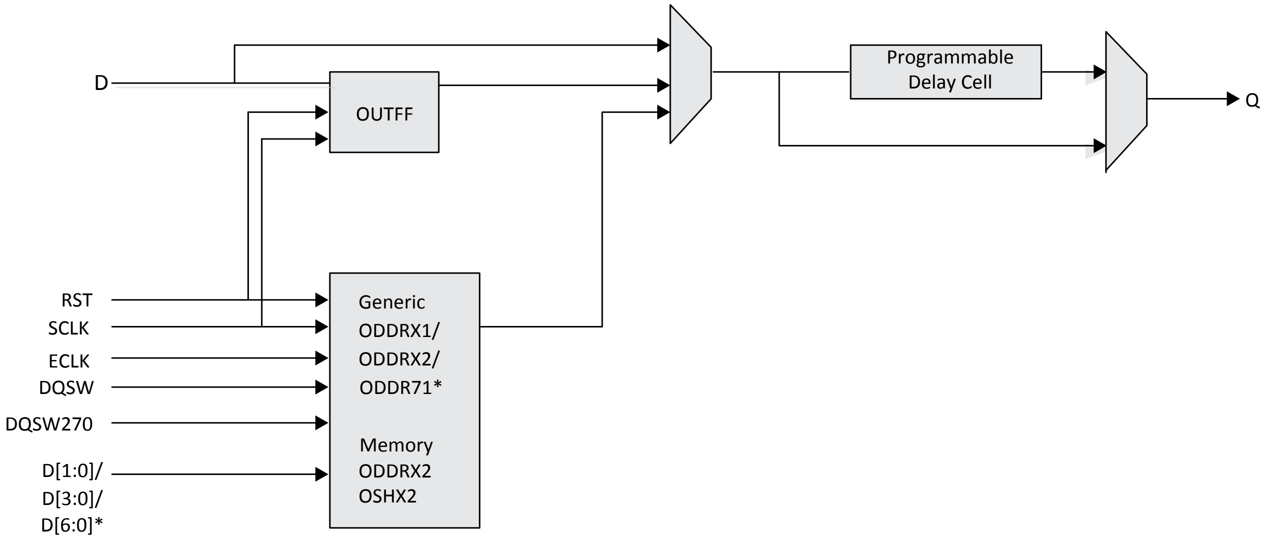
For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

2.9. sysDSP™ Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

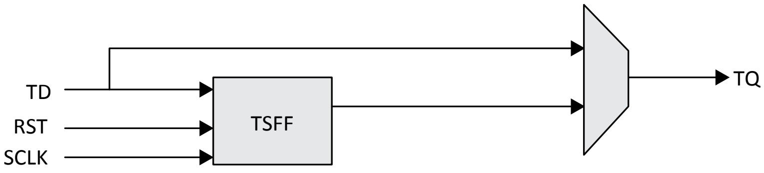
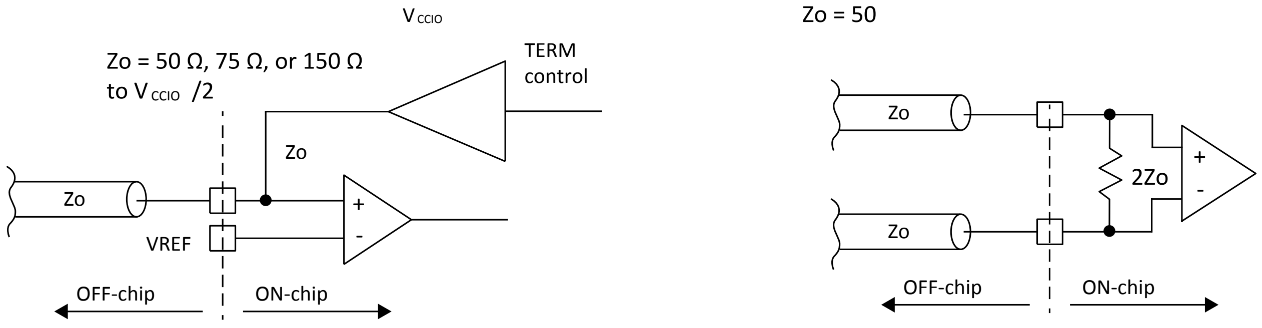


Figure 2.21. Tristate Register Block on Top Side

2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.



Parallel Single-Ended Input

Differential Input

Figure 2.26. On-Chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to V_{CCIO}/2*	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Notes**:

TERMINATE to V_{CCIO}/2 (Single-Ended) and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to V_{CCIO}/2 and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance ±20%.

Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for on-chip termination usage and value ranges.

2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the Hot Socketing Specifications section on page 48.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter			Min	Typ	Max	Unit
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC}, and V_{CCAUX}	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIOs} do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC}, V_{CCAUX}, and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash.

For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA}, before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \leq V_{IN} \leq V_{IH}$ (Max)	—	—	±1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \leq V_{IN} < V_{CCIO}$	—	—	±1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5$ V	—	18	—	mA

Notes:

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ±1 mA.

3.7. Hot Socketing Requirements

Table 3.6. Hot Socketing Requirements

Description	Min	Typ	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA
Input current per HDIN pin when device power supply is off, inputs driven[1, 2]	—	—	15	mA
Current per HDIN pin when device power ramps up, input driven[3]	—	—	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up[4]	—	—	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, no external AC coupling.
2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.
3. Device power supplies are ramping up (V_{CCA} and V_{CCAUX}), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, internal AC coupling.
4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to V_{CCHTX} by the far end receiver termination of 50 Ω single ended.

3.8. ESD Performance

Refer to the ECP5 and ECP5-5G Product Family Qualification Summary for complete qualification data, including ESD performance.

3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4]	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	$V_{CCIO} < V_{IN} \le V_{IH(MAX)}$	—	—	100	µA
I_{PU}	I/O Active Pull-up Current, sustaining logic HIGH state	$0.7\ V_{CCIO} \le V_{IN} \le V_{CCIO}$	–30	—	—	µA
	I/O Active Pull-up Current, pulling down from logic HIGH state	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	—	—	–150	µA
I_{PD}	I/O Active Pull-down Current, sustaining logic LOW state	$0 \le V_{IN} \le V_{IL}$ (MAX)	30	—	—	µA
	I/O Active Pull-down Current, pulling up from logic LOW state	$0 \le V_{IN} \le V_{CCIO}$	—	—	150	µA
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to $V_{IH(MAX)}$	—	5	8	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to $V_{IH(MAX)}$	—	5	7	pf
V_{HYST}	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V	—	300	—	mV
		V_{CCIO} = 2.5 V	—	250	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as V_{REF}, maximum leakage= 25 µA.

3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

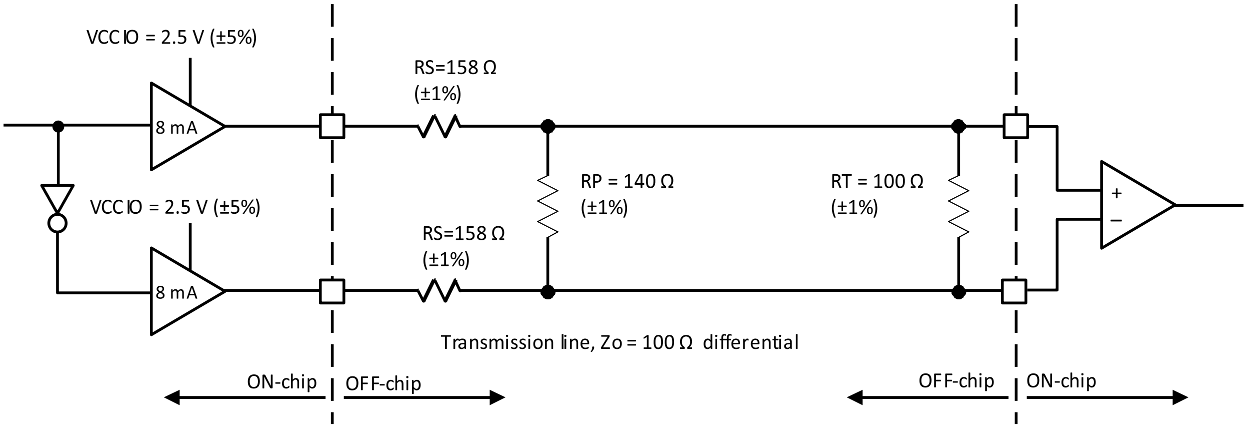


Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (±1%)	158	Ω
R_P	Driver Parallel Resistor (±1%)	140	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.14.6. LVPECL33

The ECP5/ECP5-5G devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.3 is one possible solution for point-to-point signals.

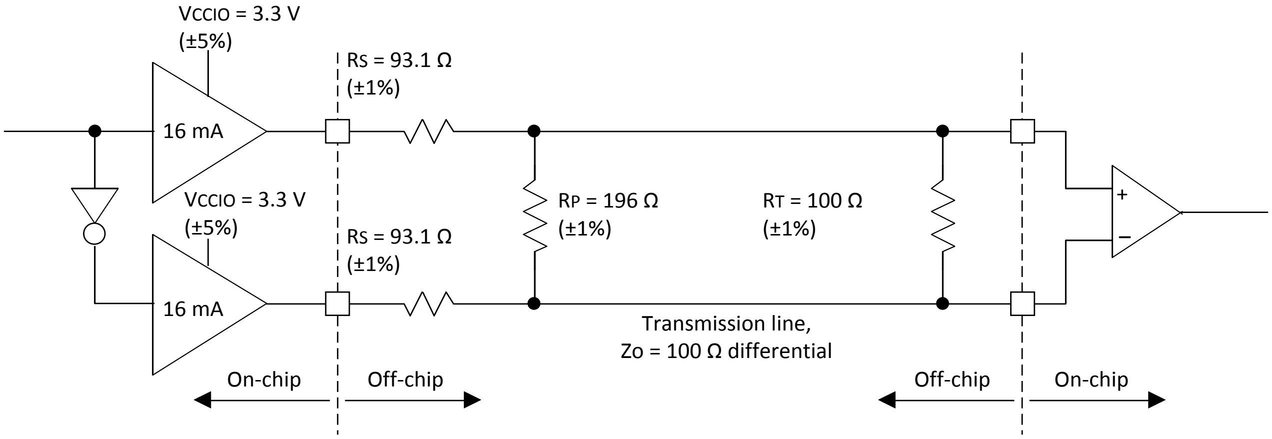


Figure 3.3. Differential LVPECL33

Over recommended operating conditions.

Table 3.16. LVPECL33 DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (±1%)	93	Ω
R_P	Driver Parallel Resistor (±1%)	196	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

Table 3.18. Input to SLVS

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.

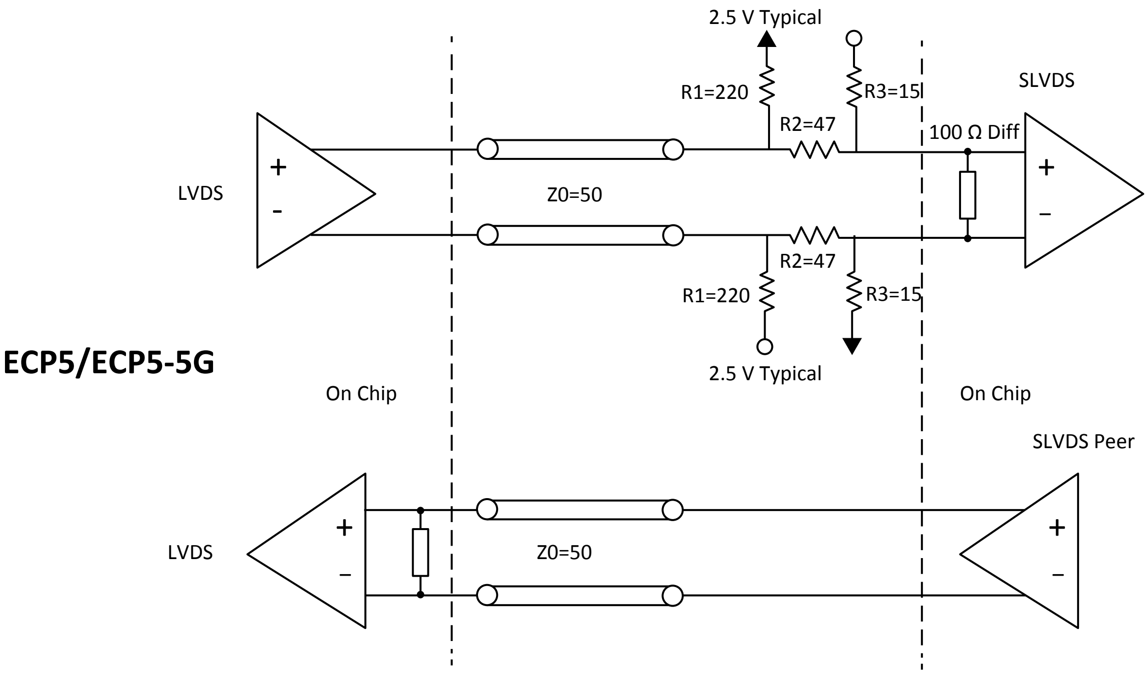


Figure 3.5. SLVS Interface

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
Generic DDR Input									
Generic DDRX1 Inputs With Clock and Data Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{SU\_GDDRX1\_centered}$	Data Setup Before CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$t_{HD\_GDDRX1\_centered}$	Data Hold After CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs With Clock and Data Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.7									
$t_{SU\_GDDRX1\_aligned}$	Data Setup from CLK Input	All Devices	—	–0.55	—	–0.55	—	–0.55	ns + 1/2 UI
$t_{HD\_GDDRX1\_aligned}$	Data Hold from CLK Input	All Devices	0.55	—	0.55	—	0.55	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Inputs With Clock and Data Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.6									
$t_{SU\_GDDRX2\_centered}$	Data Setup before CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$t_{HD\_GDDRX2\_centered}$	Data Hold after CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Inputs With Clock and Data Aligned at Pin (GDDRX2_RX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.7									
$t_{SU\_GDDRX2\_aligned}$	Data Setup from CLK Input	All Devices	—	–0.344	—	–0.42	—	-0.495	ns + 1/2 UI
$t_{HD\_GDDRX2\_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	—	0.495	—	ns + 1/2 UI
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Inputs With Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) Using PLL Clock Input, Left and Right sides Only Figure 3.11									
$t_{SU\_LVDS71\_i}$	Data Setup from CLK Input (bit i)	All Devices	—	–0.271	—	–0.39	—	–0.41	ns+(1/2+i) * UI
$t_{HD\_LVDS71\_i}$	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	—	0.41	—	ns+(1/2+i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz

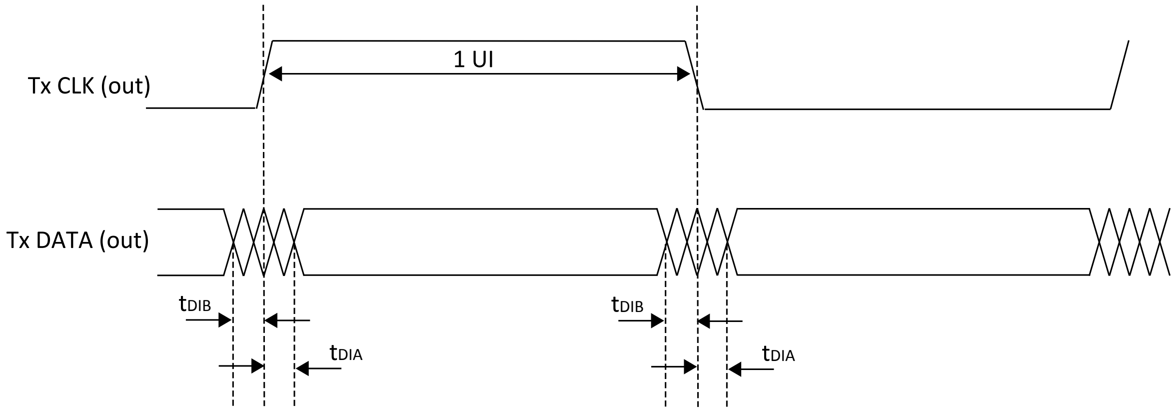
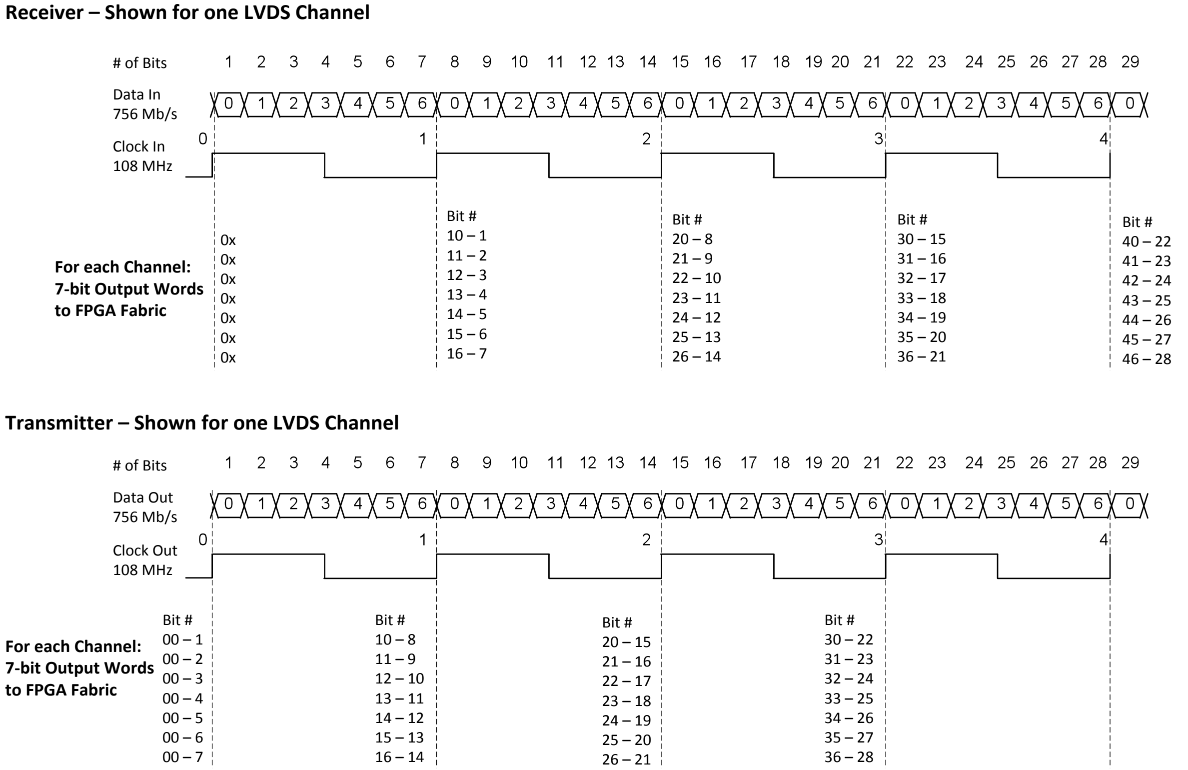


Figure 3.9. Transmit TX.CLK.Aligned Waveforms


Receiver – Shown for one LVDS Channel

Transmitter – Shown for one LVDS Channel

Figure 3.10. DDRX71 Video Timing Waveforms

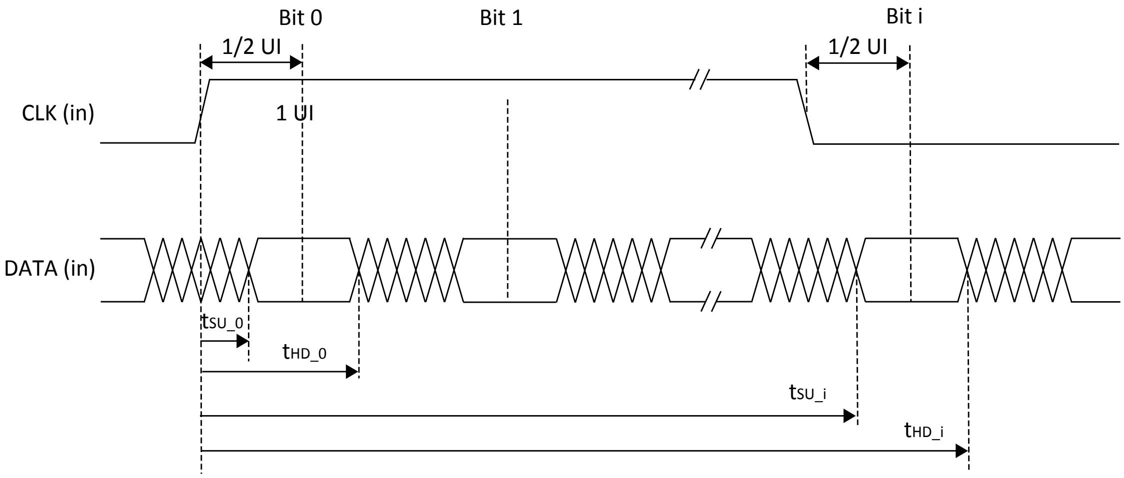


Figure 3.11. Receiver DDRX71_RX Waveforms

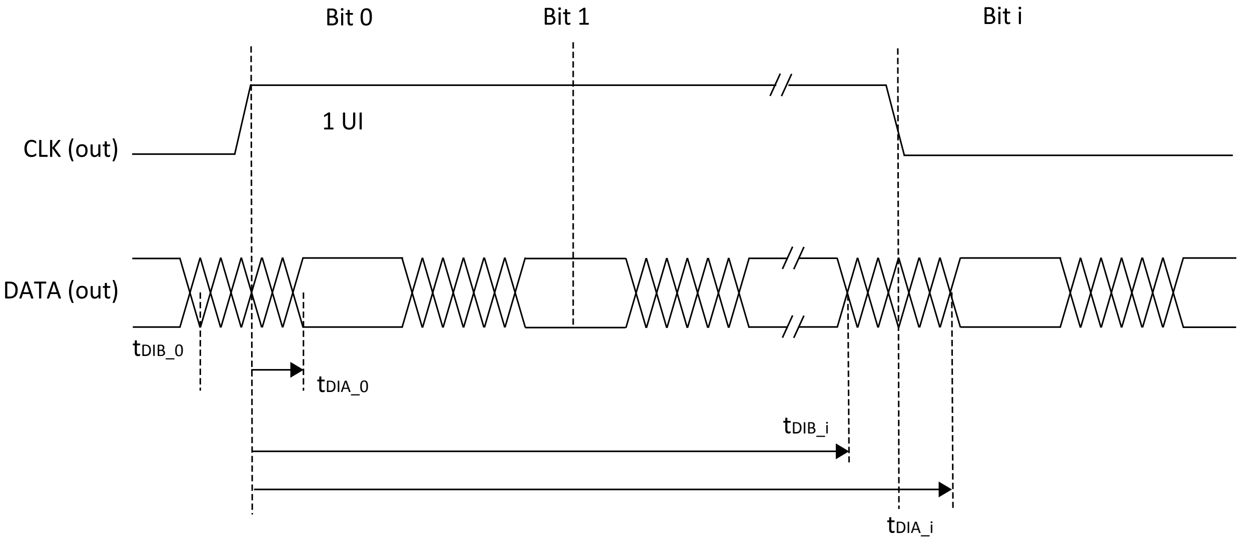


Figure 3.12. Transmitter DDRX71_TX Waveforms

Table 3.31. PCIe (5 Gb/s) *(Continued)*

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Receive[1, 2]						
UI	Unit Interval	—	199.94	200	200.06	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	0.34[3]	—	1.2	V, p-p
$T_{RX-RJ-RMS}$	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	—	—	4.2	ps, RMS
T_{RX-DJ}	Receiver deterministic jitter tolerance	—	—	—	88	ps
$V_{RX-CM-AC}$	Common mode noise from Rx	—	—	—		mV, p-p
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z_{RX-DC}	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Receiver DC single ended impedance when powered down	—	200K	—	—	Ω
$V_{RX-CM-AC-P}$	Rx AC peak common mode voltage	—	—	—		mV, peak
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect Threshold	—	65	—	340[3]	mv,
$L_{RX-SKEW}$	Receiver lane-lane skew	—	—	—	8	ns

Notes:

1. Values are measured at 5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express standard.

Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) *(Continued)*		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin
SERDES Function		
VCCAx	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCAx = 1.1 V for ECP5, VCCAx = 1.2 V for ECP5-5G.
VCCAUXAx	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUXAx = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes

5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	–6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	–7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	–8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	–6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	–7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	–8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	–6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	–7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	–8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	–6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	–7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	–8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	–6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	–7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	–8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	No