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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-25f-7bg381i

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1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

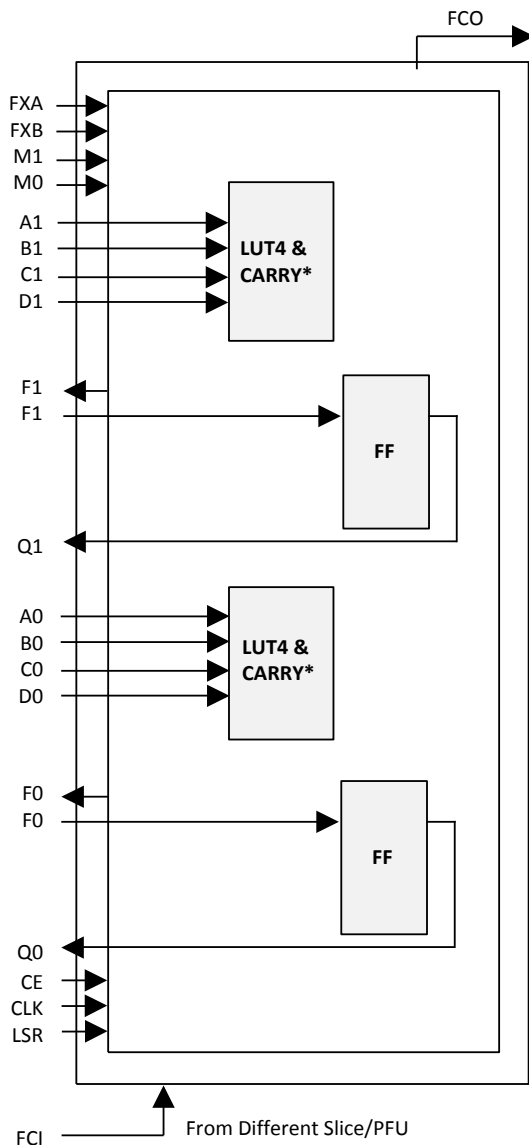
The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
 - 12K to 84K LUTs
 - 197 to 365 user programmable I/Os
- Embedded SERDES
 - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
 - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
 - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
 - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
 - Fully cascadable slice architecture
 - 12 to 160 slices for high performance multiply and accumulate
 - Powerful 54-bit ALU operations
 - Time Division Multiplexing MAC Sharing
 - Rounding and truncation
 - Each slice supports
 - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
 - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
 - Up to 3.744 Mb sysMEM™ Embedded Block RAM (EBR)
 - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

WCK is CLK

WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2

WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

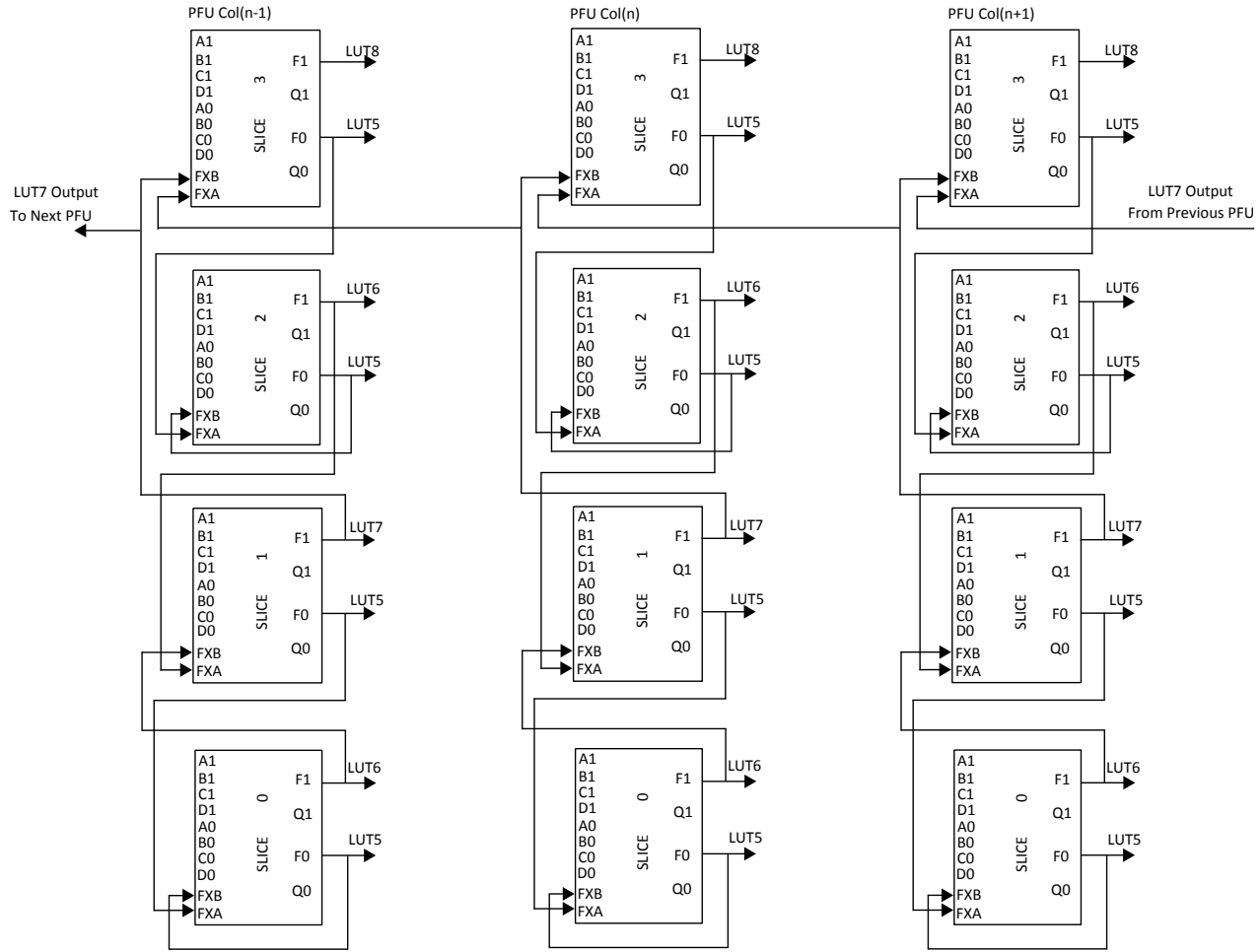


Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output ¹

Notes:

1. See [Figure 2.3](#) on page 15 for connection details.
2. Requires two adjacent PFUs.

2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

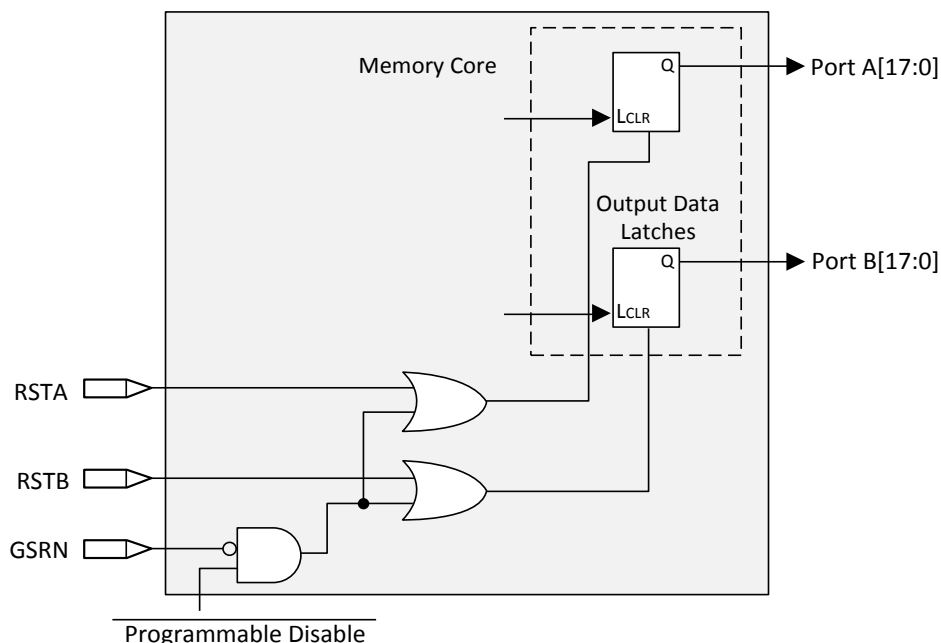


Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in [Supplemental Information](#) section on page 102.

2.9. sysDSP™ Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in [DDR Memory Support](#) section on page 35.

Table 2.8. Input Block Port Description

Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in [Figure 2.19](#). The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

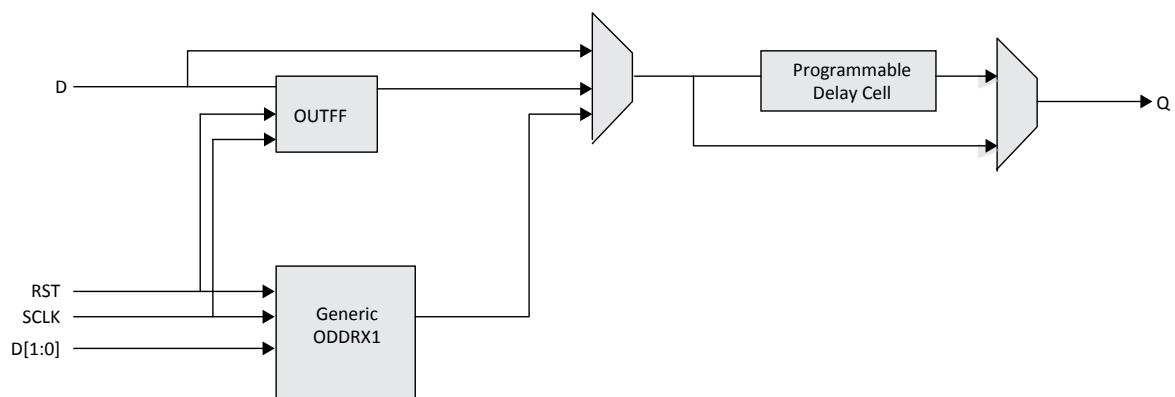


Figure 2.19. Output Register Block on Top Side

2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. [Figure 2.27](#) shows the position of the dual blocks for the LFE5-85. [Table 2.13](#) shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. [Figure 2.28](#) shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Figure 10: SERDES and PCS Block Diagram. The diagram illustrates the data flow and clock management between the SERDES, PCS, and FPGA Core.

SERDES Section:

- Receiver Path:** HDINP and HDINN inputs feed into a Receiver block. The output goes through an Equalizer, then a Clock/Data Recovery block, and finally a Deserializer (1:8/1:10). The RX_REFCLK input is connected to the Clock/Data Recovery block.
- Transmitter Path:** HDOUTP and HDOUTN inputs feed into a De-emphasis Tx Driver. The output goes through a TX PLL (Per Dual), then a Serializer (8:1/10:1), and finally a Driver. The TX_REFCLK input is connected to the TX PLL.

PCS Section:

- Recovered Clock*:** This clock signal is distributed to the Deserializer, the Polarity Adjust block, the Word Alignment 8b/10b Decoder, the CTC FIFO, and the Downsample FIFO.
- Receiver Path (Continued):** The output of the Deserializer goes through a Polarity Adjust block, a Word Alignment 8b/10b Decoder, a CTC FIFO, and a Downsample FIFO. Bypass blocks are provided for the Polarity Adjust, Word Alignment 8b/10b Decoder, and CTC FIFO.
- Transmitter Path (Continued):** The output of the Serializer goes through a Polarity Adjust block, an 8b/10b Encoder, and an Upsample FIFO. Bypass blocks are provided for the Polarity Adjust and 8b/10b Encoder.

FPGA Core Section:

- Recovered Clock:** Output from the Recovered Clock* input.
- Receive Data:** Output from the Downsample FIFO.
- Receive Clock:** Input to the Downsample FIFO.
- SERDES Tx Clock:** Output from the TX PLL.
- Transmit Data:** Input to the Upsample FIFO.
- Transmit Clock:** Input to the Upsample FIFO.

* 1/8 or 1/10 line rate

Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for more information.

Table 3.10. ECP5-5G

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I _{CCA-SB}	V _{CCA} Power Supply Current (Per Channel)	4	9.5	mA
I _{CCHRX-SB} ⁴	V _{CCHRX} , Input Buffer Current (Per Channel)	—	0.1	mA
I _{CCHTX-SB}	V _{CCHTX} , Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 5 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	58	67	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 3.2 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	48	57	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	44	53	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	36	46	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	30	40	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For I_{CCHRX-SB}, during Standby, input termination on Rx are disabled.
5. For I_{CCHRX-OP}, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

3.13. sysI/O Single-Ended DC Electrical Characteristics

Table 3.12. Single-Ended DC Characteristics

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max (V)	V _{OH} Min (V)	I _{OL} ¹ (mA)	I _{OH} ¹ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCN0533	−0.3	0.8	2.0	3.465	0.4	V _{CCIO} − 0.4	16, 12, 8, 4	−16, −12, −8, −4
LVCN0525	−0.3	0.7	1.7	3.465	0.4	V _{CCIO} − 0.4	12, 8, 4	−12, −8, −4
LVCN0518	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	12, 8, 4	−12, −8, −4
LVCN0515	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	8, 4	−8, −4
LVCN0512	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	8, 4	−8, −4
LVTTL33	−0.3	0.8	2.0	3.465	0.4	V _{CCIO} − 0.4	16, 12, 8, 4	−16, −12, −8, −4
SSTL18_I (DDR2 Memory)	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	3.465	0.4	V _{CCIO} − 0.4	6.7	−6.7
SSTL18_II	−0.3	V _{REF} −	V _{REF} + 0.125	3.465	0.28	V _{CCIO} − 0.28	13.4	−13.4
SSTL15_I (DDR3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} − 0.31	7.5	−7.5
SSTL15_II (DDR3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} − 0.31	8.8	−8.8
SSTL135_I (DDR3L Memory)	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} − 0.27	7	−7
SSTL135_II (DDR3L Memory)	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} − 0.27	8	−8
MIPI D-PHY (LP) ³	−0.3	0.55	0.88	3.465	—	—	—	—
HSUL12 (LPDDR2/3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.3	V _{CCIO} − 0.3	4	−4

Notes:

1. For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O (All I/Os used in the same V_{CCIO}).
2. Not all IO types are supported in all banks. Refer to [ECP5 and ECP5-5G sysI/O Usage Guide \(TN1262\)](#) for details.
3. MIPI D-PHY LP input can be implemented by powering V_{CCIO} to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCN0512 with V_{CCIO} at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCN0512.

Table 3.20. Register-to-Register Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	441	MHz
32-Bit Decoder	441	MHz
64-Bit Decoder	332	MHz
4:1 Mux	441	MHz
8:1 Mux	441	MHz
16:1 Mux	441	MHz
32:1 Mux	441	MHz
8-Bit Adder	441	MHz
16-Bit Adder	441	MHz
64-Bit Adder	441	MHz
16-Bit Counter	384	MHz
32-Bit Counter	317	MHz
64-Bit Counter	263	MHz
64-Bit Accumulator	288	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	214	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	441	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	441	MHz
DSP Functions		
9 x 9 Multiplier (All Registers)	225	MHz
18 x 18 Multiplier (All Registers)	225	MHz
36 x 36 Multiplier (All Registers)	225	MHz
18 x 18 Multiply-Add/Sub (All Registers)	225	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	225	MHz

Notes:

1. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

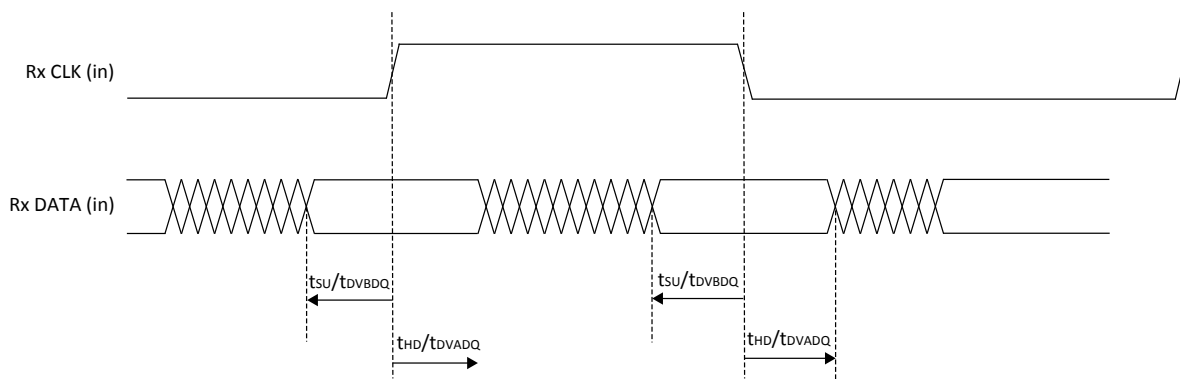


Figure 3.6. Receiver RX.CLK.Centered Waveforms

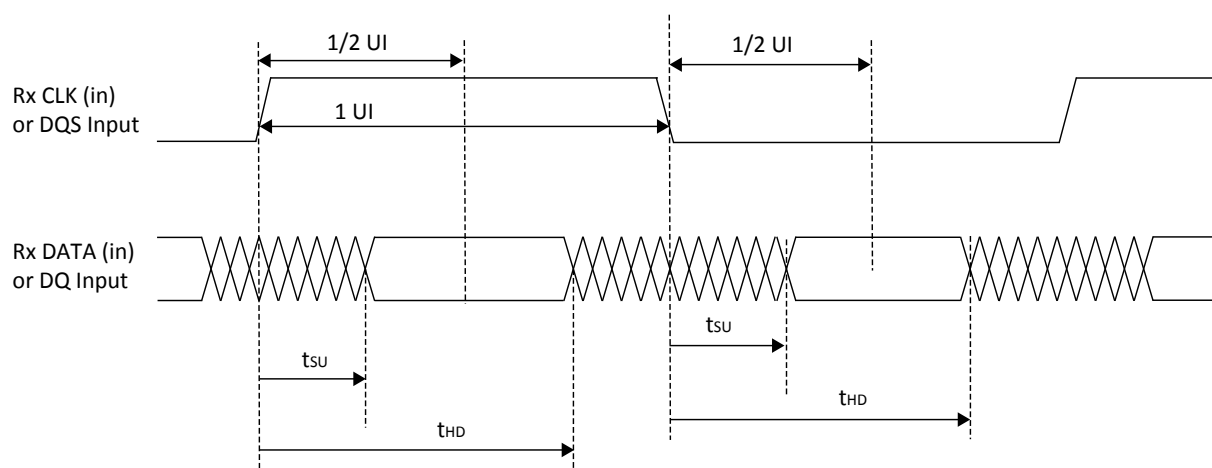


Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

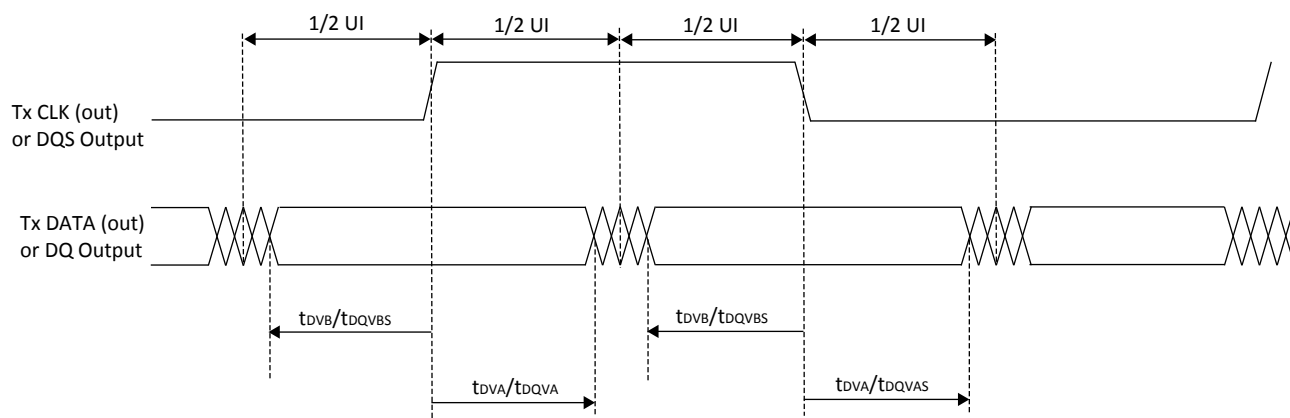


Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

Table 3.31. PCIe (5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit¹						
UI	Unit Interval	—	199.94	200	200.06	ps
B _{WTX-PKG-PLL2}	Tx PLL bandwidth corresponding to PKGTx-PLL2	—	5	—	16	MHz
P _{KGTx-PLL2}	Tx PLL Peaking	—	—	—	1	dB
V _{TX-DIFF-PP}	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
V _{TX-DIFF-PP-LOW}	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
V _{TX-DE-RATIO-3.5dB}	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
V _{TX-DE-RATIO-6dB}	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
T _{MIN-PULSE}	Instantaneous lone pulse width	—	—	—	—	UI
T _{TX-RISE-FALL}	Transmitter rise and fall time	—	—	—	—	UI
T _{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T _{TX-DJ}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T _{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
T _{RF-MISMATCH}	Tx rise/fall time mismatch	—	—	—	—	UI
R _{LTX-DIFF}	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R _{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
Z _{TX-DIFF-DC}	DC differential Impedance	—	—	—	120	Ω
V _{TX-CM-AC-PP}	Tx AC peak common mode voltage, peak-peak	—	—	—	—	mV, p-p
I _{TX-SHORT}	Transmitter short-circuit current	—	—	—	90	mA
V _{TX-DC-CM}	Transmitter DC common-mode voltage	—	0	—	1.2	V
V _{TX-IDLE-DIFF-DC}	Electrical Idle Output DC voltage	—	0	—	5	mV
V _{TX-IDLE-DIFF-AC-p}	Electrical Idle Differential Output peak voltage	—	—	—	—	mV
V _{TX-RCV-DETECT}	Voltage change allowed during Receiver Detect	—	—	—	600	mV
T _{TX-IDLE-MIN}	Min. time in Electrical Idle	—	20	—	—	ns
T _{TX-IDLE-SET-TO-IDLE}	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
T _{TX-IDLE-TO-DIFF-DATA}	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
L _{TX-SKEW}	Lane-to-lane output skew	—	—	—	—	ps

Table 3.36. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J _{RX_DJ} ^{2, 3, 4}	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J _{RX_RJ} ^{2, 3, 4}	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J _{RX_SJ} ^{2, 3, 4}	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T _{RX_EYE}	Receiver eye opening	—	0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.29. Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics

3.29.1. AC and DC Characteristics

Table 3.37. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T _{RF}	Differential rise/fall time	20% to 80%	—	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance	—	80	100	120	Ω
J _{TX_DDJ} ^{2, 3}	Output data deterministic jitter	—	—	—	0.10	UI
J _{TX_TJ} ^{1, 2, 3}	Total output data jitter	—	—	—	0.24	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.38. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J _{RX_DJ} ^{1, 2, 3, 4}	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.34	UI
J _{RX_RJ} ^{1, 2, 3, 4}	Random jitter tolerance (peak-to-peak)	—	—	—	0.26	UI
J _{RX_SJ} ^{1, 2, 3, 4}	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.11	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total jitter tolerance (peak-to-peak)	—	—	—	0.71	UI
T _{RX_EYE}	Receiver eye opening	—	0.29	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

Table 3.44. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V _{OH} – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Pin Information Summary		LFE5UM/ LFE5UM5G-25		LFE5UM/LFE5UM5G-45			LFE5UM/LFE5UM5G-85			
Pin Type		285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA
TAP		4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated Pins		7	7	7	7	7	7	7	7	7
GND		83	59	83	59	113	83	59	113	166
NC		1	8	1	2	33	1	0	17	29
Reserved		0	2	0	2	4	0	2	4	4
SERDES		14	28	14	28	28	14	28	28	28
VCCA (SERDES)	VCCA0	2	2	2	2	6	2	2	6	8
	VCCA1	0	2	0	2	6	0	2	6	9
VCCAUX (SERDES)	VCCAUXA0	2	2	2	2	2	2	2	2	2
	VCCAUXA1	0	2	0	2	2	0	2	2	2
GNDA (SERDES)		26	26	26	26	49	26	26	49	60
Total Balls		285	381	285	381	554	285	381	554	756
High Speed Differential Input / Output Pairs	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	10/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8	24/12
	Bank 3	14/7	16/8	14/7	16/8	24/12	14/7	16/8	24/12	32/16
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	13/6	16/8	13/6	16/8	24/12	13/6	16/8	24/12	32/16
	Bank 7	8/6	16/8	8/6	16/8	16/8	8/6	16/8	16/8	24/12
	Bank 8	0	0	0	0	0	0	0	0	0
Total High Speed Differential I/O Pairs		45/2	64/32	45/27	64/3	80/40	45/27	65/3	80/40	112/5
DQS Groups (> 11 pins in group)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	1	2	1	2	2	1	2	2	3
	Bank 3	2	2	2	2	3	2	2	3	4
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	2	2	2	2	3	2	2	3	4
	Bank 7	1	2	1	2	2	1	2	2	3
	Bank 8	0	0	0	0	0	0	0	0	0
Total DQS Groups		6	8	6	8	10	6	8	10	14

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	No
LFE5U-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	No
LFE5UM-25F-6MG285C	–6	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-7MG285C	–7	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-6BG381C	–6	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-7BG381C	–7	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-45F-6MG285C	–6	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-7MG285C	–7	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-6BG381C	–6	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-7BG381C	–7	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-6BG554C	–6	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-7BG554C	–7	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes
LFE5UM5G-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM5G-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM5G-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM5G-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM5G-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM5G-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes

5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	–6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	–7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	–8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	–6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	–7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	–8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	–6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	–7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	–8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	–6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	–7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	–8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	–6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	–7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	–8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	No

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	No
LFE5UM-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes
LFE5UM5G-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM5G-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM5G-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM5G-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM5G-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM5G-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM5G-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM5G-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM5G-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes



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