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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-25f-8mg285c

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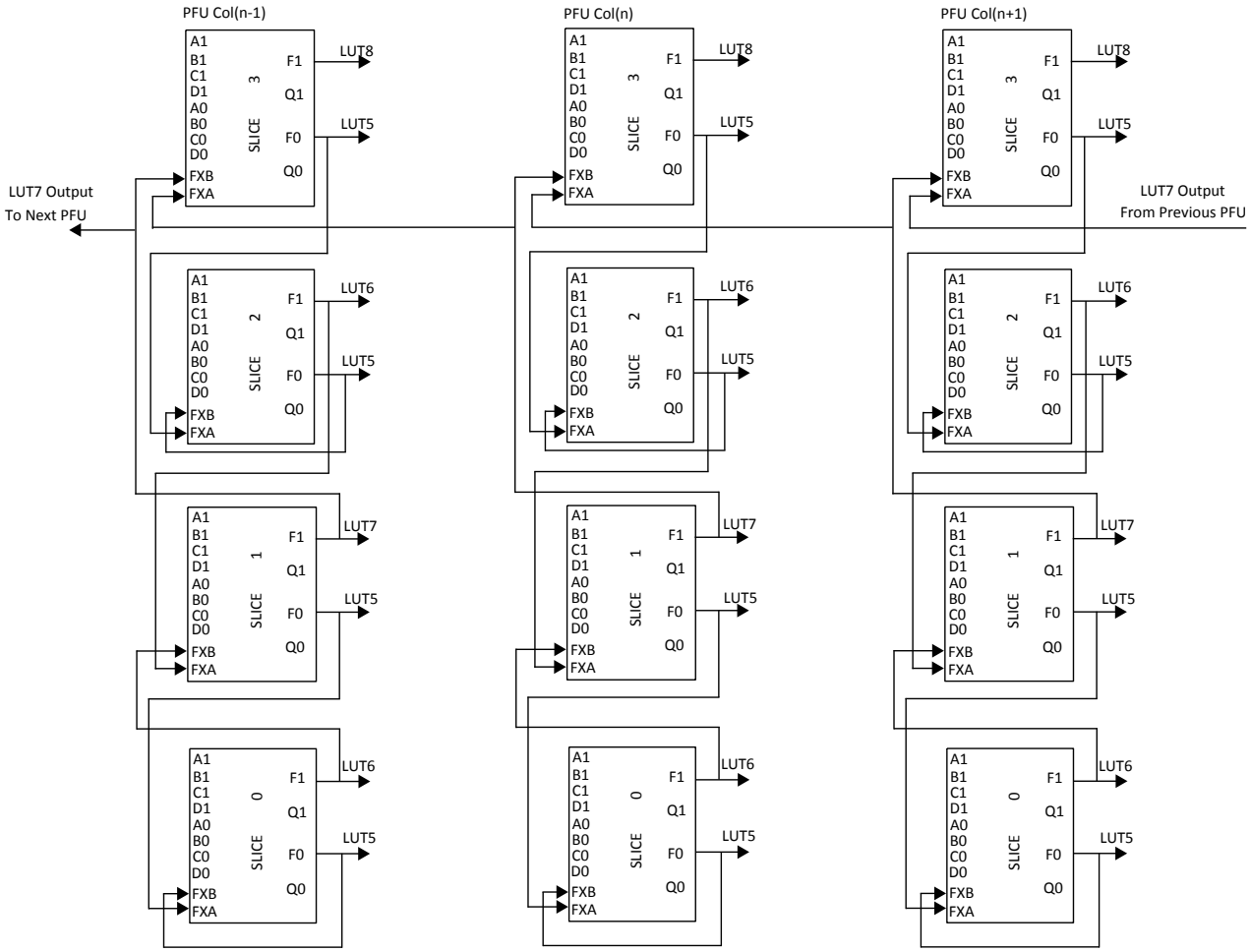


Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output[1]

Notes:

1. See Figure 2.3 on page 15 for connection details.
2. Requires two adjacent PFUs.

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

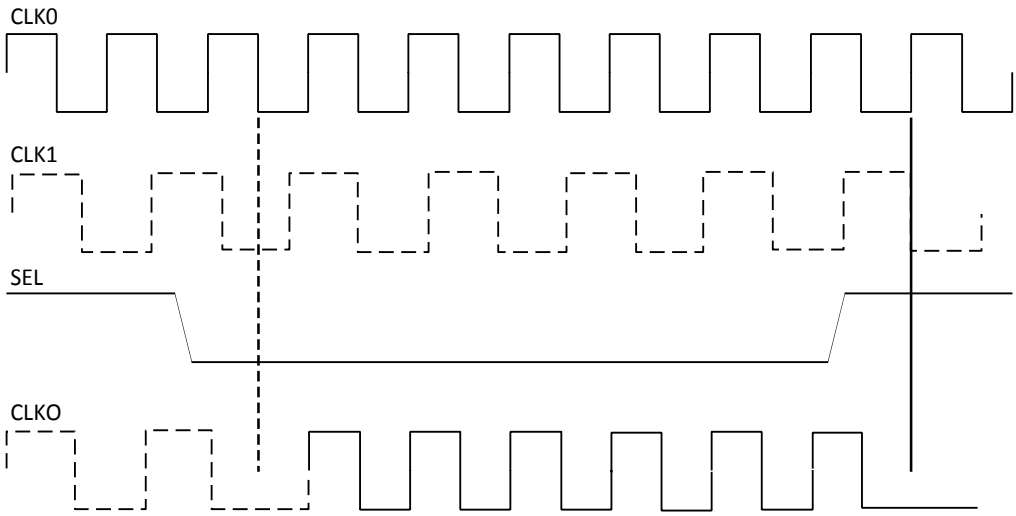


Figure 2.7. DCS Waveforms

2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

- Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

  Bank 4 I/O only exists in the LFE5-85 device.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Diamond tool.

- Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).

2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. Figure 2.27 shows the position of the dual blocks for the LFE5-85. Table 2.13 shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

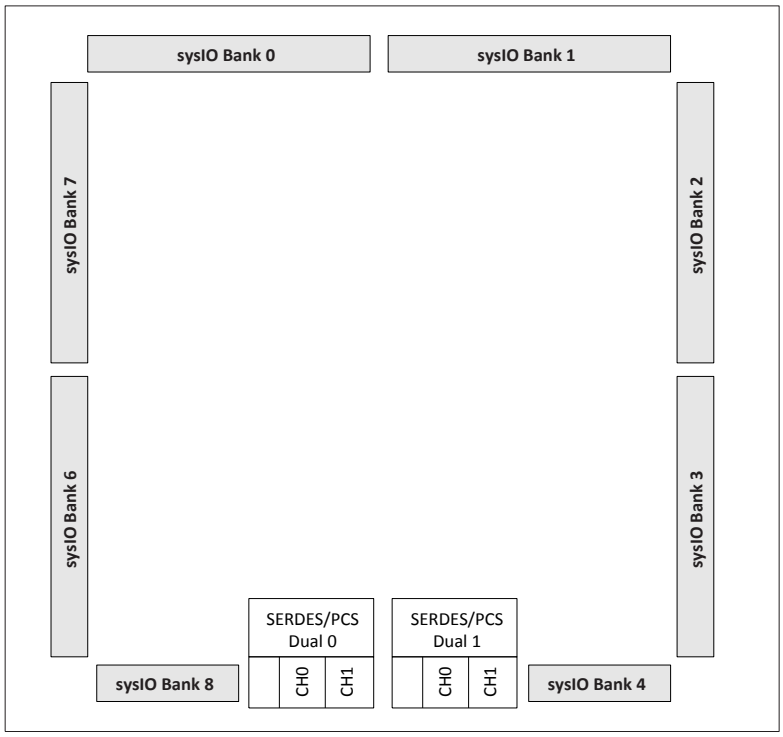


Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 [2]	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 [2]	x1	8b10b
SD-SDI (259M, 344M) [1]	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	—	—
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.

Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).

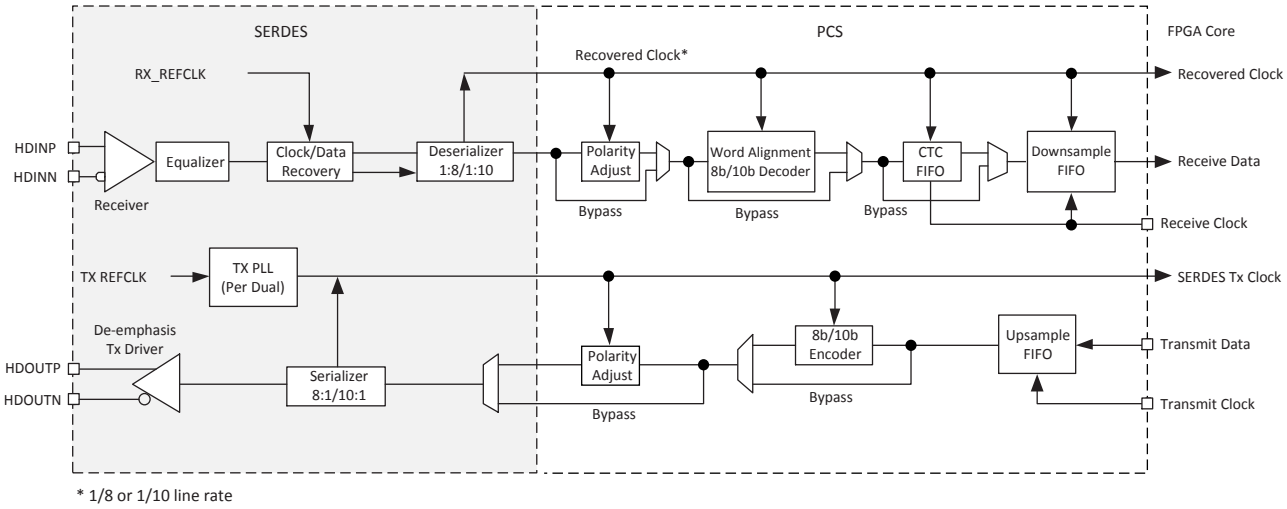


Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.5	1.32	V
V_{CCA}	Supply Voltage	–0.5	1.32	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	–0.5	2.75	V
V_{CCIO}	Supply Voltage	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CCHRX}, V_{CCHTX}	SERDES RX/TX Buffer Supply Voltages	–0.5	1.32	V
—	Voltage Applied on SERDES Pins	–0.5	1.80	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:
1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[2]	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage	—	2.375	2.625	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	—	1.14	3.465	V
V_{REF}[1]	Input Reference Voltage	—	0.5	1.0	V
t_{JCOM}	Junction Temperature, Commercial Operation	—	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	—	–40	100	°C
SERDES External Power Supply[5]					
V_{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V_{CCAUXA}	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
V_{CCHRX}[6]	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V_{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

Notes:
1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 on page 48.
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
5. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

3.14.5. **BLVDS25**

The ECP5/ECP5-5G devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

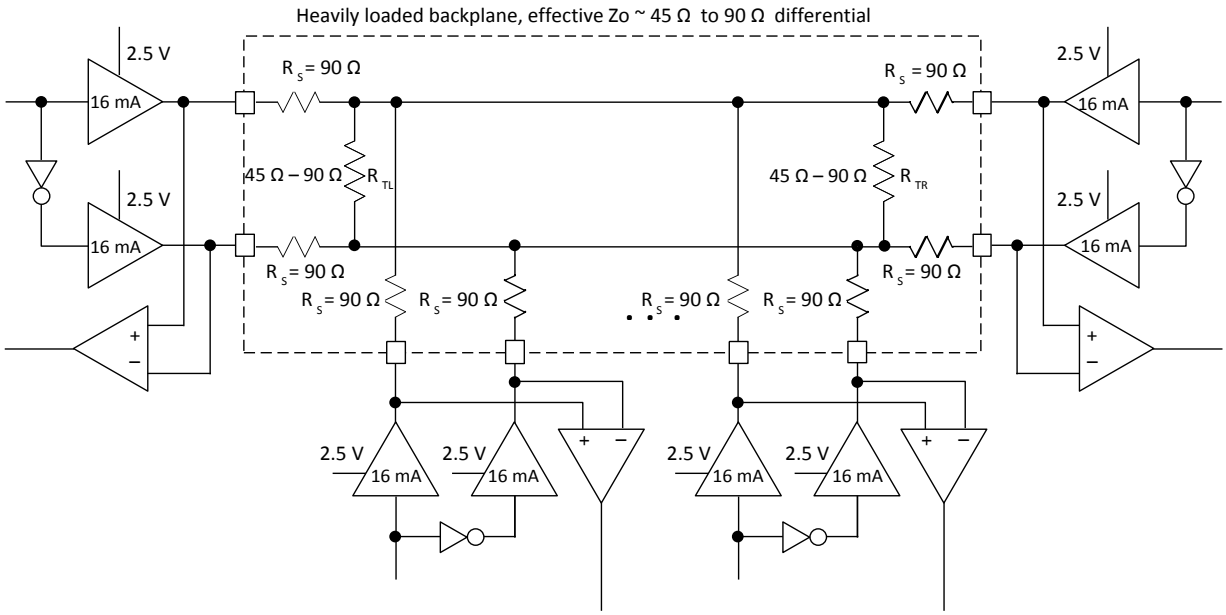


Figure 3.2. BLVDS25 Multi-point Output Example

Over recommended operating conditions.

Table 3.15. BLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo = 45 Ω	Zo = 90 Ω	
V_{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (±1%)	90.00	90.00	Ω
R_{TL}	Driver Parallel Resistor (±1%)	45.00	90.00	Ω
R_{TR}	Receiver Termination (±1%)	45.00	90.00	Ω
V_{OH}	Output High Voltage	1.38	1.48	V
V_{OL}	Output Low Voltage	1.12	1.02	V
V_{OD}	Output Differential Voltage	0.25	0.46	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	11.24	10.20	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks									
Primary Clock									
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
Edge Clock									
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
t_{SKEW_EDGE}	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
Generic SDR Input									
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL									
t_{CO}	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL									
t_{COPLL}	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
Generic DDR Output									
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDRX1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{DVB\_GDDRX1\_centered}$	Data Output Valid before CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$t_{DVA\_GDDRX1\_centered}$	Data Output Valid after CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9									
$t_{DIB\_GDDRX1\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.3	—	–0.3	—	–0.3	—	ns
$t_{DIA\_GDDRX1\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.3	—	0.3	—	0.3	ns
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8									
$t_{DVB\_GDDRX2\_centered}$	Data Output Valid Before CLK Output	All Devices	–0.442	—	–0.56	—	–0.676	—	ns + 1/2 UI
$t_{DVA\_GDDRX2\_centered}$	Data Output Valid After CLK Output	All Devices	—	0.442	—	0.56	—	0.676	ns + 1/2 UI
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9									
$t_{DIB\_GDDRX2\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns
$t_{DIA\_GDDRX2\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDRX71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12									
$t_{DIB\_LVDS71\_i}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns + (i) * UI
$t_{DIA\_LVDS71\_i}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns + (i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz
Memory Interface									
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)									
t_{DVBDQ_DDR2} t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	–0.26	—	–0.317	—	–0.374	ns + 1/2 UI
t_{DVADQ_DDR2} t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.26	—	0.317	—	0.374	—	ns + 1/2 UI

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

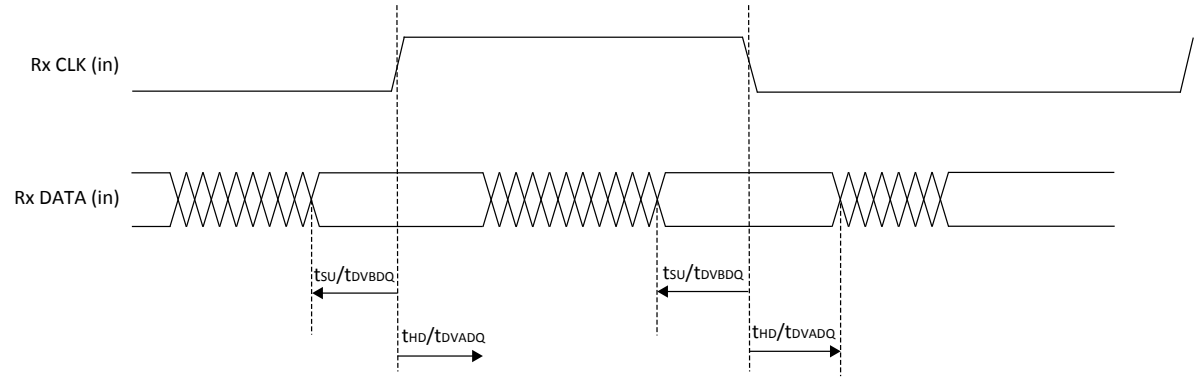


Figure 3.6. Receiver RX.CLK.Centered Waveforms

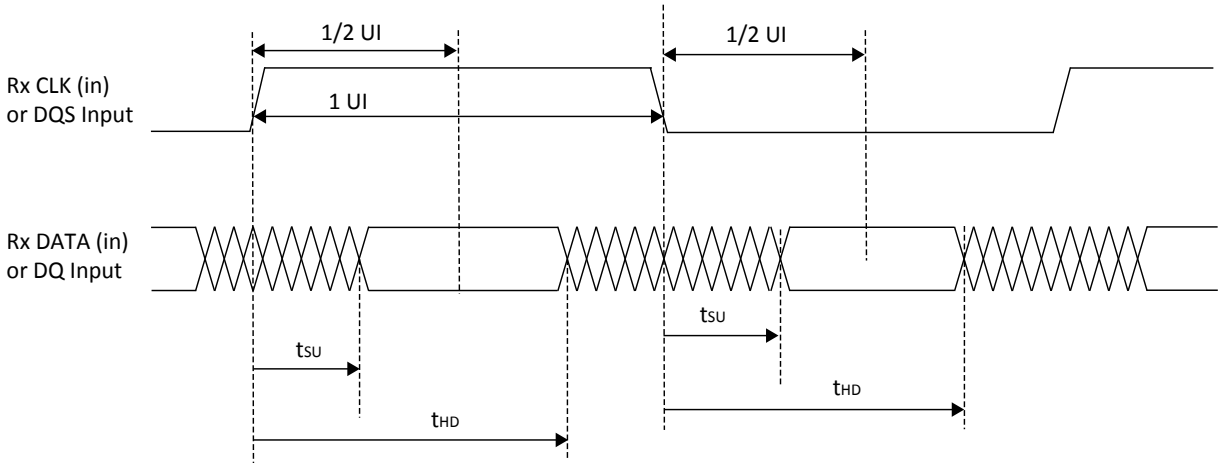


Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

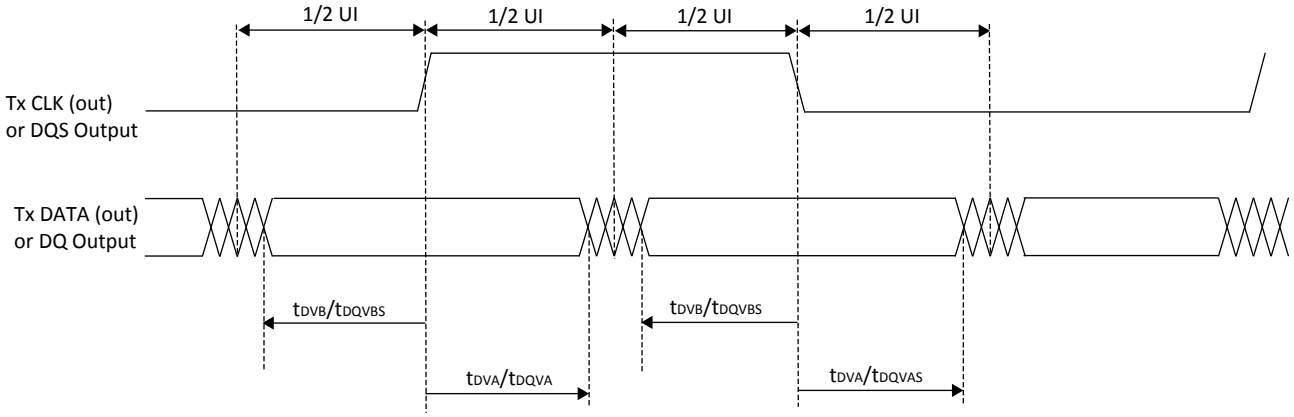


Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

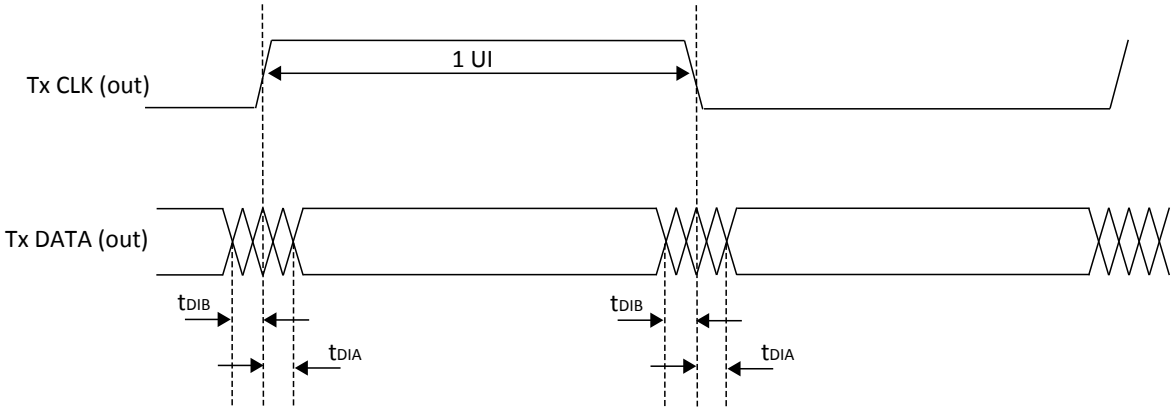
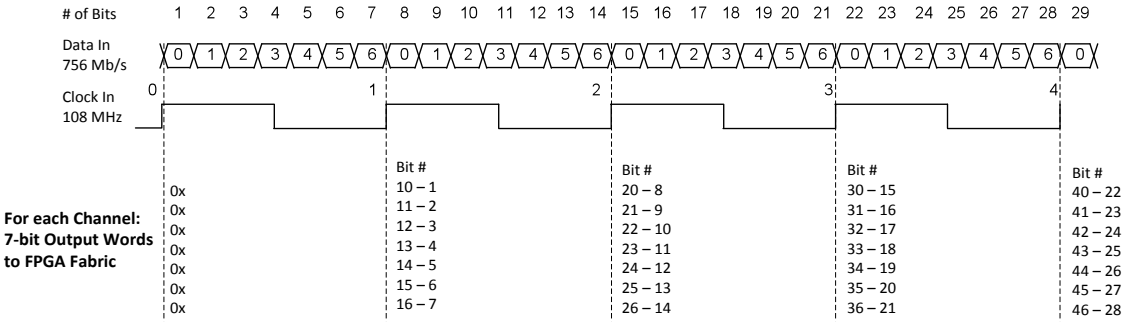


Figure 3.9. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter – Shown for one LVDS Channel

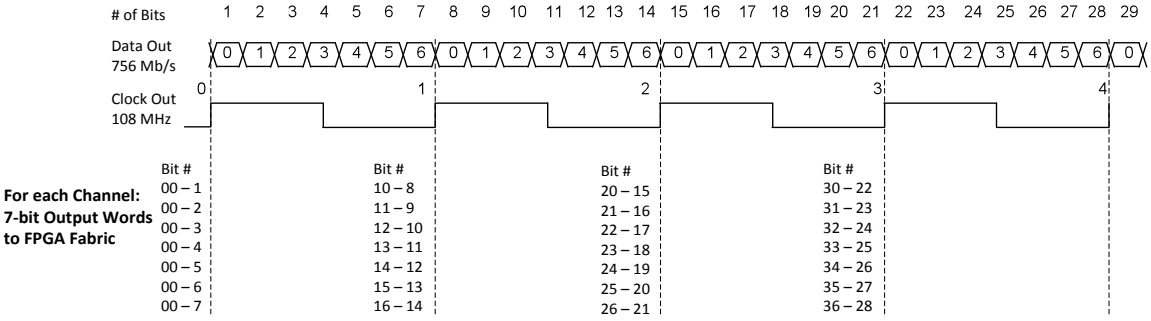


Figure 3.10. DDRX71 Video Timing Waveforms

3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

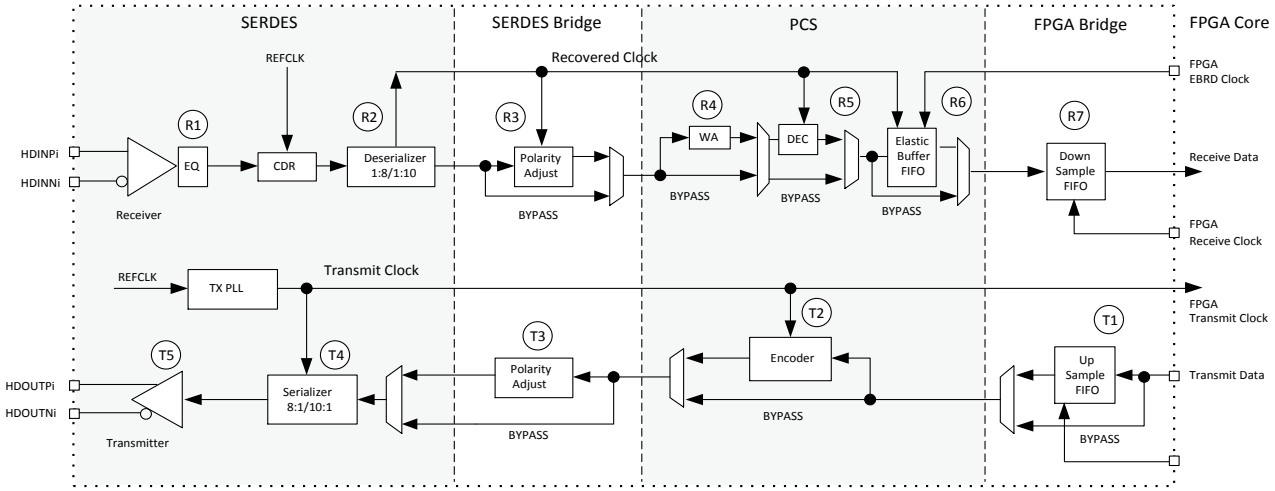
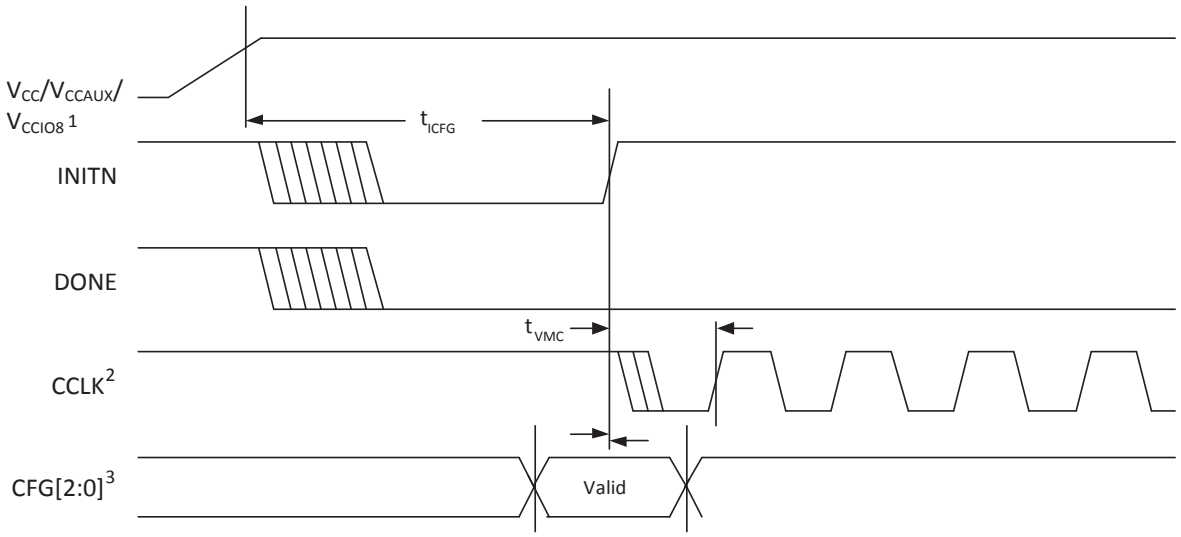


Figure 3.13. Transmitter and Receiver Latency Block Diagram



1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hardwired).

Figure 3.18. Power-On-Reset (POR) Timing

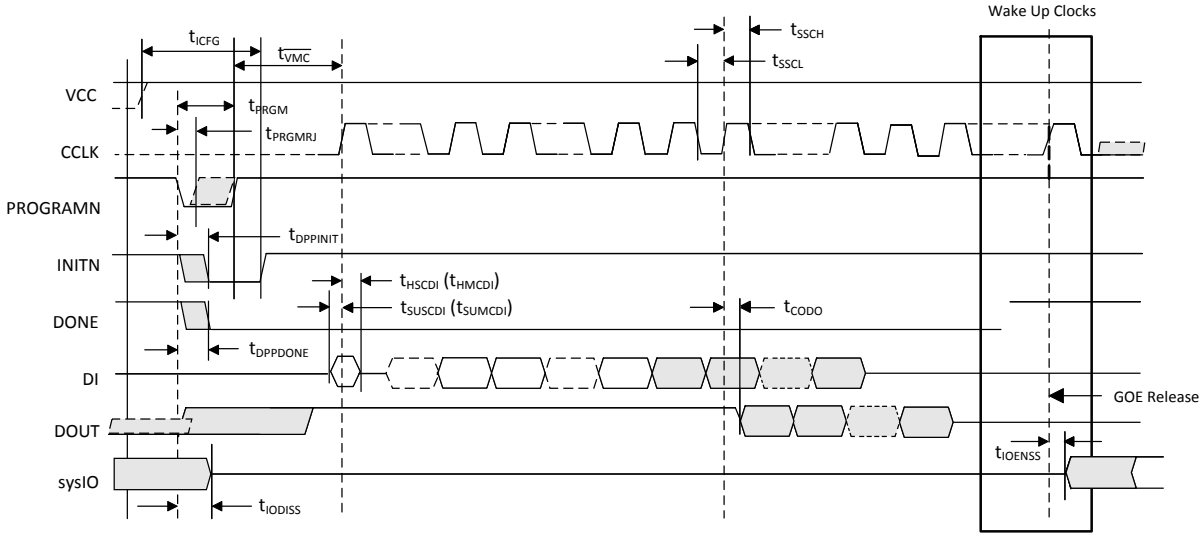
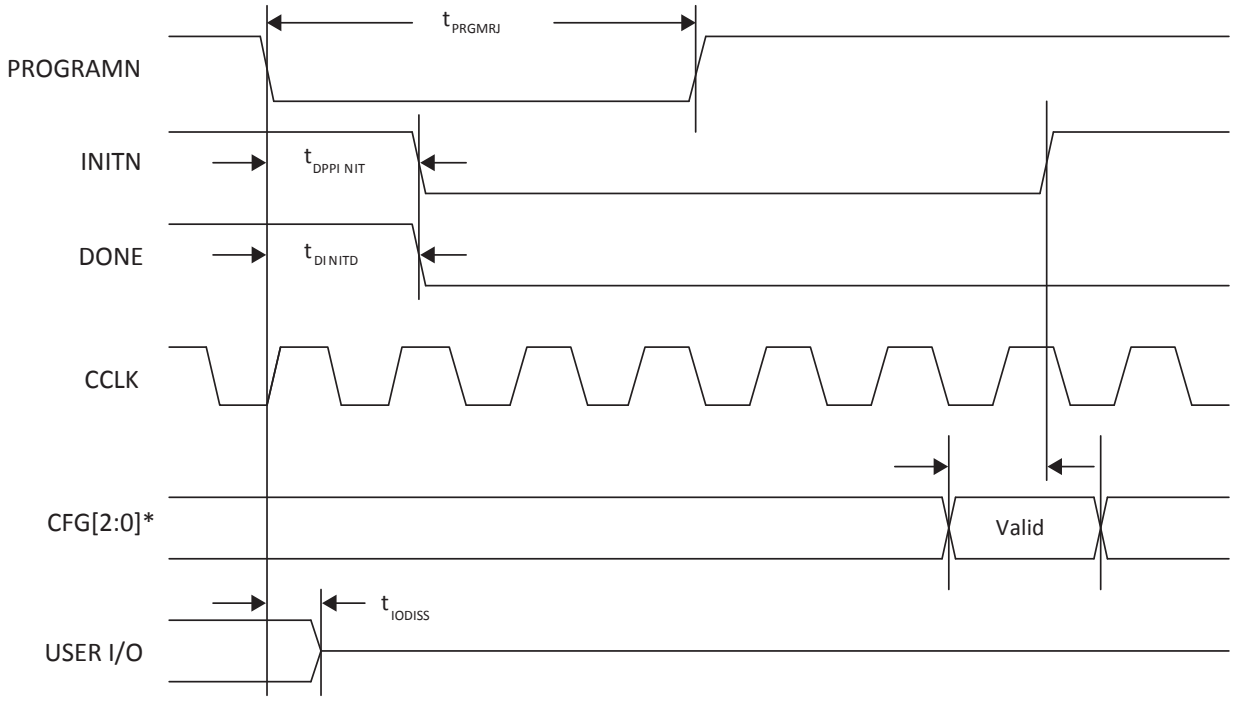


Figure 3.19. sysCONFIG Port Timing



*The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

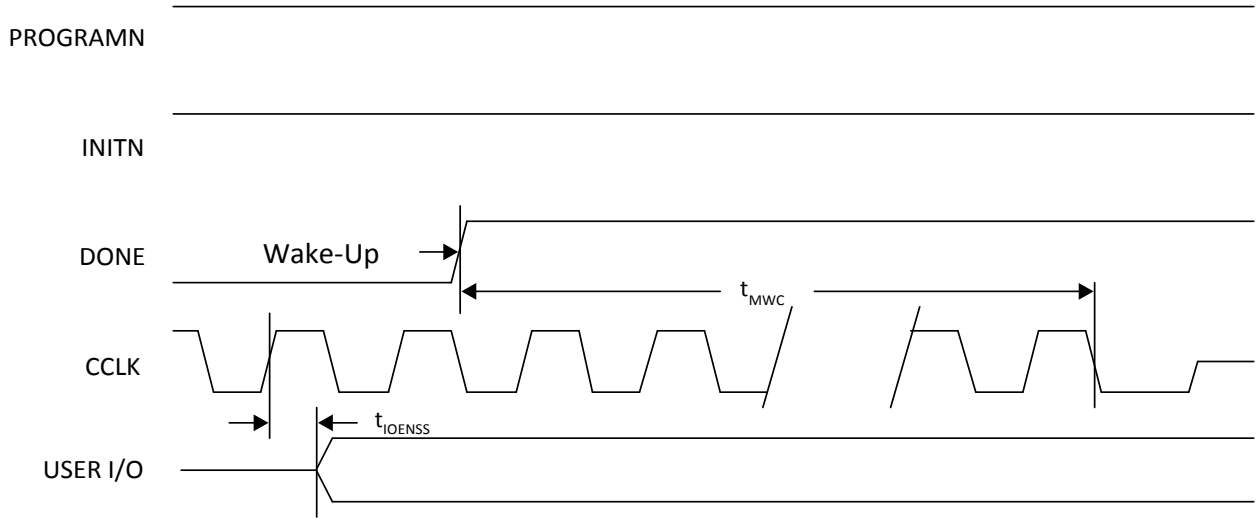


Figure 3.21. Wake-Up Timing

4. Pinout Information

4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[L/R] [Group Number]_[A/B/C/D]	I/O	[L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIO A and B are grouped as a pair, and PIO C and D are group as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer. Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω.
P[T/B][Group Number]_[A/B]	I/O	[T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer. PIO A/B forms a pair of emulated differential output buffer.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins. V_{CC} = 1.1 V (ECP5), 1.2 V (ECP5UM5G)
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. V_{CCAUX} = 2.5 V.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x. V_{CCIO8} is used for configuration and JTAG.
VREF1_x	—	Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as VREF1 input. When not used, they may be used as I/O pins.
PLL, DLL and Clock Functions		
[LOC][_GPLL[T, C]_IN	I	General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not configured as GPLL input pads, they can be used as general purpose I/O pins.
GR_PCLK[Bank][num]	I	General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to ECP5 sysClock PLL/DLL Design and Usage Guide (TN1263). These pins are shared I/O pins. When not configured as GR pins, they can be used as general purpose I/O pins.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/ O pins. When not configured as PCLK pins, they can be used as general purpose I/O pins.

5. Ordering Information

5.1. ECP5/ECP5-5G Part Number Description