E.J. Lattice Semiconductor Corporation - <u>LFE5U-45F-6BG381C Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	203
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-6bg381c

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1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, highspeed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance. The Lattice Diamond[™] design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
 - 12K to 84K LUTs
 - 197 to 365 user programmable I/Os
- Embedded SERDES
 - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
 - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
 - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
 - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
 - Fully cascadable slice architecture
 - 12 to 160 slices for high performance multiply and accumulate
 - Powerful 54-bit ALU operations
 - Time Division Multiplexing MAC Sharing
 - Rounding and truncation
 - Each slice supports
 - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
 - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
 - Up to 3.744 Mb sysMEM[™] Embedded Block RAM (EBR)
 - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs





*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Name	Туре	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

Table 2.9. Output Block Port Description

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).



Figure 2.21. Tristate Register Block on Top Side







Name	Туре	Description
TD	Input	Tristate Input to Tristate SDR Register
RST	Input	Reset to the Tristate Block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.13. DDR Memory Support

2.13.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in Figure 2.23 on page 36. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as "virtual" VCCIO, by driving these pins to HIGH, with the user connecting these pins to VCCIO power supply. These connections create "soft" connections to V_{CCIO} thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).



	PIO A	sysIO Buffer	Pad A (T)
••	PIO B	sysIO Buffer	Pad B (C)
••	PIO C	sysIO Buffer	Pad C
••	PIO D	sysIO Buffer ←→	Pad D
↓	PIO A	sysIO Buffer	Pad A (T)
••	PIO B	sysIO Buffer	Pad B (C)
↓	PIO C	sysIO Buffer	Pad C
••	PIO D	sysIO Buffer	Pad D
	DQSBUF	Delay	'
↓ →	PIO A	sysIO Buffer	Pad A (T)
↓	PIO B	sysIO Buffer	Pad B (C)
↓	PIO C	sysIO Buffer	Pad C
↓ →	PIO D	sysIO Buffer	Pad D
↓	PIO A	sysIO Buffer	Pad A (T)
↓	PIO B	sysIO Buffer	Pad B (C)
↓	PIO C	syslO Buffer ◀ ┿	Pad C
	PIO D	sysIO Buffer	Pad D

Figure 2.23. DQS Grouping on the Left and Right Edges

2.13.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR2/3, LPDDR2/3), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifted is achieved by using DQSDEL programmable delay line in the DQS Delay Block (DQS read circuit). The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block shown in Figure 2.24 generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.



2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. Figure 2.27 shows the position of the dual blocks for the LFE5-85. Table 2.13 shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).



Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	-	2	2
756 caBGA	-	-	2

Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).



Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

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3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Dawawashaw	Description	Device	-8		-7		-6		Unit
Parameter	Description	Device	Min	Max	Min	Max	Min	Max	Unit
Clocks									
Primary Clock									
f _{MAX_PRI}	Frequency for Primary Clock Tree	_	—	370	—	303	—	257	MHz
t _{w_pri}	Clock Pulse Width for Primary Clock	_	0.8	—	0.9	-	1.0	-	ns
t _{skew_pri}	Primary Clock Skew within a Device	_	_	420	_	462	_	505	ps
Edge Clock									
f _{MAX_EDGE}	Frequency for Edge Clock Tree	_	_	400	_	350	_	312	MHz
tw_edge	Clock Pulse Width for Edge Clock	_	1.175	—	1.344		1.50		ns
t _{skew_edge}	Edge Clock Skew within a Bank	—	_	160	_	180	—	200	ps
Generic SDR Input									
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ithout PL	L					
t _{co}	Clock to Output - PIO Output Register	All Devices	—	5.4	_	6.1	—	6.8	ns
t _{su}	Clock to Data Setup - PIO Input Register	All Devices	0	_	0	-	0	-	ns
t _H	Clock to Data Hold - PIO Input Register	All Devices	2.7	_	3	-	3.3	-	ns
t _{su_del}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	_	1.33	_	1.46	_	ns
t _{h_del}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	_	0	_	0	_	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	_	400	_	350	_	312	MHz
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ith PLL						
t _{copll}	Clock to Output - PIO Output Register	All Devices	_	3.5	_	3.8	_	4.1	ns
t _{supll}	Clock to Data Setup - PIO Input Register	All Devices	0.7	_	0.78	-	0.85	_	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	_	0.89	_	0.98	_	ns
t _{su_delpll}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	_	1.78	_	1.95	_	ns

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	.			-8	-	-7	-6		
Parameter	Description	Device	Min	Max	Min	Max	Min	Max	Unit
t _{h_delpll}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	_	0	_	0	_	ns
Generic DDR Input							•		
Generic DDRX1 Inp	uts With Clock and Data Centere	d at Pin (GDDI	RX1_RX.	SCLK.Cent	tered) Us	ing PCLK	Clock In	put - Fig	ure 3.6
t _{SU_GDDRX1_centered}	Data Setup Before CLK Input	All Devices	0.52	-	0.52	-	0.52	_	ns
t _{HD_GDDRX1_centered}	Data Hold After CLK Input	All Devices	0.52	_	0.52	_	0.52	_	ns
f _{DATA_GDDRX1_centered}	GDDRX1 Data Rate	All Devices	_	500	_	500	_	500	Mb/s
f _{MAX_GDDRX1_centered}	GDDRX1 CLK Frequency (SCLK)	All Devices	_	250	-	250	_	250	MHz
Generic DDRX1 Inp	uts With Clock and Data Aligned	at Pin (GDDR)	(1_RX.SC	LK.Aligne	ed) Using	PCLK Cl	ock Input	- Figure	3.7
$t_{su_GDDRX1_aligned}$	Data Setup from CLK Input	All Devices	-	-0.55	-	-0.55	-	-0.55	ns + 1/2 UI
$t_{HD_GDDRX1_aligned}$	Data Hold from CLK Input	All Devices	0.55	_	0.55	-	0.55	-	ns + 1/2 UI
$f_{DATA_GDDRX1_aligned}$	GDDRX1 Data Rate	All Devices	—	500	-	500	—	500	Mb/s
f _{MAX_GDDRX1_aligned}	GDDRX1 CLK Frequency (SCLK)	All Devices	_	250	_	250	_	250	MHz
Generic DDRX2 Inp	uts With Clock and Data Centere	d at Pin (GDDI	RX2_RX.I	ECLK.Cen	tered) Us	ing PCLK	Clock In	put, Left	and
Right sides Only - F	igure 3.6	1	T		T	1	1	1	1
$t_{SU_GDDRX2_centered}$	Data Setup before CLK Input	All Devices	0.321	. –	0.403	—	0.471	—	ns
$t_{HD_GDDRX2_centered}$	Data Hold after CLK Input	All Devices	0.321	. —	0.403	_	0.471	_	ns
$f_{\text{DATA}_{GDDRX2}_{centered}}$	GDDRX2 Data Rate	All Devices	_	800	_	700	_	624	Mb/s
$f_{MAX_GDDRX2_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	-	400	—	350	—	312	MHz
Generic DDRX2 Inp	uts With Clock and Data Aligned	at Pin (GDDR)	(2_RX.EC	LK.Aligne	ed) Using	PCLK Cl	ock Input	, Left an	d Right
sides Only - Figure	3.7								1
t _{SU_GDDRX2_aligned}	Data Setup from CLK Input	All Devices	—	-0.344	—	-0.42	_	-0.495	ns + 1/2 UI
$t_{HD_GDDRX2_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	_	0.495	-	ns + 1/2 UI
$f_{DATA_GDDRX2_aligned}$	GDDRX2 Data Rate	All Devices	_	800	—	700	—	624	Mb/s
f _{MAX_GDDRX2_aligned}	GDDRX2 CLK Frequency	All Devices	—	400	_	350	_	312	MHz
Video DDRX71 Inpu	uts With Clock and Data Aligned a	t Pin (GDDRX	71_RX.E	CLK) Usin	g PLL Clo	ck Input	, Left and	Right si	des Only
Figure 3.11									
t _{su_lvds71_i}	Data Setup from CLK Input (bit i)	All Devices	_	-0.271	—	-0.39	_	-0.41	ns+(1/2+i) * UI
t _{HD_LVDS71_i}	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	_	0.41	_	ns+(1/2+i) * UI
f _{DATA_LVDS71}	DDR71 Data Rate	All Devices	_	756	—	620	—	525	Mb/s
f _{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	_	378	—	310	—	262.5	MHz

Table 3.22. ECP5/ECP5-5G External Switching Characteristics (Continued)



Deveryoten	Description	Device	-8		-7		-6		11
Parameter	Description	Device	Min	Мах	Min	Max	Min	Max	Unit
fdata_ddr2 fdata_ddr3 fdata_ddr3l fdata_lddr3l fdata_lpddr2 fdata_lpddr3	DDR Memory Data Rate	All Devices	_	800	_	700	_	624	Mb/s
fmax_ddr2 fmax_ddr3 fmax_ddr3l fmax_lpddr2 fmax_lpddr3	DDR Memory CLK Frequency (ECLK)	All Devices	_	400	_	350	_	312	MHz
DDR2/DDR3/DDR	3L/LPDDR2/LPDDR3 WRITE (DO	Q Output Data	are Cente	ered to DC	QS)				
tDQVBS_DDR2 tDQVBS_DDR3 tDQVBS_DDR3L tDQVBS_LPDDR2 tDQVBS_LPDDR3 tDQVAS_DDR2	Data Output Valid before DQS Output	All Devices	_	-0.25	_	-0.25	_	-0.25	UI
t _{DQVAS_DDR3} t _{DQVAS_DDR3L} t _{DQVAS_LPDDR2} t _{DQVAS_LPDDR3}	Data Output Valid after DQS Output	All Devices	0.25	_	0.25	_	0.25	_	UI
fdata_ddr2 fdata_ddr3 fdata_ddr3 fdata_ddr3l fdata_lpddr2 fdata_lpddr3	DDR Memory Data Rate	All Devices	_	800	_	700	_	624	Mb/s
fmax_ddr2 fmax_ddr3 fmax_ddr3l fmax_lpddr2 fmax_lpddr3	DDR Memory CLK Frequency (ECLK)	All Devices	_	400	_	350	_	312	MHz

Notes:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.

 General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load. Generic DDR timing are numbers based on LVDS I/O. DDR2 timing numbers are based on SSTL18. DDR3 timing numbers are based on SSTL15. LPDDR2 and LPDDR3 timing numbers are based on HSUL12.

- 3. Uses LVDS I/O standard for measurements.
- 4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- 5. All numbers are generated with the Diamond software.

FPGA-DS-02012-1.9





Figure 3.6. Receiver RX.CLK.Centered Waveforms



Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms



Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

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Figure 3.9. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter - Shown for one LVDS Channel



Figure 3.10. DDRX71 Video Timing Waveforms

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3.25. PCI Express Electrical and Timing Characteristics

3.25.1. PCIe (2.5 Gb/s) AC and DC Characteristics

Over recommended operating conditions.

Table 3.30. PCIe (2.5 Gb/s)

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
Transmit ¹						
UI	Unit interval	_	399.88	400	400.12	ps
V _{TX-DIFF_P-P}	Differential peak-to-peak output	—	0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio	_	-3	-3.5	-4	dB
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage	_	_	_	20	mV
V _{TX-RCV-DETECT}	Amount of voltage change allowed during receiver detection	_	_	_	600	mV
V _{TX-CM-DC}	Tx DC common mode voltage	_	0	_	V _{CCHTX}	V
I _{TX-SHORT}	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	_	_	90	mA
Z _{TX-DIFF-DC}	Differential output impedance	—	80	100	120	Ω
RL _{TX-DIFF}	Differential return loss	—	10	_	—	dB
RL _{TX-CM}	Common mode return loss	—	6.0	_	—	dB
T _{TX-RISE}	Tx output rise time	20% to 80%	0.125	_	—	UI
T _{TX-FALL}	Tx output fall time	20% to 80%	0.125	_	—	UI
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link	-	-	-	1.3	ns
T _{TX-EYE}	Transmitter eye width	—	0.75	_	—	UI
T _{TX-EYE-MEDIAN-TO-MAX-} JITTER	Maximum time between jitter median and maximum deviation from median	-	-	-	0.125	UI
Receive ^{1, 2}						
UI	Unit Interval	_	399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage	_	0.34 ³	_	1.2	v
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage	_	65	—	340 ³	mV
V _{RX-CM-AC_P}	RMS AC peak common-mode input voltage	_	_	_	150	mV
Z _{RX-DIFF-DC}	DC differential input impedance	_	80	100	120	Ω
Z _{RX-DC}	DC input impedance	_	40	50	60	Ω
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance	_	200K	—	-	Ω
RL _{RX-DIFF}	Differential return loss	_	10	—	-	dB
RL _{RX-CM}	Common mode return loss	-	6.0	—	—	dB

Notes:

- 1. Values are measured at 2.5 Gb/s.
- 2. Measured with external AC-coupling on the receiver.
- 3. Not in compliance with PCI Express 1.1 standard.

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Table 3.36. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	-	—	dB
Z _{RX_DIFF}	Differential termination resistance	_	80	100	120	Ω
J _{RX_DJ} ^{2, 3, 4}	Deterministic jitter tolerance (peak-to-peak)	_	—	-	0.37	UI
J _{RX_RJ} ^{2, 3, 4}	Random jitter tolerance (peak-to-peak)	_	—	—	0.18	UI
J _{RX_SJ} ^{2, 3, 4}	Sinusoidal jitter tolerance (peak-to-peak)	—	_	_	0.10	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total jitter tolerance (peak-to-peak)	_	—	—	0.65	UI
T _{RX_EYE}	Receiver eye opening	—	0.35	—	-	UI

Notes:

- 1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
- 2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
- 3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
- 4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.29. Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics

3.29.1. AC and DC Characteristics

Table 3.37. Transmit

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
T _{RF}	Differential rise/fall time	20% to 80%	-	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance	-	80	100	120	Ω
J _{TX_DDJ} ^{2, 3}	Output data deterministic jitter	-	-	_	0.10	UI
J _{TX_TJ} ^{1, 2, 3}	Total output data jitter	-	1	—	0.24	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.38. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential termination resistance	-	80	100	120	Ω
J _{RX_DJ} ^{1, 2, 3, 4}	Deterministic jitter tolerance (peak-to-peak)	-	—	—	0.34	UI
J _{RX_RJ} ^{1, 2, 3, 4}	Random jitter tolerance (peak-to-peak)	-	—	—	0.26	UI
J _{RX_SJ} ^{1, 2, 3, 4}	Sinusoidal jitter tolerance (peak-to-peak)	-	—	—	0.11	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total jitter tolerance (peak-to-peak)	—	—	—	0.71	UI
T _{RX_EYE}	Receiver eye opening	—	0.29	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.

- 2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
- 3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
- 4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

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Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f _{MAX}	TCK clock frequency		25	MHz
t _{втсрн}	TCK [BSCAN] clock pulse width high	20	—	ns
t _{btcpl}	TCK [BSCAN] clock pulse width low	20	—	ns
t _{BTS}	TCK [BSCAN] setup time	10	_	ns
t _{BTH}	TCK [BSCAN] hold time	8	_	ns
t _{BTRF}	TCK [BSCAN] rise/fall time	50	_	mV/ns
t _{втсо}	TAP controller falling edge of clock to valid output		10	ns
t _{BTCODIS}	TAP controller falling edge of clock to valid disable		10	ns
t _{btcoen}	TAP controller falling edge of clock to valid enable		10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	_	ns
t _{втскн}	BSCAN test capture register hold time	25	_	ns
t _{витсо}	BSCAN test update register, falling edge of clock to valid output		25	ns
t _{btuodis}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t btupoen	BSCAN test update register, falling edge of clock to valid enable	_	25	ns

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Figure 3.23. JTAG Port Timing Waveforms

3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.



*CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards



Signal Name	I/O	Description					
Configuration Pads (Used during sysCONFIG) (Continued)							
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.					
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.					
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.					
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.					
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.					
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.					
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin					
SERDES Function	SERDES Function						
VCCAx	-	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCAx = 1.1 V for ECP5, VCCAx = 1.2 V for ECP5-5G.					
VCCAUXAx	-	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUXAx = 2.5 V.					
HDRX[P/N]_D[dual_num]CH[chan_num]	Ι	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.					
HDTX[P/N]_D[dual_num]CH[chan_num]	0	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.					
REFCLK[P/N]_D[dual_num]	Ι	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.					
VCCHRX_D[dual_num]CH[chan_num]	_	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.					
VCCHTX_D[dual_num]CH[chan_num]	_	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.					

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.

2. These pins are dedicated inputs or can be used as general purpose I/O.

3. m defines the associated channel in the quad.

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Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-45F-8BG554C	-8	Lead free caBGA	554	Commercial	44	No
LFE5U-85F-6MG285C	-6	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-7MG285C	LFE5U-85F-7MG285C -7		285	Commercial	84	No
LFE5U-85F-8MG285C	-8	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-6BG381C	-6	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-7BG381C	-7	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-8BG381C	-8	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-6BG554C	-6	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-7BG554C	-7	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-8BG554C	-8	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-6BG756C	-6	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-7BG756C	-7	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-8BG756C	-8	Lead free caBGA	756	Commercial	84	No
LFE5UM-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-8BG554C	-8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-85F-6MG285C	-6	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-7MG285C	-7	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-8MG285C	-8	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-6BG381C	-6	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-7BG381C	-7	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-8BG381C	-8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-6BG554C	-6	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-7BG554C	-7	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-8BG554C	-8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-6BG756C	-6	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-7BG756C	-7	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-8BG756C	-8	Lead free caBGA	756	Commercial	84	Yes
LFE5UM5G-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM5G-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM5G-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM5G-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM5G-45F-8BG554C	-8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM5G-85F-8MG285C	-8	Lead free csfBGA	285	Commercial	84	Yes



(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.