Lattice Semiconductor Corporation - LFE5U-45F-6BG554C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	245
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-6bg554c

Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.

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Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).

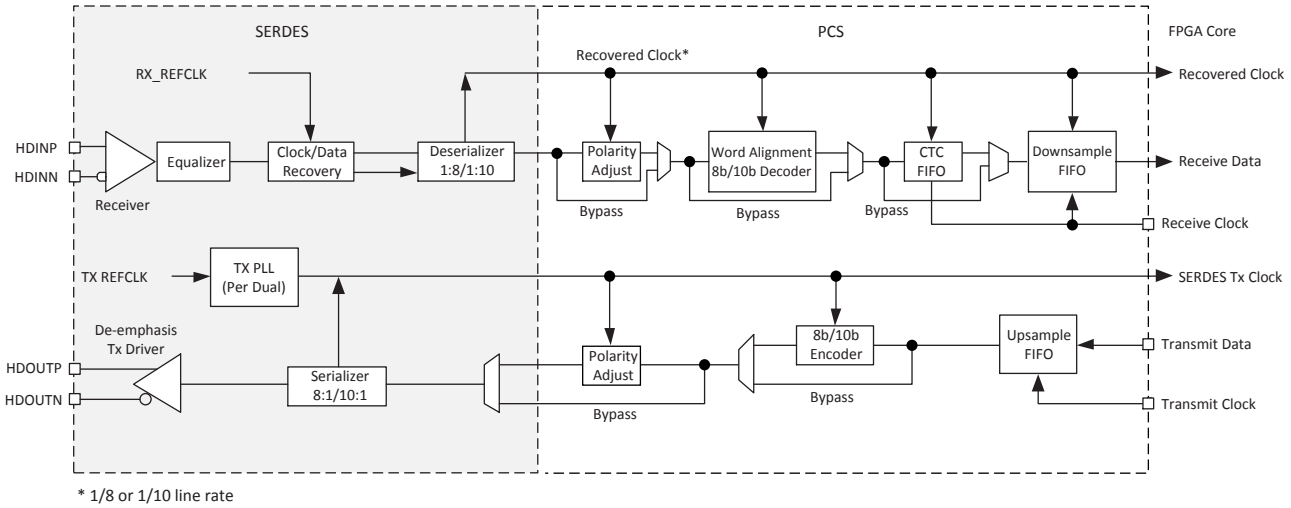

Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

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2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) – Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to Minimizing System Interruption During Configuration Using TransFR Technology (TN1087) for details.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

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When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

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3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

Table 3.18. Input to SLVS

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.

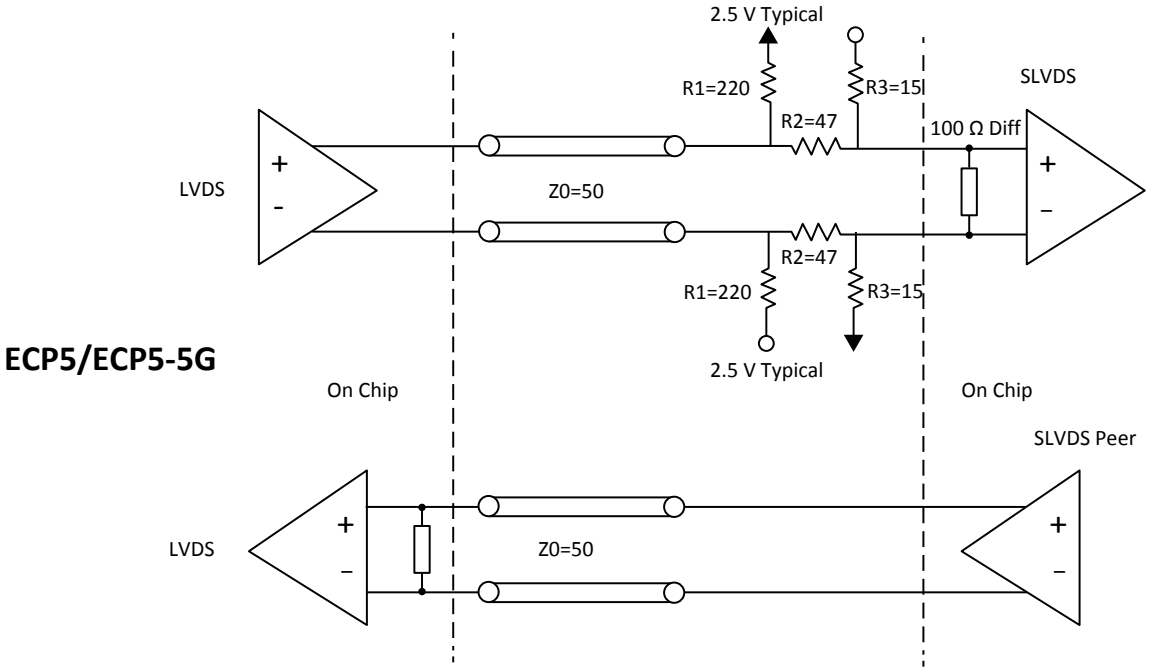

Figure 3.5. SLVS Interface

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Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
Generic DDR Input									
Generic DDRX1 Inputs With Clock and Data Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{SU_GDDRX1_centered}$	Data Setup Before CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$t_{HD_GDDRX1_centered}$	Data Hold After CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$f_{DATA_GDDRX1_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX_GDDRX1_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs With Clock and Data Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.7									
$t_{SU_GDDRX1_aligned}$	Data Setup from CLK Input	All Devices	—	–0.55	—	–0.55	—	–0.55	ns + 1/2 UI
$t_{HD_GDDRX1_aligned}$	Data Hold from CLK Input	All Devices	0.55	—	0.55	—	0.55	—	ns + 1/2 UI
$f_{DATA_GDDRX1_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX_GDDRX1_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Inputs With Clock and Data Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.6									
$t_{SU_GDDRX2_centered}$	Data Setup before CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$t_{HD_GDDRX2_centered}$	Data Hold after CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$f_{DATA_GDDRX2_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX_GDDRX2_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Inputs With Clock and Data Aligned at Pin (GDDRX2_RX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.7									
$t_{SU_GDDRX2_aligned}$	Data Setup from CLK Input	All Devices	—	–0.344	—	–0.42	—	-0.495	ns + 1/2 UI
$t_{HD_GDDRX2_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	—	0.495	—	ns + 1/2 UI
$f_{DATA_GDDRX2_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX_GDDRX2_aligned}$	GDDRX2 CLK Frequency	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Inputs With Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) Using PLL Clock Input, Left and Right sides Only Figure 3.11									
$t_{SU_LVDS71_i}$	Data Setup from CLK Input (bit i)	All Devices	—	–0.271	—	–0.39	—	–0.41	ns+(1/2+i) * UI
$t_{HD_LVDS71_i}$	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	—	0.41	—	ns+(1/2+i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz

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3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

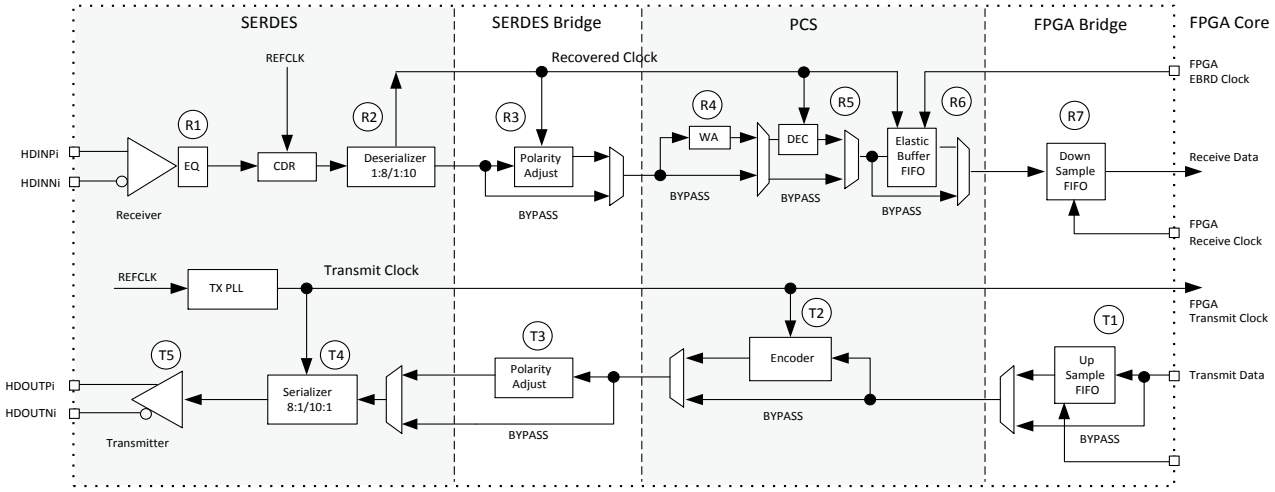

Figure 3.13. Transmitter and Receiver Latency Block Diagram

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(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section. • Deleted Serial RapidIO protocol under Embedded SERDES. • Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3. Mentioned transmit de-emphasis “pre- and post-cursors”.
		Architecture	Updated Overview section. • Revised description of PFU blocks. • Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section. • Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. • Deleted Serial RapidIO protocol. • Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section. • Deleted “130 MHz ±15% CMOS” oscillator. • Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA}.
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to t_{SKEW_PR} V_{CCA} and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.

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