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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-6mg285i

Figures

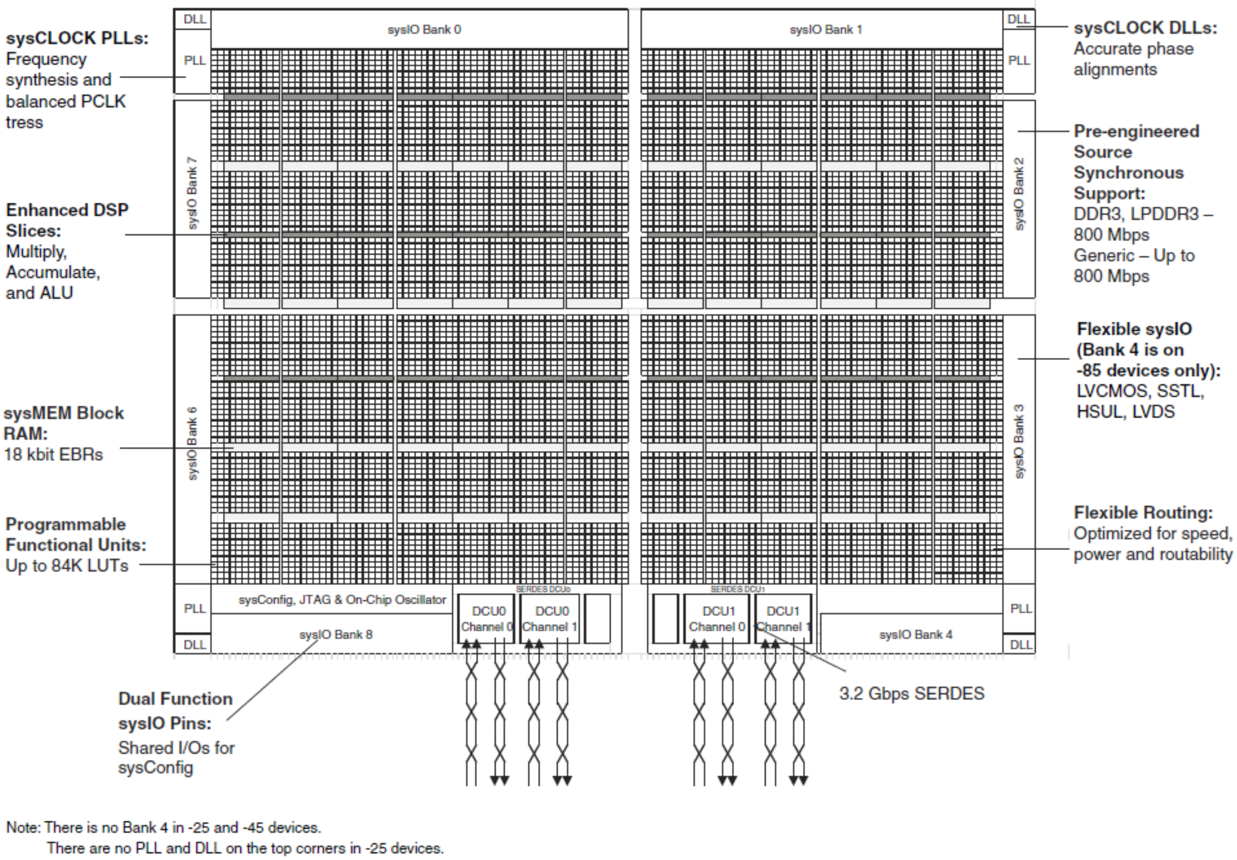

Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.

Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.

2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTL, LVPECL, and MIPI.

2.14.1. sysI/O Buffer Banks

ECP5/ECP5-5G devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank (Bank 8) is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O. For LFE5-85 devices, there is an additional I/O bank (Bank 4) that is not available in other device in the family.

In ECP5/ECP5-5G devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, the banks on the Left and Right sides of the device, have voltage reference input (shared I/O pin), VREF1 per bank, which allow it to be completely independent of each other. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5/ECP5-5G devices, single-ended output buffers and ratioed input buffers (LVTTL, and LVCMOS) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

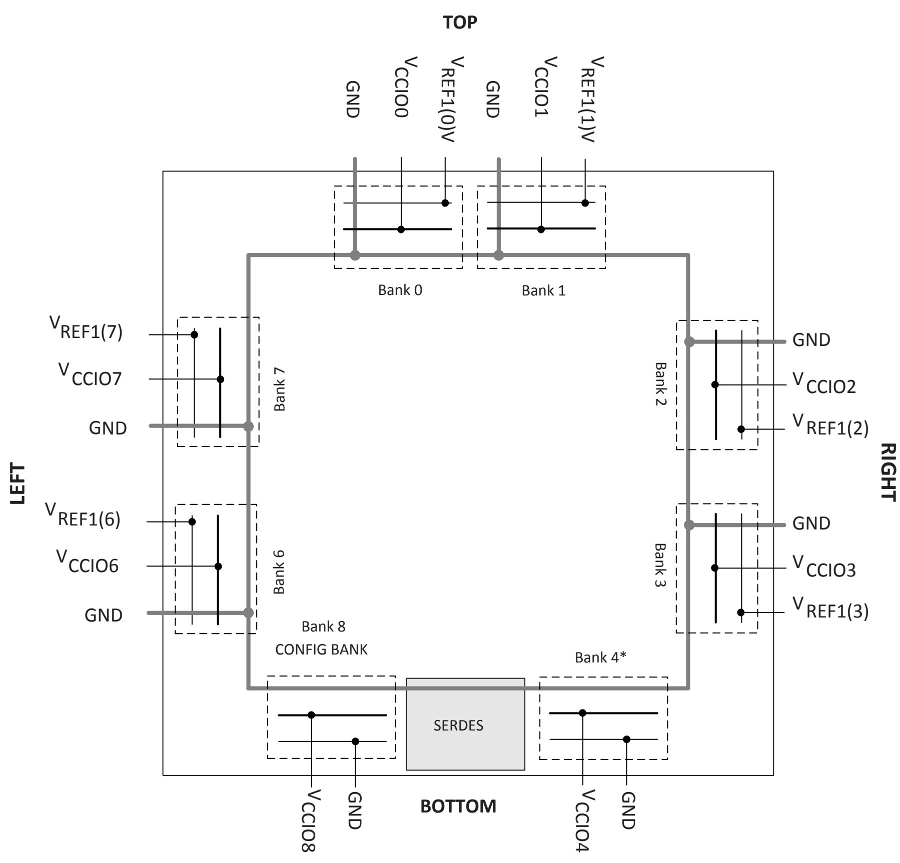

Figure 2.25. ECP5/ECP5-5G Device Family Banks

ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

- Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

  Bank 4 I/O only exists in the LFE5-85 device.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Diamond tool.

- Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).

2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. Figure 2.27 shows the position of the dual blocks for the LFE5-85. Table 2.13 shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2.15 lists the allowable combination of primary and secondary protocol combinations.

2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

Table 2.15 lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter			Min	Typ	Max	Unit
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC}, and V_{CCAUX}	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIOs} do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC}, V_{CCAUX}, and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash.

For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA}, before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \le V_{IN} \le V_{IH}$ (Max)	—	—	±1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \le V_{IN} < V_{CCIO}$	—	—	±1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5$ V	—	18	—	mA

Notes:

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ±1 mA.

3.14.6. LVPECL33

The ECP5/ECP5-5G devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.3 is one possible solution for point-to-point signals.

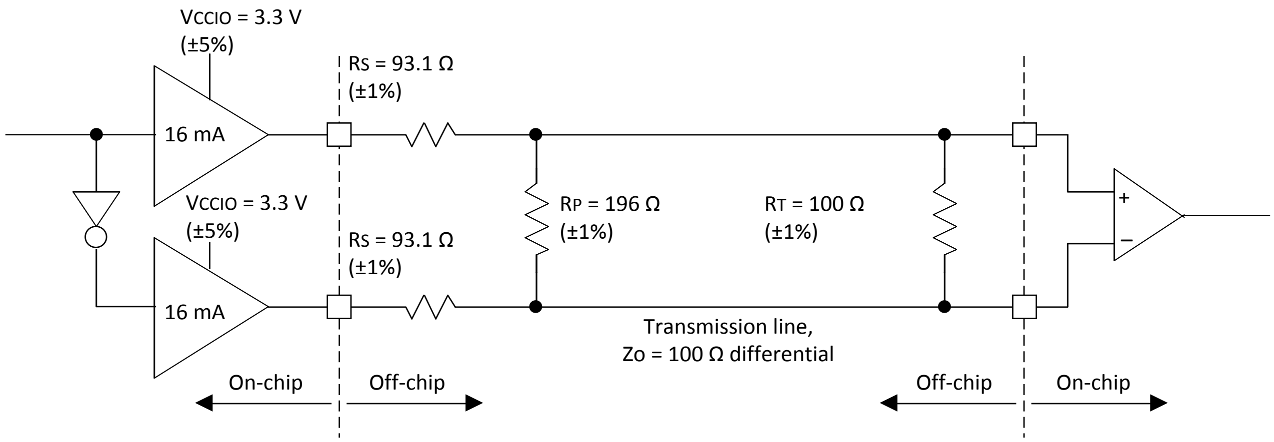

Figure 3.3. Differential LVPECL33

Over recommended operating conditions.

Table 3.16. LVPECL33 DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (±1%)	93	Ω
R_P	Driver Parallel Resistor (±1%)	196	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.14.7. MLVDS25

The ECP5/ECP5-5G devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.

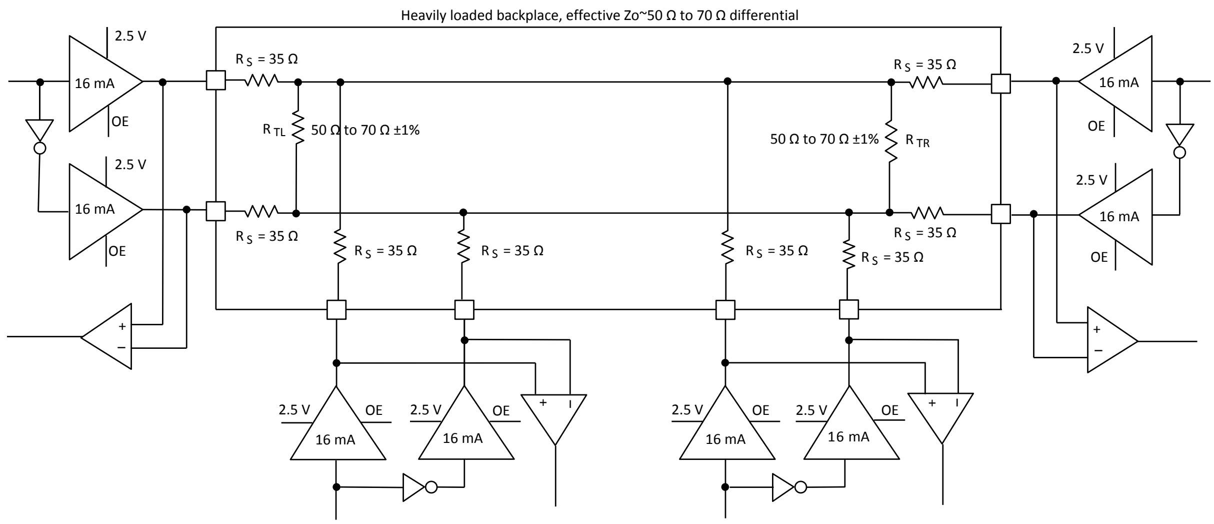

Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Table 3.17. MLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo=50 Ω	Zo=70 Ω	
V_{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (±1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (±1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.17. Maximum I/O Buffer Speed

Over recommended operating conditions.

Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
MIPI D-PHY (HS Mode)	MIPI Video	400	MHz
SLVS	SLVS similar to MIPI	400	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL_12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	200	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	200	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	200	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	200	MHz
LVCMOS15	LVCMOS 1.5, V_{CCIO} = 1.5 V	200	MHz
LVCMOS12	LVCMOS 1.2, V_{CCIO} = 1.2 V	200	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	150	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, VCCIO = 3.3 V	150	MHz
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	150	MHz
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	150	MHz
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	150	MHz
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	150	MHz
LVCMOS12 (For all drives)	LVCMOS, 1.2 V	150	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Switching Test Conditions, Table 3.44 on page 90.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks									
Primary Clock									
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
Edge Clock									
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
t_{SKEW_EDGE}	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
Generic SDR Input									
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL									
t_{CO}	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL									
t_{COPLL}	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns

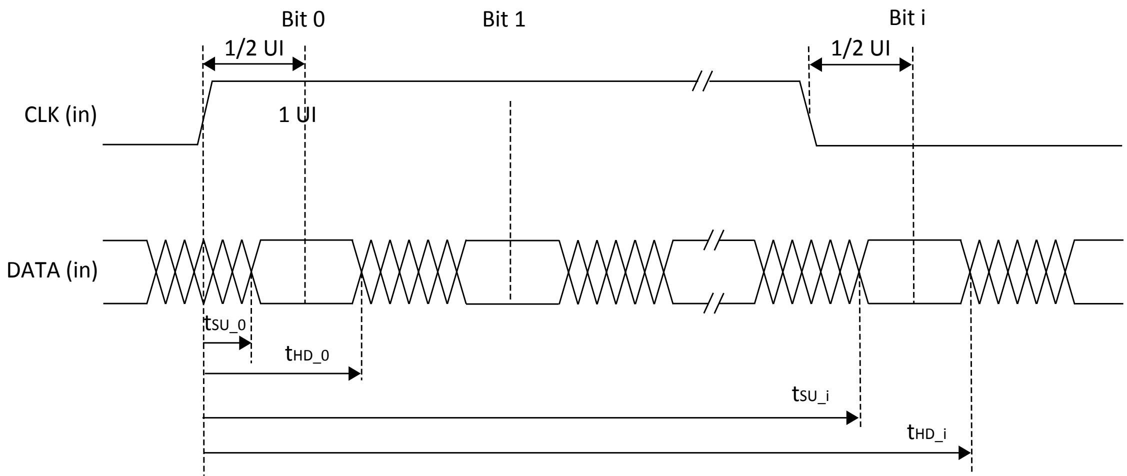

Figure 3.11. Receiver DDRX71_RX Waveforms

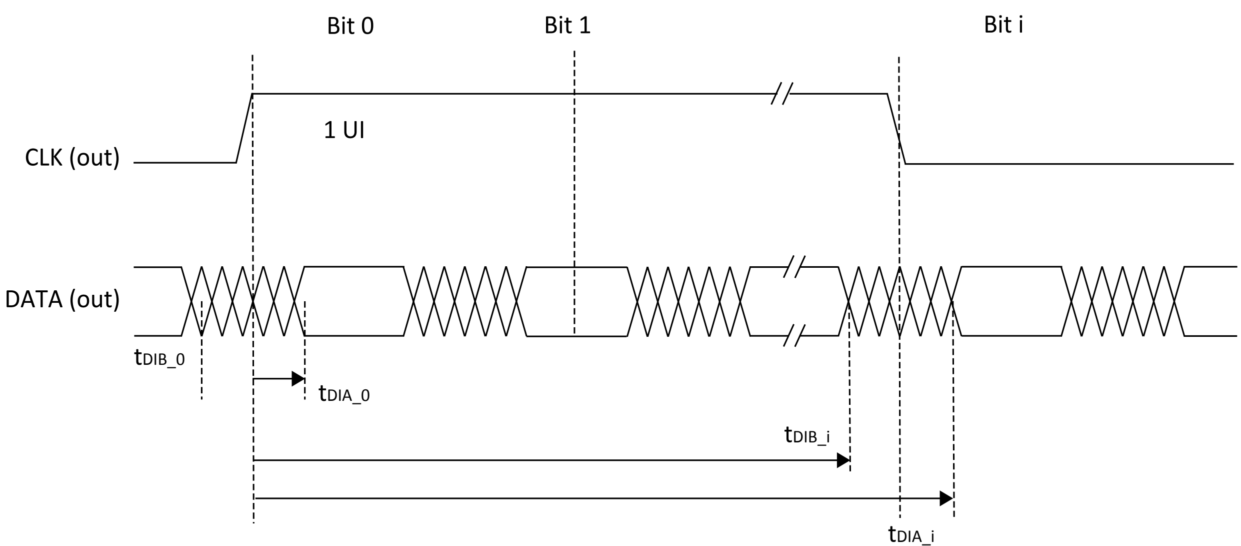

Figure 3.12. Transmitter DDRX71_TX Waveforms

3.27. XAUI/CPRI LV E.30 Electrical and Timing Characteristics

3.27.1. AC and DC Characteristics

Over recommended operating conditions.

Table 3.33. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	Ω
J_{TX_DDJ}[2, 3]	Output data deterministic jitter	—	—	—	0.17	UI
J_{TX_TJ}[1, 2, 3]	Total output data jitter	—	—	—	0.35	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Over recommended operating conditions.

Table 3.34. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J_{RX_DJ}[1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J_{RX_RJ}[1, 2, 3]	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J_{RX_SJ}[1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J_{RX_TJ}[1, 2, 3]	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening	—	0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

3.28. CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics

3.28.1. AC and DC Characteristics

Table 3.35. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}[1]	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	Ω
J_{TX_DDJ}[3, 4]	Output data deterministic jitter	—	—	—	0.17	UI
J_{TX_TJ}[2, 3, 4]	Total output data jitter	—	—	—	0.35	UI

Notes:

1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) *(Continued)*		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin
SERDES Function		
VCCAx	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCAx = 1.1 V for ECP5, VCCAx = 1.2 V for ECP5-5G.
VCCAUXAx	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUXAx = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes

5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	–6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	–7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	–8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	–6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	–7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	–8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	–6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	–7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	–8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	–6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	–7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	–8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	–6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	–7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	–8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	No

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Date	Version	Section	Change Summary
April 2017	1.7	All	Changed document number from DS1044 to FPGA-DS-02012.
		General Description	Updated Features section. Changed "1.1 V core power supply" to "1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G".
		Architecture	Updated Overview section. Change "The ECP5/ECP5-5G devices use 1.1 V as their core voltage" to "The ECP5 devices use 1.1V, ECP5UM5G devices use 1.2V as their core voltage"
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions Added ECP5-5G on VCC to be 1.2V +/- 5% Added ECP5-5G on VCCA to be 1.2V +/- 3% Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) Changed "Core Power Supply Current" for ICC on LFE5UM5G devices Changed "SERDES Power Supply Current (Per Dual)" for ICCA on LFE5UM5G devices Updated Table 3.20. Register-to-Register Performance. Remove "(DDR/SDR)" from DSP Function Changed DSP functions to 225 MHz
		Pinout Information	Update Section 4.1 Signal Description. Revised Vcc Description to "Power supply pins for core logic. Dedicated pins. VCC = 1.1 V (ECP5), 1.2 V (ECP5UM5G)"
February 2016	1.6	All	Changed document status from Preliminary to Final.
		General Description	Updated Features section. Changed "24K to 84K LUTs" to "12K to 84K LUTs". Added LFE5U-12 column to Table 1.1. ECP5 and ECP5-5G Family Selection Guide.
		DC and Switching Characteristics	Updated Power up Sequence section. Identified typical ICC current for specific devices in Table 3.8. ECP5/ECP5-5G Supply Current (Standby). Updated values in Table 3.9. ECP5. Updated values in Table 3.10. ECP5-5G. Added values to –8 Timing column of Table 3.19. Pin-to-Pin Performance. Added values to –8 Timing column of Table 3.20. Register-to-Register Performance. Changed LFE5-45 to All Devices in Table 3.22. ECP5/ECP5-5G External Switching Characteristics. Added table notes to Table 3.31. PCIe (5 Gb/s). Added table note to Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics.
		Pinout Information	Added LFE5U-12 column to the table in LFE5U section.
		Ordering Information	Updated LFE5U in ECP5/ECP5-5G Part Number Description section: added 12 F = 12K LUTs to Logic Capacity. Added LFE5U-12F information to Ordering Part Numbers section.

(Continued)

Date	Version	Section	Change Summary
November 2015	1.5	All	Added ECP5-5G device family.
			Changed document title to ECP5 and ECP5-5G Family Data Sheet.
	1.4	General Description	Updated Features section. Added support for eDP in RDR and HDR.
		Architecture	Updated Overview section. Revised Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level). Modified Flexible sysIO description and Note.
			Updated SERDES and Physical Coding Sublayer section. • Changed E.24.V in CPRI protocol to E.24.LV. • Removed “1.1 V” from paragraph on unused Dual.
		DC and Switching Characteristics	Updated Hot Socketing Requirements section. Revised V_{CCHTX} in table notes 1 and 3. Indicated V_{CCHTX} in table note 4.
			Updated SERDES High-Speed Data Transmitter section. Revised V_{CCHTX} in table note 1.
		Ordering Information	Updated ECP5/ECP5-5G Part Number Description section. Changed “LFE5 FPGA” under Device Family to “ECP5 FPGA”.
August 2015	1.3	General Description	Updated Features section. • Removed SMPTE3G under Embedded SERDES. • Added Single Event Upset (SEU) Mitigation Support. Removed SMPTE protocol in fifth paragraph.
		Architecture	General update.
		DC and Switching Characteristics	General update.
		Pinout Information	Updated Signal Descriptions section. Revised the descriptions of the following signals: • P[L/R] [Group Number]_[A/B/C/D] • P[T/B][Group Number]_[A/B] • D4/IO4 (Previously named D4/MOSI2/IO4) • D5/IO5 (Previously named D5/MISO/IO5) • VCCHRX_D[dual_num]CH[chan_num] • VCCHTX_D[dual_num]CH[chan_num]
		Supplemental Information	Added TN1184 reference.

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