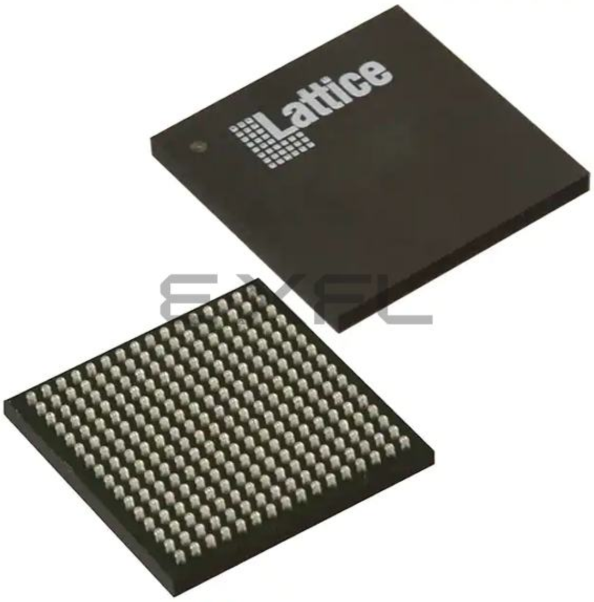
Lattice Semiconductor Corporation - LFE5U-45F-7BG256I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-7bg256i

2. Architecture

2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2.1 on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG™ ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.

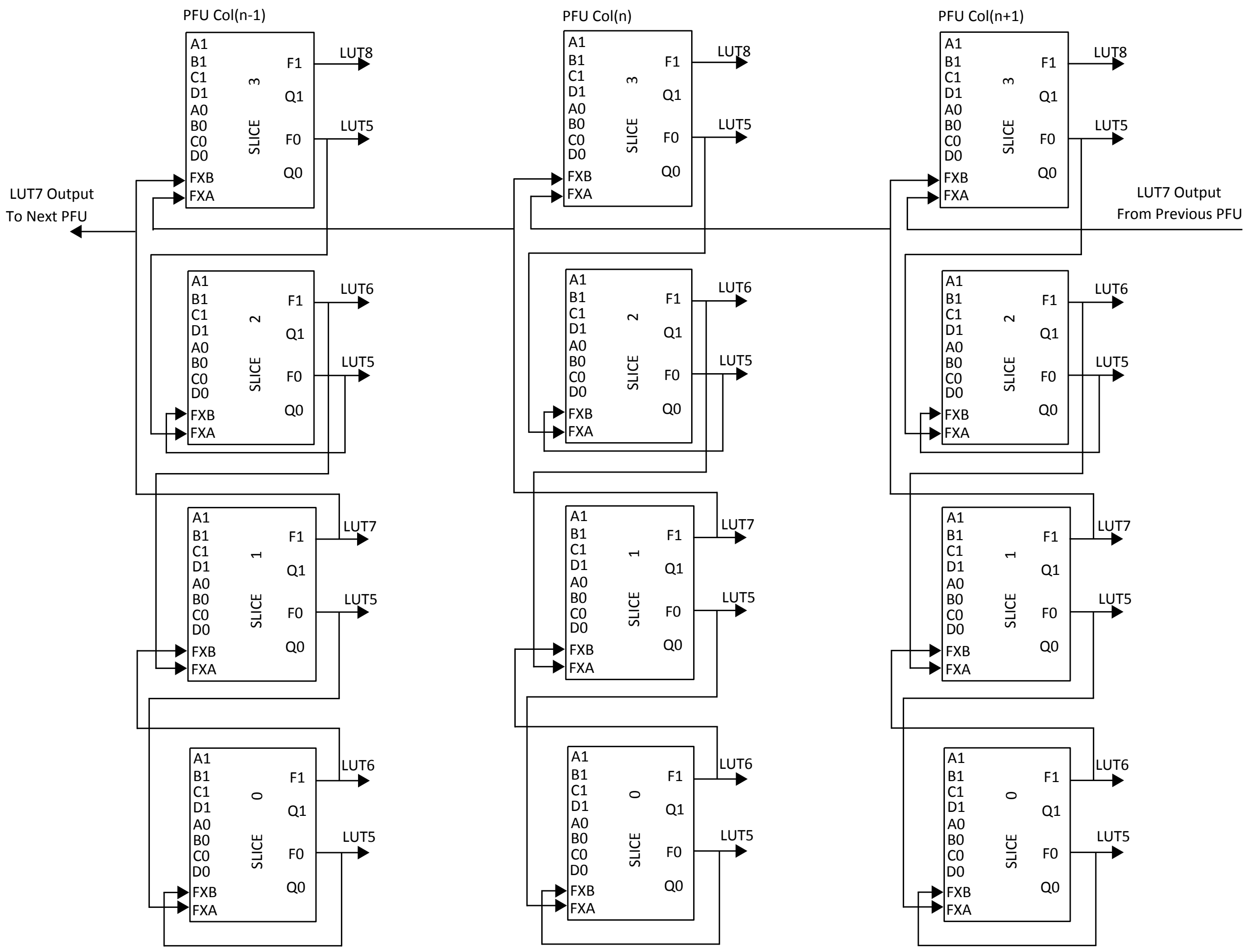


Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output[1]

Notes:

1. See Figure 2.3 on page 15 for connection details.
2. Requires two adjacent PFUs.

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

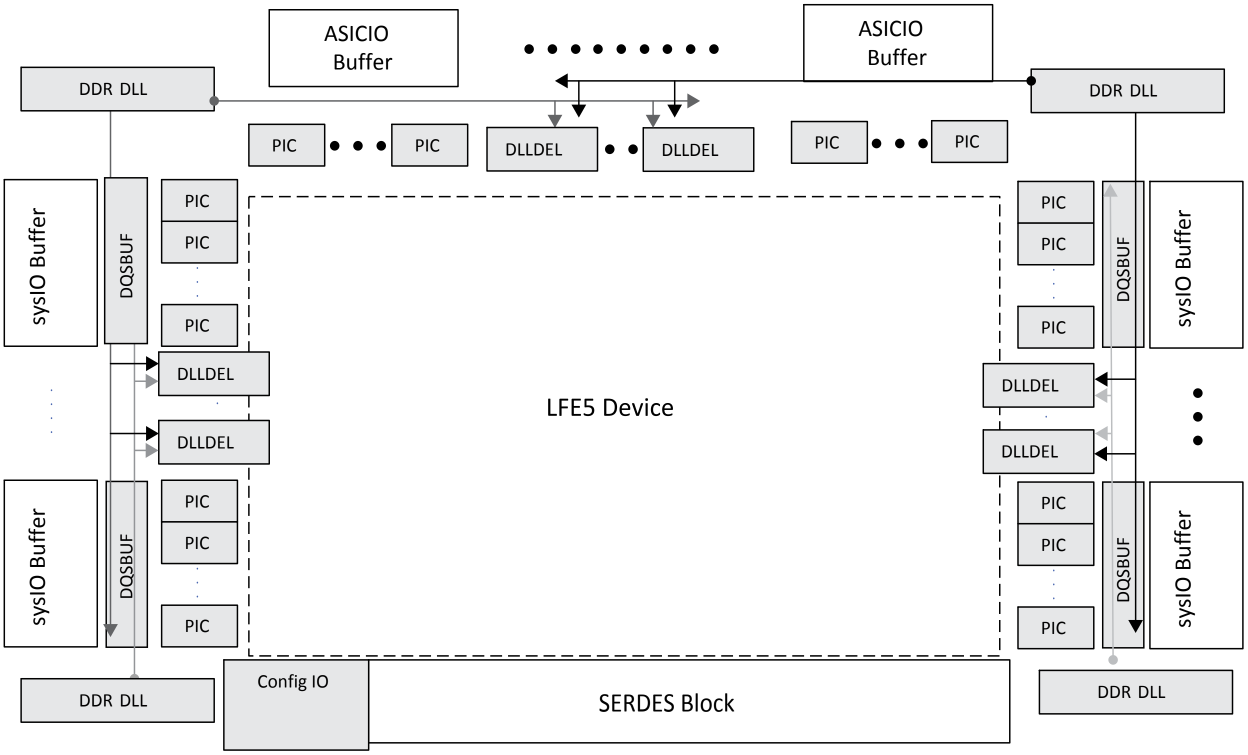


Figure 2.11. ECP5/ECP5-5G DLL Top Level View (For LFE-45 and LFE-85)

2.8. sysMEM Memory

ECP5/ECP5-5G devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

2.8.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.6 on page 25. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

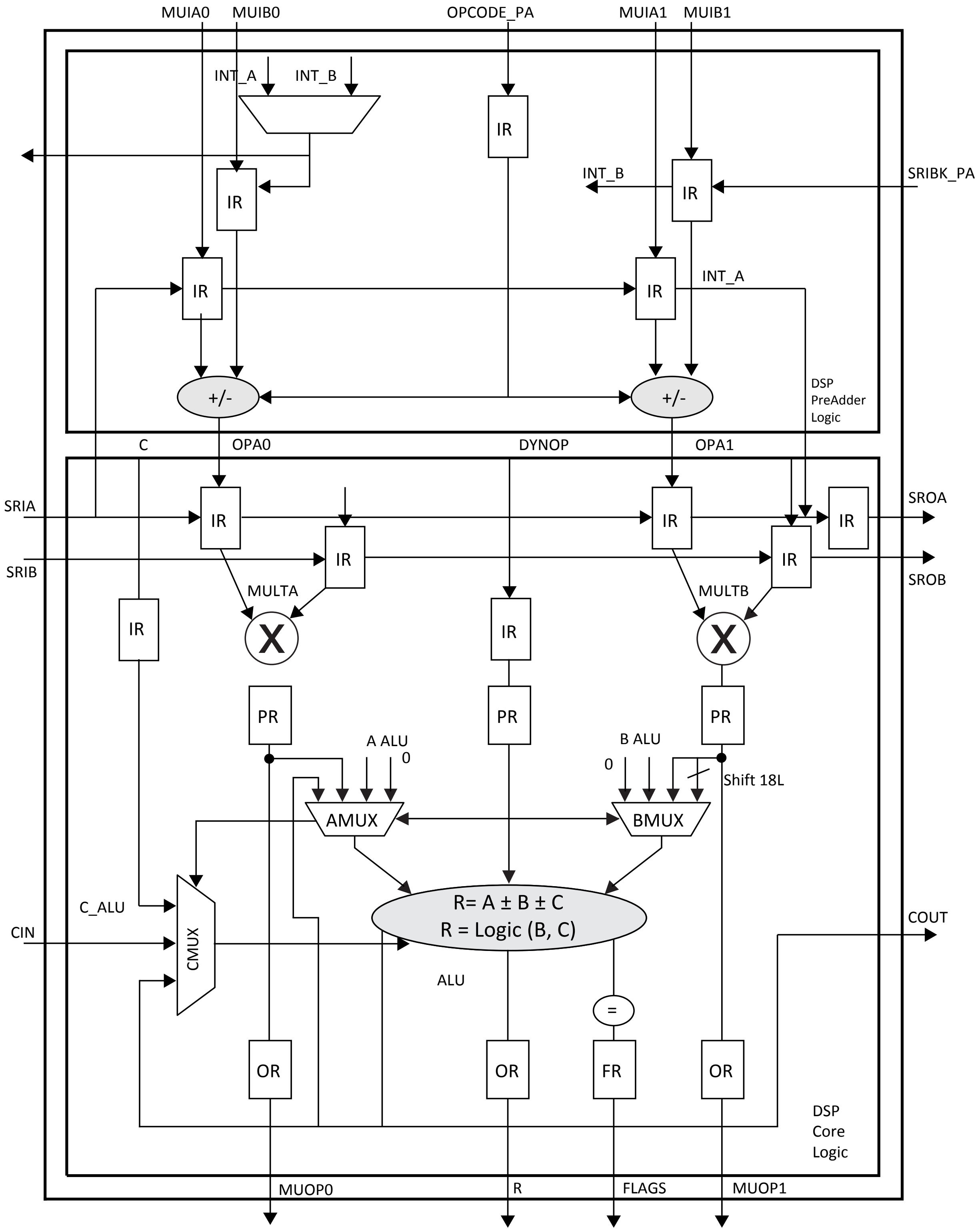


Figure 2.15. Detailed sysDSP Slice Diagram

In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note**: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

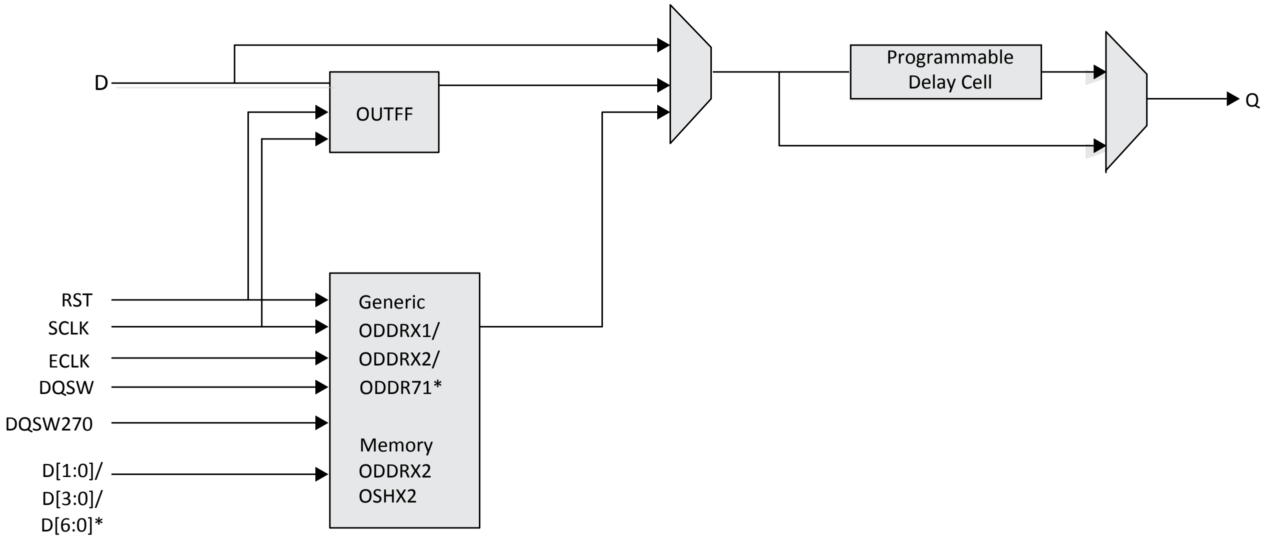
- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

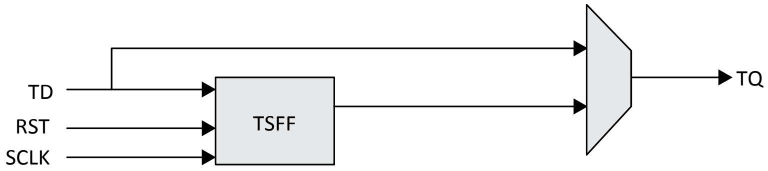


Figure 2.21. Tristate Register Block on Top Side

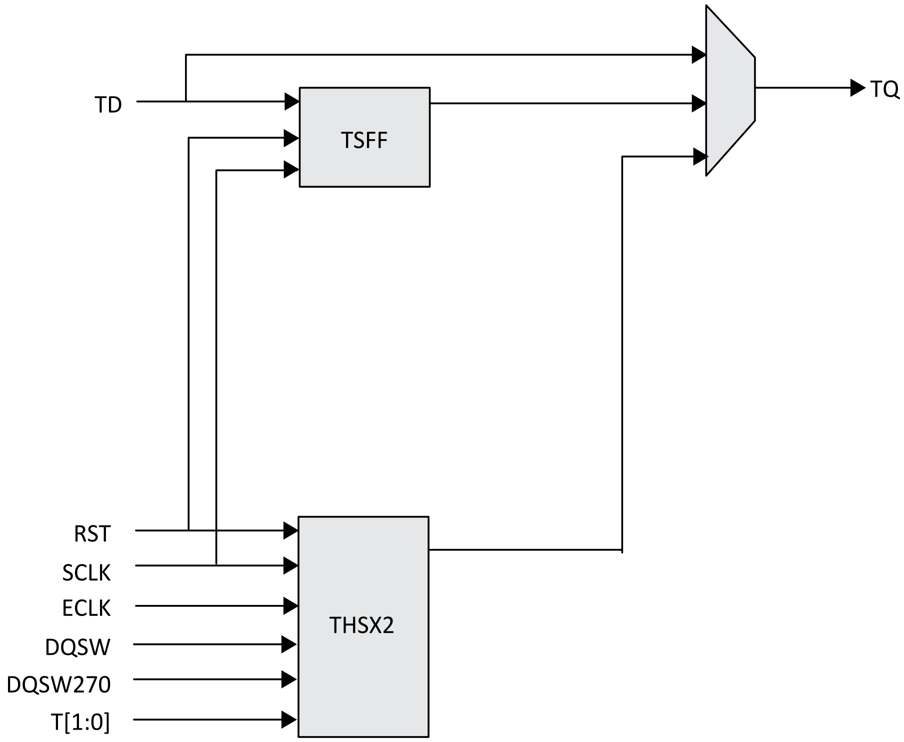


Figure 2.22. Tristate Register Block on Left and Right Sides

Table 2.10. Tristate Block Port Description

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR Register
RST	Input	Reset to the Tristate Block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.13. DDR Memory Support

2.13.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in Figure 2.23 on page 36. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as "virtual" VCCIO, by driving these pins to HIGH, with the user connecting these pins to VCCIO power supply. These connections create "soft" connections to V_{CCIO} thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

- Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

  Bank 4 I/O only exists in the LFE5-85 device.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Diamond tool.

- Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).

2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) – Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to Minimizing System Interruption During Configuration Using TransFR Technology (TN1087) for details.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.5	1.32	V
V_{CCA}	Supply Voltage	–0.5	1.32	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	–0.5	2.75	V
V_{CCIO}	Supply Voltage	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CCHRX}, V_{CCHTX}	SERDES RX/TX Buffer Supply Voltages	–0.5	1.32	V
—	Voltage Applied on SERDES Pins	–0.5	1.80	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
$V_{CC}{}^2$	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
$V_{CCAUX}{}^{2, 4}$	Auxiliary Supply Voltage	—	2.375	2.625	V
$V_{CCIO}{}^{2, 3}$	I/O Driver Supply Voltage	—	1.14	3.465	V
$V_{REF}{}^1$	Input Reference Voltage	—	0.5	1.0	V
t_{JCOM}	Junction Temperature, Commercial Operation	—	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	—	–40	100	°C
SERDES External Power Supply⁵					
V_{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V_{CCAUXA}	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
$V_{CCHRX}{}^6$	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V_{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 on page 48.
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
5. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

3.15. Typical Building Block Function Performance

Table 3.19. Pin-to-Pin Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	5.06	ns
32-Bit Decoder	6.08	ns
64-Bit Decoder	5.06	ns
4:1 Mux	4.45	ns
8:1 Mux	4.63	ns
16:1 Mux	4.81	ns
32:1 Mux	4.85	ns

Notes:

1. I/Os are configured with LVCMOS25 with V_{CCIO}=2.5, 12 mA drive.
2. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
3. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.17. Maximum I/O Buffer Speed

Over recommended operating conditions.

Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
MIPI D-PHY (HS Mode)	MIPI Video	400	MHz
SLVS	SLVS similar to MIPI	400	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL_12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	200	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	200	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	200	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	200	MHz
LVCMOS15	LVCMOS 1.5, V_{CCIO} = 1.5 V	200	MHz
LVCMOS12	LVCMOS 1.2, V_{CCIO} = 1.2 V	200	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	150	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, VCCIO = 3.3 V	150	MHz
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	150	MHz
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	150	MHz
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	150	MHz
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	150	MHz
LVCMOS12 (For all drives)	LVCMOS, 1.2 V	150	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Switching Test Conditions, Table 3.44 on page 90.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

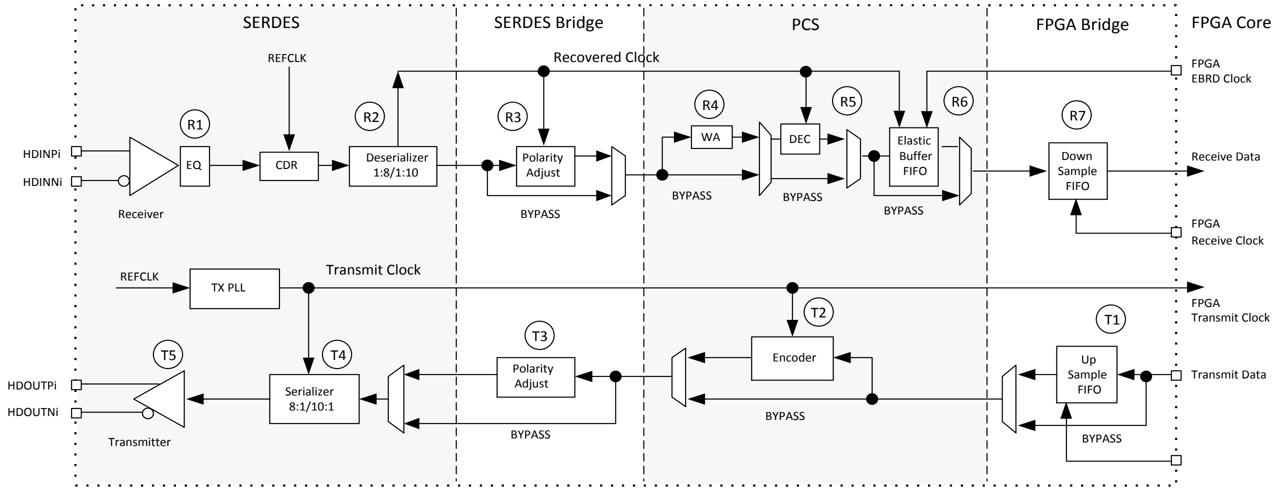


Figure 3.13. Transmitter and Receiver Latency Block Diagram

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss (without package)	—	—	–10	dB

Notes:

1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Notes:

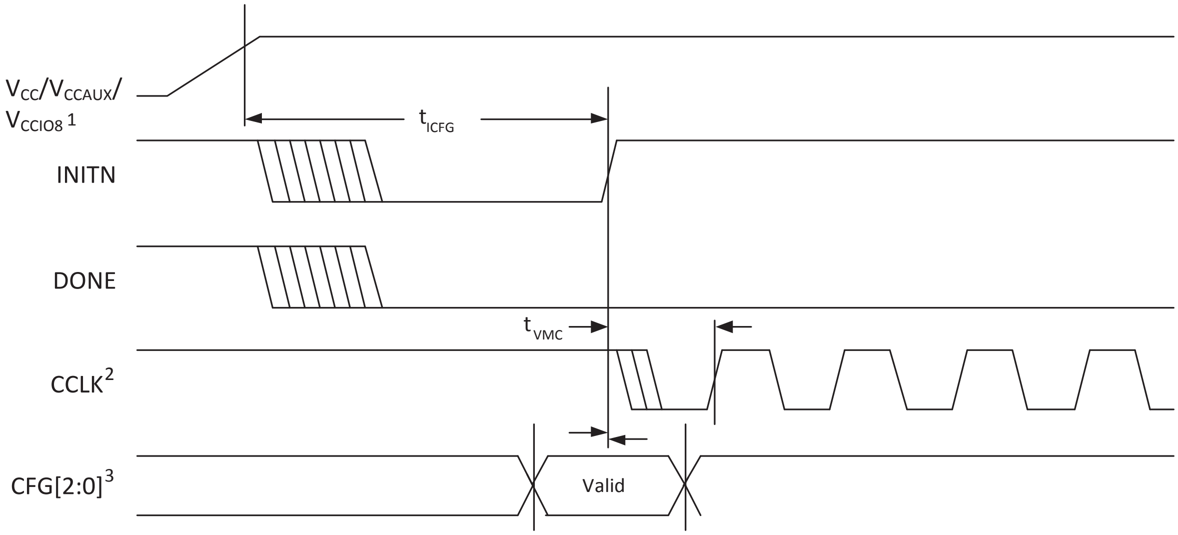
1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

Table 3.31. PCIe (5 Gb/s) *(Continued)*

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Receive[1, 2]						
UI	Unit Interval	—	199.94	200	200.06	ps
$V_{RX\text{-}DIFF\text{-}PP}$	Differential Rx peak-peak voltage	—	0.34[3]	—	1.2	V, p-p
$T_{RX\text{-}RJ\text{-}RMS}$	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	—	—	4.2	ps, RMS
$T_{RX\text{-}DJ}$	Receiver deterministic jitter tolerance	—	—	—	88	ps
$V_{RX\text{-}CM\text{-}AC}$	Common mode noise from Rx	—	—	—		mV, p-p
$RL_{RX\text{-}DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
$RL_{RX\text{-}CM}$	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
$Z_{RX\text{-}DC}$	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Receiver DC single ended impedance when powered down	—	200K	—	—	Ω
$V_{RX\text{-}CM\text{-}AC\text{-}P}$	Rx AC peak common mode voltage	—	—	—		mV, peak
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$	Electrical Idle Detect Threshold	—	65	—	340[3]	mv,
$L_{RX\text{-}SKEW}$	Receiver lane-lane skew	—	—	—	8	ns

Notes:

1. Values are measured at 5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express standard.



1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hardwired).

Figure 3.18. Power-On-Reset (POR) Timing

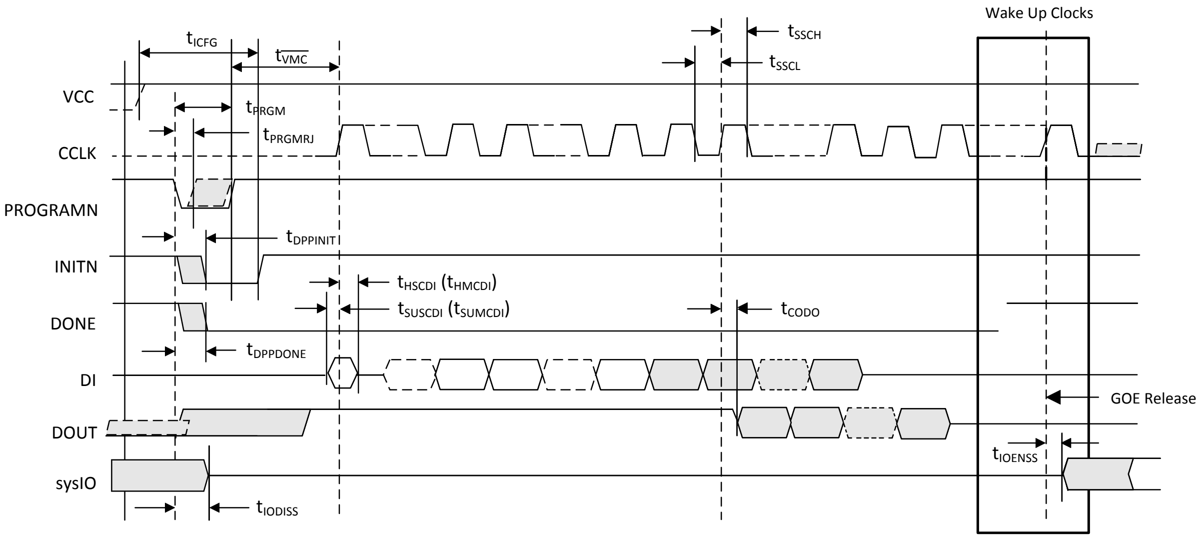


Figure 3.19. sysCONFIG Port Timing

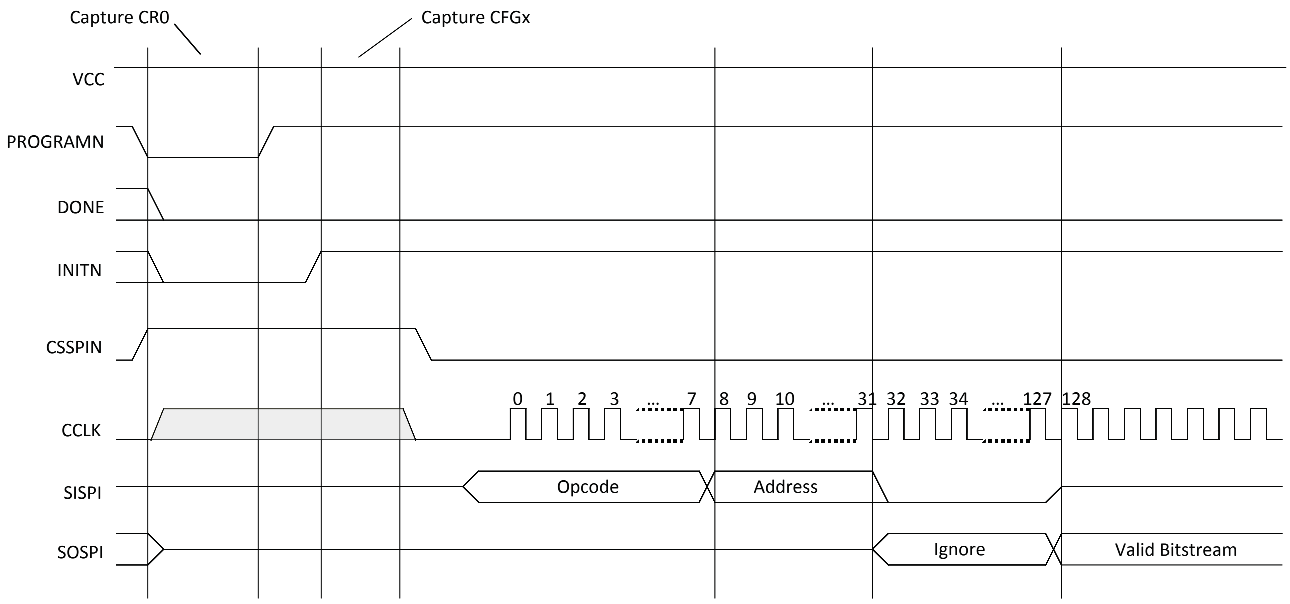


Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) *(Continued)*		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin
SERDES Function		
VCCAx	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCAx = 1.1 V for ECP5, VCCAx = 1.2 V for ECP5-5G.
VCCAUXAx	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUXAx = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

(Continued)

Date	Version	Section	Change Summary
November 2015	1.5	All	Added ECP5-5G device family.
			Changed document title to ECP5 and ECP5-5G Family Data Sheet.
	1.4	General Description	Updated Features section. Added support for eDP in RDR and HDR.
		Architecture	Updated Overview section. Revised Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level). Modified Flexible sysIO description and Note.
			Updated SERDES and Physical Coding Sublayer section. • Changed E.24.V in CPRI protocol to E.24.LV. • Removed "1.1 V" from paragraph on unused Dual.
		DC and Switching Characteristics	Updated Hot Socketing Requirements section. Revised V_{CCHTX} in table notes 1 and 3. Indicated V_{CCHTX} in table note 4.
			Updated SERDES High-Speed Data Transmitter section. Revised V_{CCHTX} in table note 1.
		Ordering Information	Updated ECP5/ECP5-5G Part Number Description section. Changed "LFE5 FPGA" under Device Family to "ECP5 FPGA".
August 2015	1.3	General Description	Updated Features section. • Removed SMPTE3G under Embedded SERDES. • Added Single Event Upset (SEU) Mitigation Support. Removed SMPTE protocol in fifth paragraph.
		Architecture	General update.
		DC and Switching Characteristics	General update.
		Pinout Information	Updated Signal Descriptions section. Revised the descriptions of the following signals: • P[L/R] [Group Number]_[A/B/C/D] • P[T/B][Group Number]_[A/B] • D4/IO4 (Previously named D4/MOSI2/IO4) • D5/IO5 (Previously named D5/MISO/IO5) • VCCHRX_D[dual_num]CH[chan_num] • VCCHTX_D[dual_num]CH[chan_num]
		Supplemental Information	Added TN1184 reference.