# Lattice Semiconductor Corporation - LFE5U-45F-7BG381I Datasheet

**Welcome to E-XFL.COM**

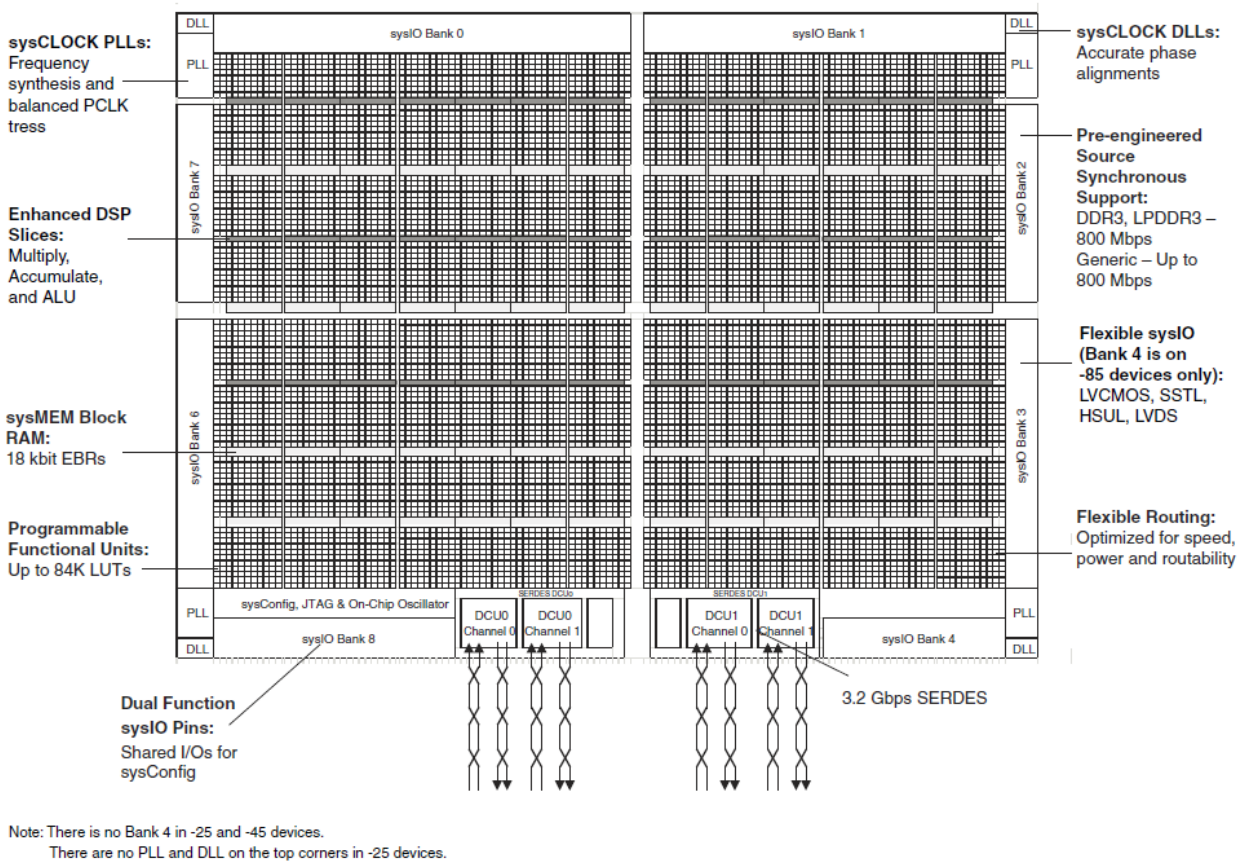
## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 11000 |
| Number of Logic Elements/Cells | 44000 |
| Total RAM Bits | 1990656 |
| Number of I/O | 203 |
| Number of Gates | - |
| Voltage - Supply | 1.045V ~ 1.155V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 381-FBGA |
| Supplier Device Package | 381-CABGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-7bg381i |



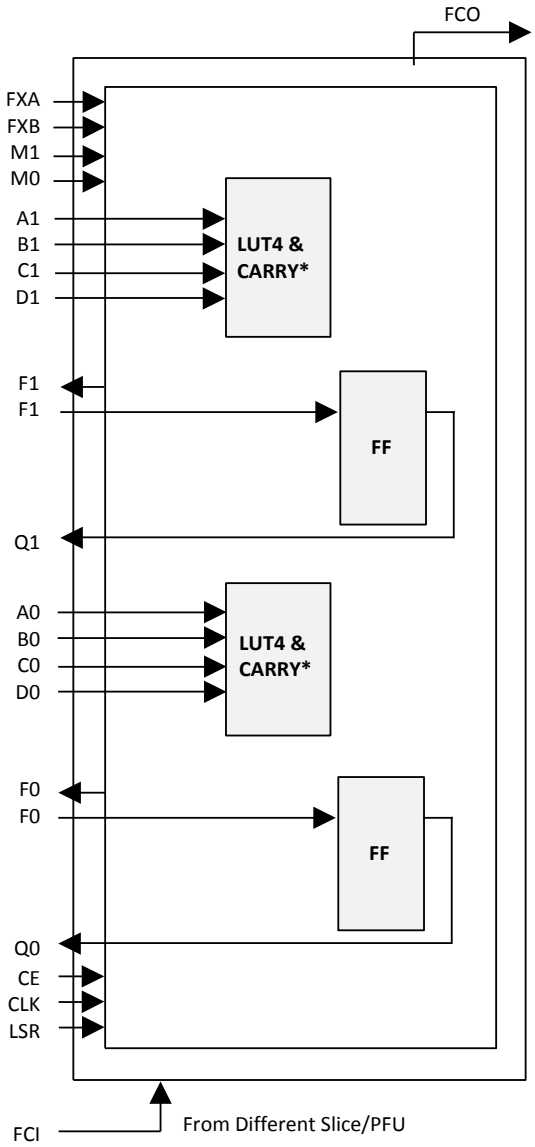

Note: There is no Bank 4 in -25 and -45 devices.
There are no PLL and DLL on the top corners in -25 devices.

**Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)**

## 2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.




**Notes**: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

**Figure 2.3. Slice Diagram**

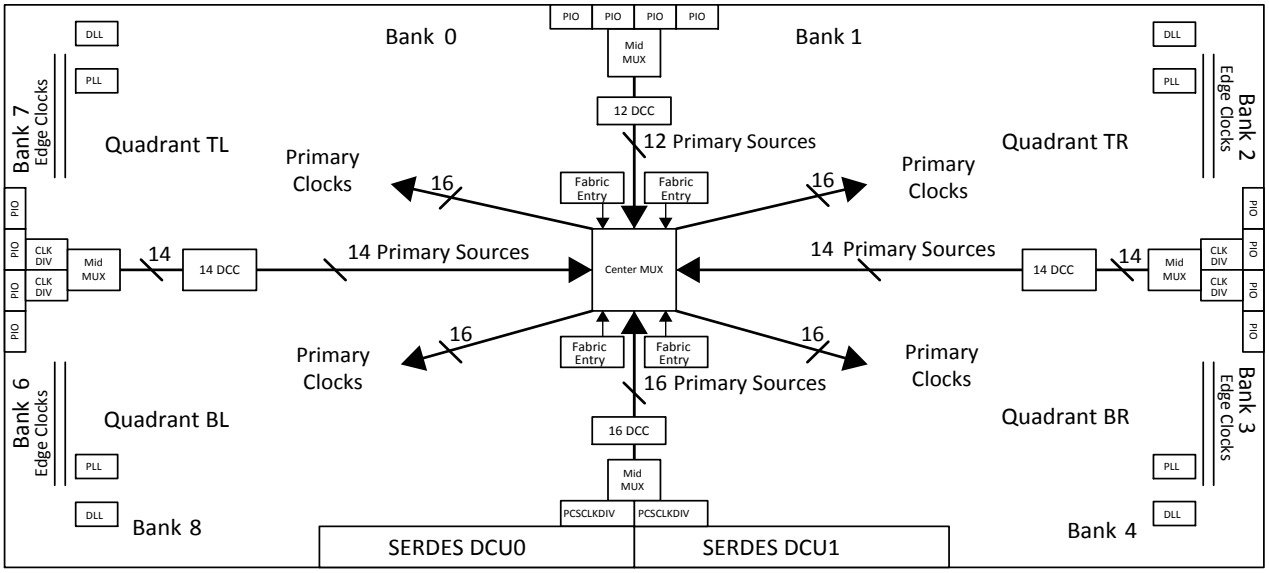



**Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking**

## 2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

### 2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

#### 2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

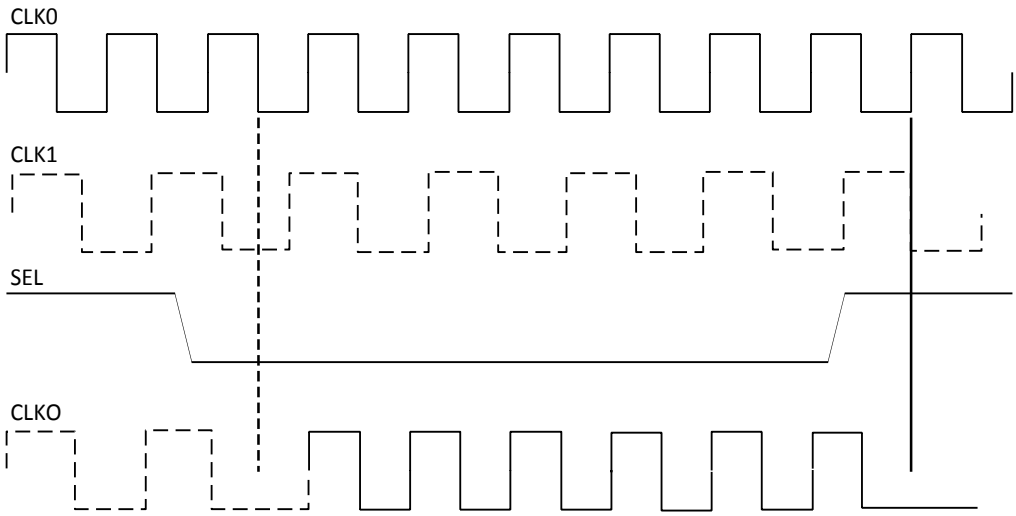



**Figure 2.7. DCS Waveforms**

### 2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

**Table 2.7. Maximum Number of Elements in a Slice**

| Width of Multiply | x9 | x18 | x36 |
|---|---|---|---|
| MULT | 4 | 2 | 1/2 |
| MAC | 1 | 1 | — |
| MULTADDSUB | 2 | 1 | — |
| MULTADDSUBSUM | 1* | 1/2 | — |

***Note**: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

## 2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

#### 2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in DDR Memory Support section on page 35.

**Table 2.8. Input Block Port Description**

| Name | Type | Description |
|---|---|---|
| D | Input | High Speed Data Input |
| Q[1:0]/Q[3:0]/Q[6:0] | Output | Low Speed Data to the device core |
| RST | Input | Reset to the Output Block |
| SCLK | Input | Slow Speed System Clock |
| ECLK | Input | High Speed Edge Clock |
| DQS | Input | Clock from DQS control Block used to clock DDR memory data |
| ALIGNWD | Input | Data Alignment signal from device core. |

### 2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in Figure 2.19. The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

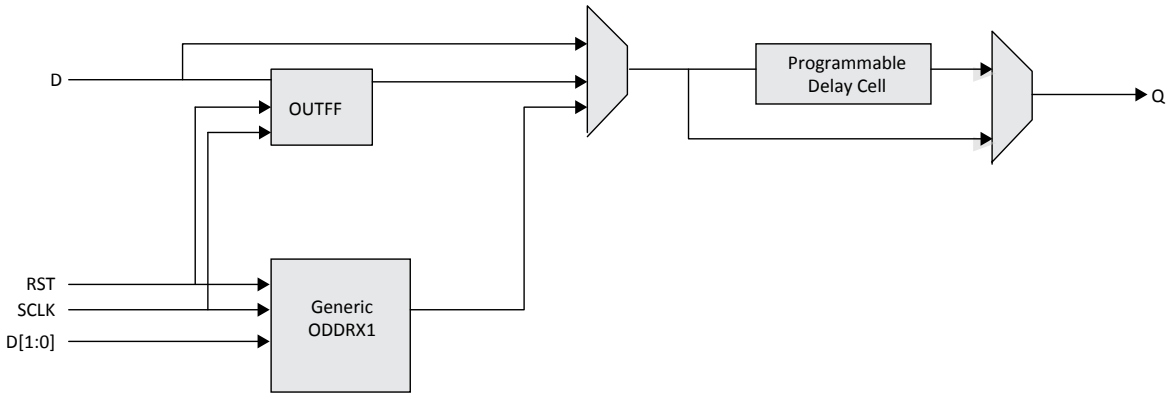



**Figure 2.19. Output Register Block on Top Side**

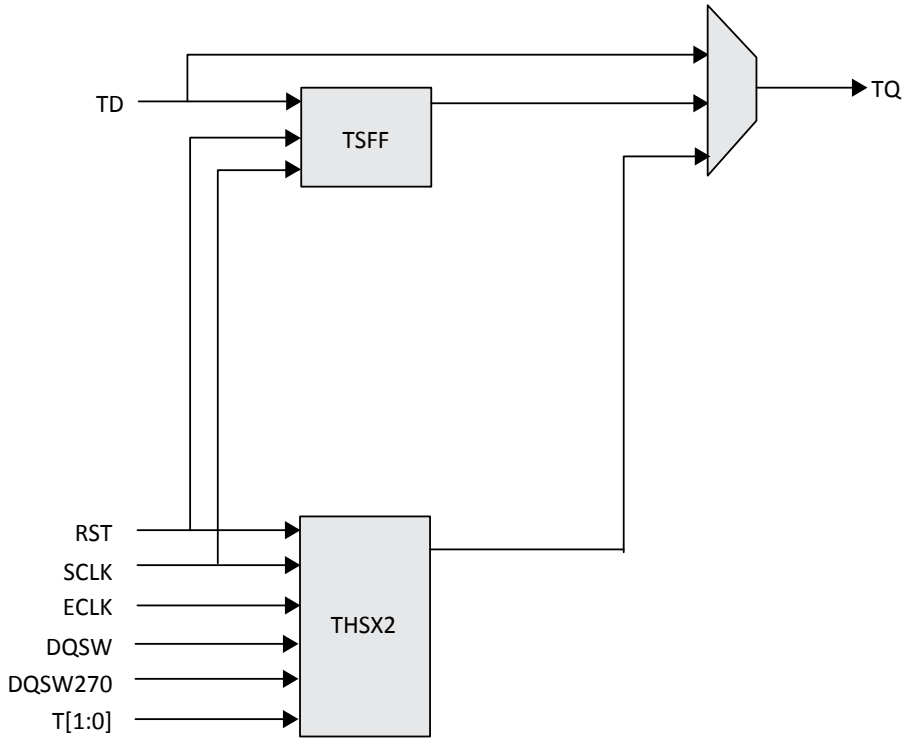



**Figure 2.22. Tristate Register Block on Left and Right Sides**

**Table 2.10. Tristate Block Port Description**

| Name | Type | Description |
|---|---|---|
| TD | Input | Tristate Input to Tristate SDR Register |
| RST | Input | Reset to the Tristate Block |
| TD[1:0] | Input | Tristate input to TSHX2 function |
| SCLK | Input | Slow Speed System Clock |
| ECLK | Input | High Speed Edge Clock |
| DQSW | Input | Clock from DQS control Block used to generate DDR memory DQS output |
| DQSW270 | Input | Clock from DQS control Block used to generate DDR memory DQ output |
| TQ | Output | Output of the Tristate block |

## 2.13. DDR Memory Support

### 2.13.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in Figure 2.23 on page 36. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as "virtual" VCCIO, by driving these pins to HIGH, with the user connecting these pins to VCCIO power supply. These connections create "soft" connections to $V_{CCIO}$ thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

## 2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.

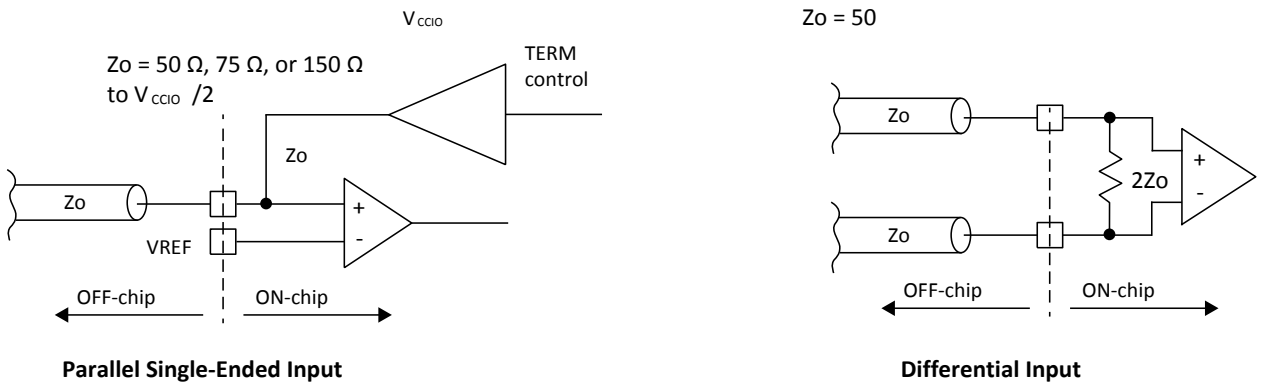



**Figure 2.26. On-Chip Termination**

See Table 2.12 for termination options for input modes.

**Table 2.12. On-Chip Termination Options for Input Modes**

| IO_TYPE | Terminate to $V_{CCIO}/2$* | Differential Termination Resistor* |
|---|---|---|
| LVDS25 | — | 100 |
| BLVDS25 | — | 100 |
| MLVDS | — | 100 |
| LVPECL33 | — | 100 |
| subLVDS | — | 100 |
| SLVS | — | 100 |
| HSUL12 | 50, 75, 150 | — |
| HSUL12D | — | 100 |
| SSTL135_I / II | 50, 75, 150 | — |
| SSTL135D_I / II | — | 100 |
| SSTL15_I / II | 50, 75, 150 | — |
| SSTL15D_I / II | — | 100 |
| SSTL18_I / II | 50, 75, 150 | — |
| SSTL18D_I / II | — | 100 |

***Notes**:

TERMINATE to $V_{CCIO}/2$ (Single-Ended) and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance ±20%.

Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for on-chip termination usage and value ranges.

## 2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the Hot Socketing Specifications section on page 48.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

### 2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

**Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)**

| MCLK Frequency (MHz) |
|---|
| 2.4 |
| 4.8 |
| 9.7 |
| 19.4 |
| 38.8 |
| 62 |

## 2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

# 3. DC and Switching Characteristics

## 3.1. Absolute Maximum Ratings

**Table 3.1. Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.5 | 1.32 | V |
| $V_{CCA}$ | Supply Voltage | –0.5 | 1.32 | V |
| $V_{CCAUX}$, $V_{CCAUXA}$ | Supply Voltage | –0.5 | 2.75 | V |
| $V_{CCIO}$ | Supply Voltage | –0.5 | 3.63 | V |
| — | Input or I/O Transient Voltage Applied | –0.5 | 3.63 | V |
| $V_{CCHRX}$, $V_{CCHTX}$ | SERDES RX/TX Buffer Supply Voltages | –0.5 | 1.32 | V |
| — | Voltage Applied on SERDES Pins | –0.5 | 1.80 | V |
| $T_A$ | Storage Temperature (Ambient) | –65 | 150 | °C |
| $T_J$ | Junction Temperature | — | +125 | °C |

**Notes**:
1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

## 3.2. Recommended Operating Conditions

**Table 3.2. Recommended Operating Conditions**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$[2] | Core Supply Voltage | ECP5 | 1.045 | 1.155 | V |
| | | ECP5-5G | 1.14 | 1.26 | V |
| $V_{CCAUX}$[2, 4] | Auxiliary Supply Voltage | — | 2.375 | 2.625 | V |
| $V_{CCIO}$[2, 3] | I/O Driver Supply Voltage | — | 1.14 | 3.465 | V |
| $V_{REF}$[1] | Input Reference Voltage | — | 0.5 | 1.0 | V |
| $t_{JCOM}$ | Junction Temperature, Commercial Operation | — | 0 | 85 | °C |
| $t_{JIND}$ | Junction Temperature, Industrial Operation | — | –40 | 100 | °C |
| **SERDES External Power Supply**[5] | | | | | |
| $V_{CCA}$ | SERDES Analog Power Supply | ECP5UM | 1.045 | 1.155 | V |
| | | ECP5-5G | 1.164 | 1.236 | V |
| $V_{CCAUXA}$ | SERDES Auxiliary Supply Voltage | — | 2.374 | 2.625 | V |
| $V_{CCHRX}$[6] | SERDES Input Buffer Power Supply | ECP5UM | 0.30 | 1.155 | V |
| | | ECP5-5G | 0.30 | 1.26 | V |
| $V_{CCHTX}$ | SERDES Output Buffer Power Supply | ECP5UM | 1.045 | 1.155 | V |
| | | ECP5-5G | 1.14 | 1.26 | V |

**Notes**:
1. For correct operation, all supplies except $V_{REF}$ must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 on page 48.
4. $V_{CCAUX}$ ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
5. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for information on board considerations for SERDES power supplies.
6. $V_{CCHRX}$ is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

## 3.3. Power Supply Ramp Rates

**Table 3.3. Power Supply Ramp Rates**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{RAMP}$ | Power Supply ramp rates for all supplies | 0.01 | — | 10 | V/ms |

**Note**: Assumes monotonic ramp rates.

## 3.4. Power-On-Reset Voltage Levels

**Table 3.4. Power-On-Reset Voltage Levels**

| Symbol | Parameter | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{PORUP}$ | All Devices | Power-On-Reset ramp-up trip point (Monitoring $V_{CC}$, $V_{CCAUX}$, and $V_{CCIO8}$) | $V_{CC}$ | 0.90 | — | 1.00 | V |
| | | | $V_{CCAUX}$ | 2.00 | — | 2.20 | V |
| | | | $V_{CCIO8}$ | 0.95 | — | 1.06 | V |
| $V_{PORDN}$ | All Devices | Power-On-Reset ramp-down trip point (Monitoring $V_{CC}$, and $V_{CCAUX}$ | $V_{CC}$ | 0.77 | — | 0.87 | V |
| | | | $V_{CCAUX}$ | 1.80 | — | 2.00 | V |

**Notes**:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only $V_{CCIO8}$ has a Power-On-Reset ramp up trip point. All other $V_{CCIOs}$ do not have Power-On-Reset ramp up detection.
- $V_{CCIO8}$ does not have a Power-On-Reset ramp down detection. $V_{CCIO8}$ must remain within the Recommended Operating Conditions to ensure proper operation.

## 3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when $V_{CC}$, $V_{CCAUX}$, and $V_{CCIO8}$ are ramped above the $V_{PORUP}$ voltage, as specified above.

$V_{CCIO8}$ controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp $V_{CCIO8}$ above $V_{IH}$ of the external SPI Flash, before at least one of the other two supplies ($V_{CC}$ and/or $V_{CCAUX}$) is ramped to $V_{PORUP}$ voltage level. If the system cannot meet this power up sequence requirement, and requires the $V_{CCIO8}$ to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until $V_{CCIO8}$ reaches $V_{IH}$ of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the $V_{IH}$ voltage requirement of the SPI Flash.

For LFE5UM/LFE5UM5G devices, it is required to power up $V_{CCA}$, before $V_{CCAUXA}$ is powered up.

## 3.6. Hot Socketing Specifications

**Table 3.5. Hot Socketing Specifications**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IDK_HS | Input or I/O Leakage Current for Top and Bottom Banks Only | $0 \le V_{IN} \le V_{IH}$ (Max) | — | — | ±1 | mA |
| IDK | Input or I/O Leakage Current for Left and Right Banks Only | $0 \le V_{IN} < V_{CCIO}$ | — | — | ±1 | mA |
| | | $V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5$ V | — | 18 | — | mA |

**Notes**:

1. $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$ should rise/fall monotonically.
2. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the $I_{DK}$ current can exceed ±1 mA.

## 3.7. Hot Socketing Requirements

**Table 3.6. Hot Socketing Requirements**

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input current per SERDES I/O pin when device is powered down and inputs driven. | — | — | 8 | mA |
| Input current per HDIN pin when device power supply is off, inputs driven[1, 2] | — | — | 15 | mA |
| Current per HDIN pin when device power ramps up, input driven[3] | — | — | 50 | mA |
| Current per HDOUT pin when device power supply is off, outputs pulled up[4] | — | — | 30 | mA |

**Notes**:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output $V_{CCHTX}$, 8b/10b data, no external AC coupling.
2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.
3. Device power supplies are ramping up ($V_{CCA}$ and $V_{CCAUX}$), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output $V_{CCHTX}$, 8b/10b data, internal AC coupling.
4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to $V_{CCHTX}$ by the far end receiver termination of 50 Ω single ended.

## 3.8. ESD Performance

Refer to the ECP5 and ECP5-5G Product Family Qualification Summary for complete qualification data, including ESD performance.

## 3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

**Table 3.7. DC Electrical Characteristics**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 4] | Input or I/O Low Leakage | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 10 | µA |
| $I_{IH}$[1, 3] | Input or I/O High Leakage | $V_{CCIO} < V_{IN} \le V_{IH(MAX)}$ | — | — | 100 | µA |
| $I_{PU}$ | I/O Active Pull-up Current, sustaining logic HIGH state | $0.7\ V_{CCIO} \le V_{IN} \le V_{CCIO}$ | –30 | — | — | µA |
| | I/O Active Pull-up Current, pulling down from logic HIGH state | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | — | — | –150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current, sustaining logic LOW state | $0 \le V_{IN} \le V_{IL}$ (MAX) | 30 | — | — | µA |
| | I/O Active Pull-down Current, pulling up from logic LOW state | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 150 | µA |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = 1.2 V, $V_{IO}$ = 0 to $V_{IH(MAX)}$ | — | 5 | 8 | pf |
| C2 | Dedicated Input Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = 1.2 V, $V_{IO}$ = 0 to $V_{IH(MAX)}$ | — | 5 | 7 | pf |
| $V_{HYST}$ | Hysteresis for Single-Ended Inputs | $V_{CCIO}$ = 3.3 V | — | 300 | — | mV |
| | | $V_{CCIO}$ = 2.5 V | — | 250 | — | mV |

**Notes**:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25 °C, f = 1.0 MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as $V_{REF}$, maximum leakage= 25 µA.

## 3.10. Supply Current (Standby)

Over recommended operating conditions.

**Table 3.8. ECP5/ECP5-5G Supply Current (Standby)**

| Symbol | Parameter | Device | Typical | Unit |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | LFE5U-12F/ LFE5U-25F/ LFE5UM-25F | 77 | mA |
| | | LFE5UM5G-25F | 77 | mA |
| | | LFE5U-45F/ LFE5UM-45F | 116 | mA |
| | | LFE5UM5G-45F | 116 | mA |
| | | LFE5U-85F/ LFE5UM-85F | 212 | mA |
| | | LFE5UM5G-85F | 212 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F | 16 | mA |
| | | LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F | 17 | mA |
| | | LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F | 26 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F | 0.5 | mA |
| | | LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F | 0.5 | mA |
| | | LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F | 0.5 | mA |
| $I_{CCA}$ | SERDES Power Supply Current (Per Dual) | LFE5UM-25F | 11 | mA |
| | | LFE5UM5G-25F | 12 | mA |
| | | LFE5UM-45F | 9.5 | mA |
| | | LFE5UM5G-45F | 11 | mA |
| | | LFE5UM-85F | 9.5 | mA |
| | | LFE5UM5G-85F | 11 | mA |

**Notes**:

- For further information on supply current, see the list of technical documentation in Supplemental Information section on page 102.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
- Frequency 0 Hz.
- Pattern represents a “blank” configuration data file.
- $T_J$ = 85 °C, power supplies at nominal voltage.
- To determine the ECP5/ECP5-5G peak start-up current, use the Power Calculator tool in the Lattice Diamond Design Software.

# 3.13. sysI/O Single-Ended DC Electrical Characteristics

**Table 3.12. Single-Ended DC Characteristics**

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min (V) | Max (V) | Min (V) | Max (V) | | | | |
| LVCMOS33 | –0.3 | 0.8 | 2.0 | 3.465 | 0.4 | $V_{CCIO}$ – 0.4 | 16, 12, 8, 4 | –16, –12, –8, –4 |
| LVCMOS25 | –0.3 | 0.7 | 1.7 | 3.465 | 0.4 | $V_{CCIO}$ – 0.4 | 12, 8, 4 | –12, –8, –4 |
| LVCMOS18 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.465 | 0.4 | $V_{CCIO}$ – 0.4 | 12, 8, 4 | –12, –8, –4 |
| LVCMOS15 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.465 | 0.4 | $V_{CCIO}$ – 0.4 | 8, 4 | –8, –4 |
| LVCMOS12 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.465 | 0.4 | $V_{CCIO}$ – 0.4 | 8, 4 | –8, –4 |
| LVTTL33 | –0.3 | 0.8 | 2.0 | 3.465 | 0.4 | $V_{CCIO}$ – 0.4 | 16, 12, 8, 4 | –16, –12, –8, –4 |
| SSTL18_I (DDR2 Memory) | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 3.465 | 0.4 | $V_{CCIO}$ – 0.4 | 6.7 | –6.7 |
| SSTL18_II | –0.3 | $V_{REF}$ – | $V_{REF}$ + 0.125 | 3.465 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL15 _I (DDR3 Memory) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.465 | 0.31 | $V_{CCIO}$ – 0.31 | 7.5 | –7.5 |
| SSTL15_II (DDR3 Memory) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.465 | 0.31 | $V_{CCIO}$ – 0.31 | 8.8 | –8.8 |
| SSTL135_I (DDR3L Memory) | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 3.465 | 0.27 | $V_{CCIO}$ – 0.27 | 7 | –7 |
| SSTL135_II (DDR3L Memory) | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 3.465 | 0.27 | $V_{CCIO}$ – 0.27 | 8 | –8 |
| MIPI D-PHY (LP)[3] | –0.3 | 0.55 | 0.88 | 3.465 | — | — | — | — |
| HSUL12 (LPDDR2/3 Memory) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.465 | 0.3 | $V_{CCIO}$ – 0.3 | 4 | –4 |

**Notes**:

1. For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O (All I/Os used in the same $V_{CCIO}$).
2. Not all IO types are supported in all banks. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
3. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on $V_{IH}$ and $V_{IL}$. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet $V_{IH}$/$V_{IL}$ spec on LVCOM12.

# 3.14. sysI/O Differential Electrical Characteristics

## 3.14.1. LVDS

Over recommended operating conditions.

**Table 3.13. LVDS**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | — | 0 | — | 2.4 | V |
| $V_{CM}$ | Input Common Mode Voltage | Half the sum of the two Inputs | 0.05 | — | 2.35 | V |
| $V_{THD}$ | Differential Input Threshold | Difference between the two Inputs | ±100 | — | — | mV |
| $I_{IN}$ | Input Current | Power On or Power Off | — | — | ±10 | µA |
| $V_{OH}$ | Output High Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ω | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output Low Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ω | 0.9 V | 1.03 | — | V |
| $V_{OD}$ | Output Voltage Differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ω | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Between High and Low | — | — | — | 50 | mV |
| $V_{OS}$ | Output Voltage Offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100 Ω | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between H and L | — | — | — | 50 | mV |
| $I_{SAB}$ | Output Short Circuit Current | $V_{OD}$ = 0 V Driver outputs shorted to each other | — | — | 12 | mA |

**Note**: On the left and right sides of the device, this specification is valid only for $V_{CCIO}$ = 2.5 V or 3.3 V.

## 3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

## 3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V $V_{CCIO}$. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

### 3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

**Table 3.18. Input to SLVS**

| Parameter | ECP5/ECP5-5G LVDS Input | SLVS Output | Unit |
|---|---|---|---|
| Vcm (min) | 50 | 150 | mV |
| Vcm (max) | 2350 | 250 | mV |
| Differential Voltage (min) | 100 | 140 | mV |
| Differential Voltage (max) | — | 270 | mV |

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.

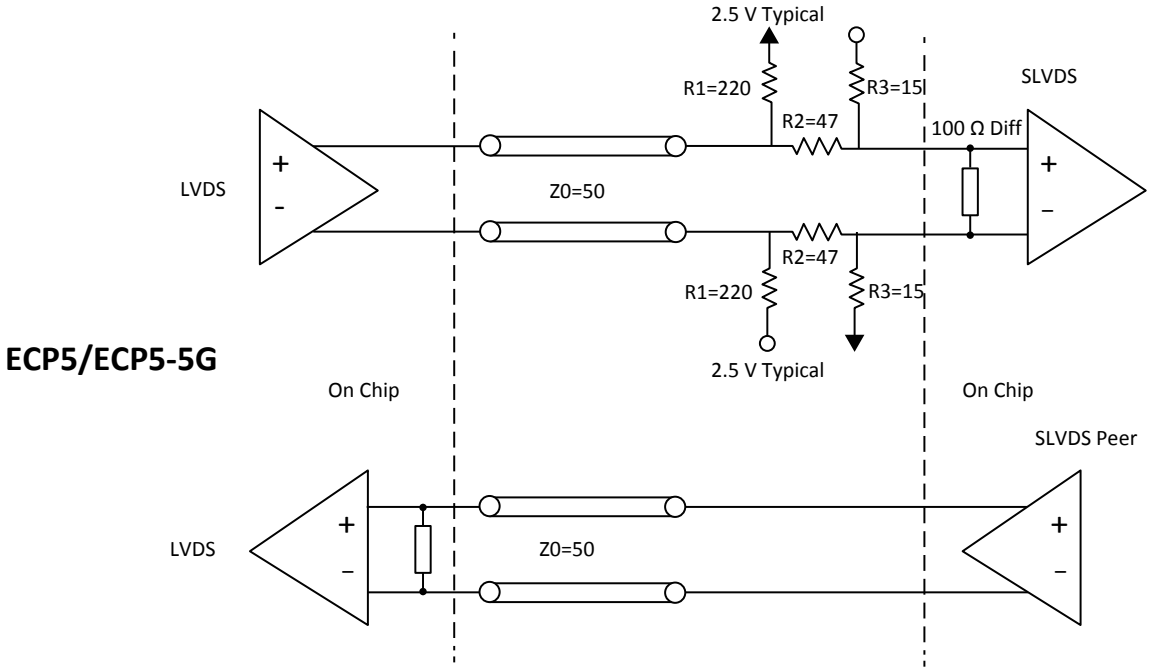
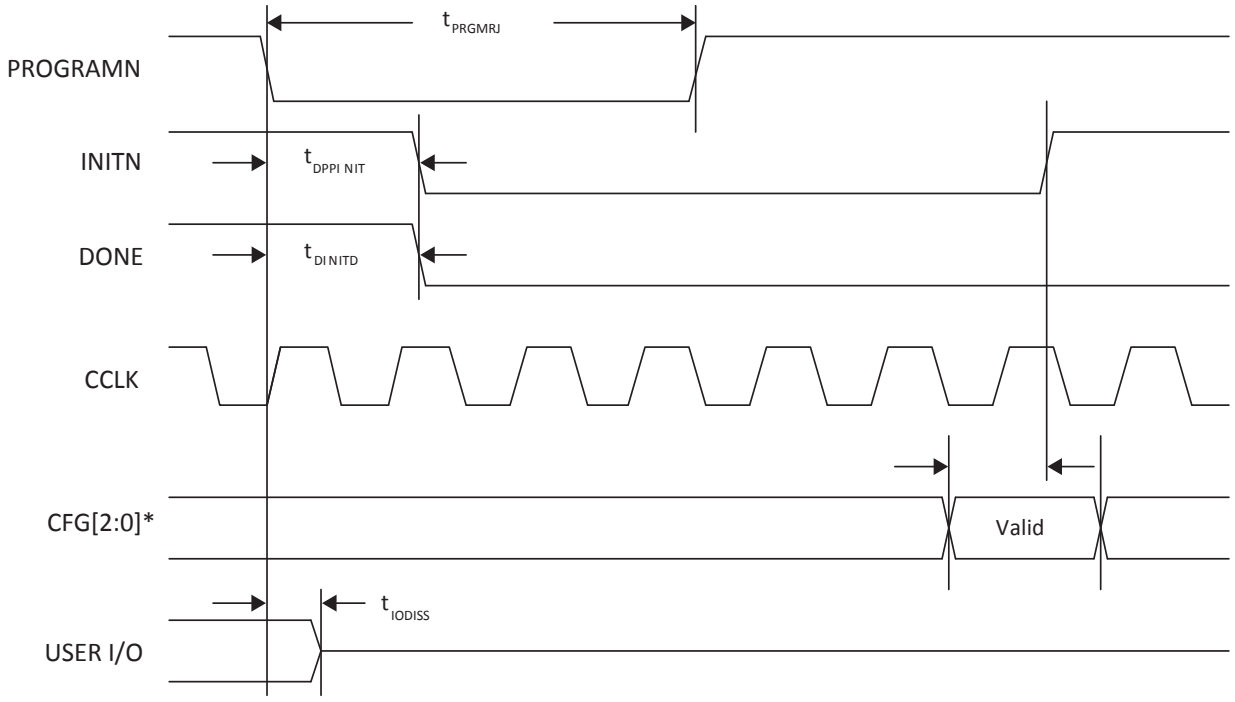



**Figure 3.5. SLVS Interface**

**Table 3.22. ECP5/ECP5-5G External Switching Characteristics** *(Continued)*

| Parameter | Description | Device | –8 | | –7 | | –6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Data Input Delay | All Devices | 0 | — | 0 | — | 0 | — | ns |
| **Generic DDR Input** | | | | | | | | | |
| **Generic DDRX1 Inputs With Clock and Data Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6** | | | | | | | | | |
| $t_{SU\_GDDRX1\_centered}$ | Data Setup Before CLK Input | All Devices | 0.52 | — | 0.52 | — | 0.52 | — | ns |
| $t_{HD\_GDDRX1\_centered}$ | Data Hold After CLK Input | All Devices | 0.52 | — | 0.52 | — | 0.52 | — | ns |
| $f_{DATA\_GDDRX1\_centered}$ | GDDRX1 Data Rate | All Devices | — | 500 | — | 500 | — | 500 | Mb/s |
| $f_{MAX\_GDDRX1\_centered}$ | GDDRX1 CLK Frequency (SCLK) | All Devices | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Inputs With Clock and Data Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.7** | | | | | | | | | |
| $t_{SU\_GDDRX1\_aligned}$ | Data Setup from CLK Input | All Devices | — | –0.55 | — | –0.55 | — | –0.55 | ns + 1/2 UI |
| $t_{HD\_GDDRX1\_aligned}$ | Data Hold from CLK Input | All Devices | 0.55 | — | 0.55 | — | 0.55 | — | ns + 1/2 UI |
| $f_{DATA\_GDDRX1\_aligned}$ | GDDRX1 Data Rate | All Devices | — | 500 | — | 500 | — | 500 | Mb/s |
| $f_{MAX\_GDDRX1\_aligned}$ | GDDRX1 CLK Frequency (SCLK) | All Devices | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX2 Inputs With Clock and Data Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.6** | | | | | | | | | |
| $t_{SU\_GDDRX2\_centered}$ | Data Setup before CLK Input | All Devices | 0.321 | — | 0.403 | — | 0.471 | — | ns |
| $t_{HD\_GDDRX2\_centered}$ | Data Hold after CLK Input | All Devices | 0.321 | — | 0.403 | — | 0.471 | — | ns |
| $f_{DATA\_GDDRX2\_centered}$ | GDDRX2 Data Rate | All Devices | — | 800 | — | 700 | — | 624 | Mb/s |
| $f_{MAX\_GDDRX2\_centered}$ | GDDRX2 CLK Frequency (ECLK) | All Devices | — | 400 | — | 350 | — | 312 | MHz |
| **Generic DDRX2 Inputs With Clock and Data Aligned at Pin (GDDRX2_RX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.7** | | | | | | | | | |
| $t_{SU\_GDDRX2\_aligned}$ | Data Setup from CLK Input | All Devices | — | –0.344 | — | –0.42 | — | -0.495 | ns + 1/2 UI |
| $t_{HD\_GDDRX2\_aligned}$ | Data Hold from CLK Input | All Devices | 0.344 | — | 0.42 | — | 0.495 | — | ns + 1/2 UI |
| $f_{DATA\_GDDRX2\_aligned}$ | GDDRX2 Data Rate | All Devices | — | 800 | — | 700 | — | 624 | Mb/s |
| $f_{MAX\_GDDRX2\_aligned}$ | GDDRX2 CLK Frequency | All Devices | — | 400 | — | 350 | — | 312 | MHz |
| **Video DDRX71 Inputs With Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) Using PLL Clock Input, Left and Right sides Only Figure 3.11** | | | | | | | | | |
| $t_{SU\_LVDS71\_i}$ | Data Setup from CLK Input (bit i) | All Devices | — | –0.271 | — | –0.39 | — | –0.41 | ns+(1/2+i) * UI |
| $t_{HD\_LVDS71\_i}$ | Data Hold from CLK Input (bit i) | All Devices | 0.271 | — | 0.39 | — | 0.41 | — | ns+(1/2+i) * UI |
| $f_{DATA\_LVDS71}$ | DDR71 Data Rate | All Devices | — | 756 | — | 620 | — | 525 | Mb/s |
| $f_{MAX\_LVDS71}$ | DDR71 CLK Frequency (ECLK) | All Devices | — | 378 | — | 310 | — | 262.5 | MHz |




*The CFG pins are normally static (hardwired).

**Figure 3.20. Configuration from PROGRAMN Timing**

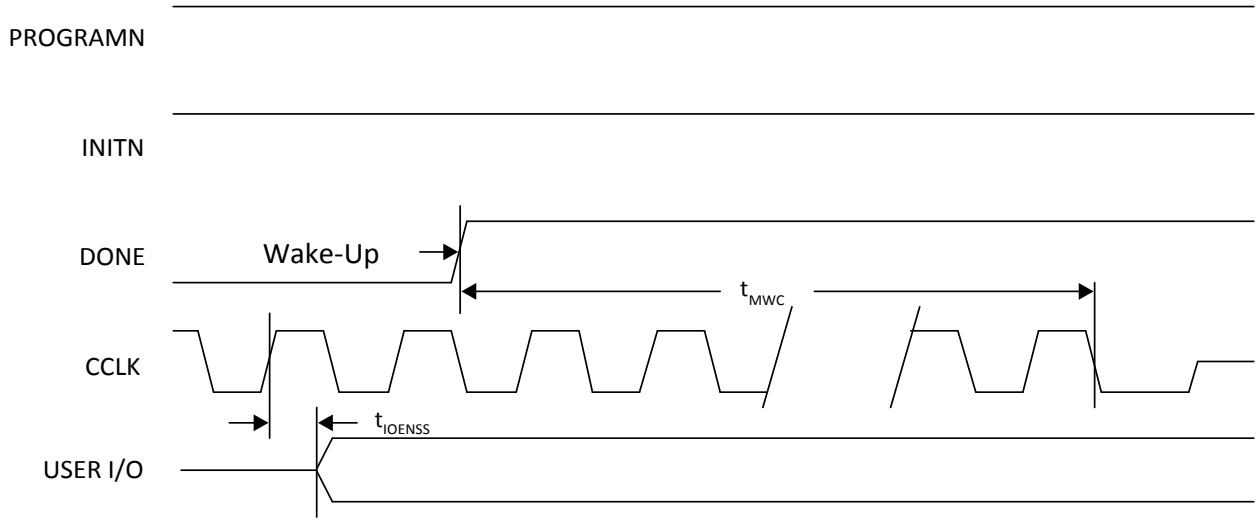



**Figure 3.21. Wake-Up Timing**

| Part number | Grade | Package | Pins | Temp. | LUTs (K) | SERDES |
|---|---|---|---|---|---|---|
| LFE5U-45F-8BG554C | –8 | Lead free caBGA | 554 | Commercial | 44 | No |
| LFE5U-85F-6MG285C | –6 | Lead free csfBGA | 285 | Commercial | 84 | No |
| LFE5U-85F-7MG285C | –7 | Lead free csfBGA | 285 | Commercial | 84 | No |
| LFE5U-85F-8MG285C | –8 | Lead free csfBGA | 285 | Commercial | 84 | No |
| LFE5U-85F-6BG381C | –6 | Lead free caBGA | 381 | Commercial | 84 | No |
| LFE5U-85F-7BG381C | –7 | Lead free caBGA | 381 | Commercial | 84 | No |
| LFE5U-85F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 84 | No |
| LFE5U-85F-6BG554C | –6 | Lead free caBGA | 554 | Commercial | 84 | No |
| LFE5U-85F-7BG554C | –7 | Lead free caBGA | 554 | Commercial | 84 | No |
| LFE5U-85F-8BG554C | –8 | Lead free caBGA | 554 | Commercial | 84 | No |
| LFE5U-85F-6BG756C | –6 | Lead free caBGA | 756 | Commercial | 84 | No |
| LFE5U-85F-7BG756C | –7 | Lead free caBGA | 756 | Commercial | 84 | No |
| LFE5U-85F-8BG756C | –8 | Lead free caBGA | 756 | Commercial | 84 | No |
| LFE5UM-25F-6MG285C | –6 | Lead free csfBGA | 285 | Commercial | 24 | Yes |
| LFE5UM-25F-7MG285C | –7 | Lead free csfBGA | 285 | Commercial | 24 | Yes |
| LFE5UM-25F-8MG285C | –8 | Lead free csfBGA | 285 | Commercial | 24 | Yes |
| LFE5UM-25F-6BG381C | –6 | Lead free caBGA | 381 | Commercial | 24 | Yes |
| LFE5UM-25F-7BG381C | –7 | Lead free caBGA | 381 | Commercial | 24 | Yes |
| LFE5UM-25F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 24 | Yes |
| LFE5UM-45F-6MG285C | –6 | Lead free csfBGA | 285 | Commercial | 44 | Yes |
| LFE5UM-45F-7MG285C | –7 | Lead free csfBGA | 285 | Commercial | 44 | Yes |
| LFE5UM-45F-8MG285C | –8 | Lead free csfBGA | 285 | Commercial | 44 | Yes |
| LFE5UM-45F-6BG381C | –6 | Lead free caBGA | 381 | Commercial | 44 | Yes |
| LFE5UM-45F-7BG381C | –7 | Lead free caBGA | 381 | Commercial | 44 | Yes |
| LFE5UM-45F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 44 | Yes |
| LFE5UM-45F-6BG554C | –6 | Lead free caBGA | 554 | Commercial | 44 | Yes |
| LFE5UM-45F-7BG554C | –7 | Lead free caBGA | 554 | Commercial | 44 | Yes |
| LFE5UM-45F-8BG554C | –8 | Lead free caBGA | 554 | Commercial | 44 | Yes |
| LFE5UM-85F-6MG285C | –6 | Lead free csfBGA | 285 | Commercial | 84 | Yes |
| LFE5UM-85F-7MG285C | –7 | Lead free csfBGA | 285 | Commercial | 84 | Yes |
| LFE5UM-85F-8MG285C | –8 | Lead free csfBGA | 285 | Commercial | 84 | Yes |
| LFE5UM-85F-6BG381C | –6 | Lead free caBGA | 381 | Commercial | 84 | Yes |
| LFE5UM-85F-7BG381C | –7 | Lead free caBGA | 381 | Commercial | 84 | Yes |
| LFE5UM-85F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 84 | Yes |
| LFE5UM-85F-6BG554C | –6 | Lead free caBGA | 554 | Commercial | 84 | Yes |
| LFE5UM-85F-7BG554C | –7 | Lead free caBGA | 554 | Commercial | 84 | Yes |
| LFE5UM-85F-8BG554C | –8 | Lead free caBGA | 554 | Commercial | 84 | Yes |
| LFE5UM-85F-6BG756C | –6 | Lead free caBGA | 756 | Commercial | 84 | Yes |
| LFE5UM-85F-7BG756C | –7 | Lead free caBGA | 756 | Commercial | 84 | Yes |
| LFE5UM-85F-8BG756C | –8 | Lead free caBGA | 756 | Commercial | 84 | Yes |
| LFE5UM5G-25F-8MG285C | –8 | Lead free csfBGA | 285 | Commercial | 24 | Yes |
| LFE5UM5G-25F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 24 | Yes |
| LFE5UM5G-45F-8MG285C | –8 | Lead free csfBGA | 285 | Commercial | 44 | Yes |
| LFE5UM5G-45F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 44 | Yes |
| LFE5UM5G-45F-8BG554C | –8 | Lead free caBGA | 554 | Commercial | 44 | Yes |
| LFE5UM5G-85F-8MG285C | –8 | Lead free csfBGA | 285 | Commercial | 84 | Yes |

| Part number | Grade | Package | Pins | Temp. | LUTs (K) | SERDES |
|---|---|---|---|---|---|---|
| LFE5UM5G-85F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 84 | Yes |
| LFE5UM5G-85F-8BG554C | –8 | Lead free caBGA | 554 | Commercial | 84 | Yes |
| LFE5UM5G-85F-8BG756C | –8 | Lead free caBGA | 756 | Commercial | 84 | Yes |

### 5.2.2. Industrial

| Part number | Grade | Package | Pins | Temp. | LUTs (K) | SERDES |
|---|---|---|---|---|---|---|
| LFE5U-12F-6BG256I | –6 | Lead free caBGA | 256 | Industrial | 12 | No |
| LFE5U-12F-7BG256I | –7 | Lead free caBGA | 256 | Industrial | 12 | No |
| LFE5U-12F-8BG256I | –8 | Lead free caBGA | 256 | Industrial | 12 | No |
| LFE5U-12F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 12 | No |
| LFE5U-12F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 12 | No |
| LFE5U-12F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 12 | No |
| LFE5U-12F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 12 | No |
| LFE5U-12F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 12 | No |
| LFE5U-12F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 12 | No |
| LFE5U-25F-6BG256I | –6 | Lead free caBGA | 256 | Industrial | 24 | No |
| LFE5U-25F-7BG256I | –7 | Lead free caBGA | 256 | Industrial | 24 | No |
| LFE5U-25F-8BG256I | –8 | Lead free caBGA | 256 | Industrial | 24 | No |
| LFE5U-25F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 24 | No |
| LFE5U-25F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 24 | No |
| LFE5U-25F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 24 | No |
| LFE5U-25F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 24 | No |
| LFE5U-25F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 24 | No |
| LFE5U-25F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 24 | No |
| LFE5U-45F-6BG256I | –6 | Lead free caBGA | 256 | Industrial | 44 | No |
| LFE5U-45F-7BG256I | –7 | Lead free caBGA | 256 | Industrial | 44 | No |
| LFE5U-45F-8BG256I | –8 | Lead free caBGA | 256 | Industrial | 44 | No |
| LFE5U-45F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 44 | No |
| LFE5U-45F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 44 | No |
| LFE5U-45F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 44 | No |
| LFE5U-45F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 44 | No |
| LFE5U-45F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 44 | No |
| LFE5U-45F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 44 | No |
| LFE5U-45F-6BG554I | –6 | Lead free caBGA | 554 | Industrial | 44 | No |
| LFE5U-45F-7BG554I | –7 | Lead free caBGA | 554 | Industrial | 44 | No |
| LFE5U-45F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 44 | No |
| LFE5U-85F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 84 | No |
| LFE5U-85F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 84 | No |
| LFE5U-85F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 84 | No |
| LFE5U-85F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 84 | No |
| LFE5U-85F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 84 | No |
| LFE5U-85F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 84 | No |
| LFE5U-85F-6BG554I | –6 | Lead free caBGA | 554 | Industrial | 84 | No |
| LFE5U-85F-7BG554I | –7 | Lead free caBGA | 554 | Industrial | 84 | No |
| LFE5U-85F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 84 | No |