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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	245
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-7bg554i

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- Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
 - DDR registers in I/O cells
 - Dedicated read/write levelling functionality
 - Dedicated gearing logic
 - Source synchronous standards support
 - ADC/DAC, 7:1 LVDS, XGMII
 - High Speed ADC/DAC devices
 - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
 - On-chip termination
 - LVTTTL and LVCMOS 33/25/18/15/12
 - SSTL 18/15 I, II
 - HSUL12
 - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
 - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
 - Shared bank for configuration I/Os
 - SPI boot flash interface
 - Dual-boot images supported
 - Slave SPI
 - TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
 - Soft Error Detect – Embedded hard macro
 - Soft Error Correction – Without stopping user operation
 - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
 - IEEE 1149.1 and IEEE 1532 compliant
 - Reveal Logic Analyzer
 - On-chip oscillator for initialization and general use
 - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U- 12	LFE5U- 25	LFE5U- 45	LFE5U- 85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels / IO Count)							
256 caBGA (14 x 14 mm ² , 0.8 mm)	—	—	—	0/197	0/197	0/197	—
285 csfBGA (10 x 10 mm ² , 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm ² , 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm ² , 0.8 mm)	—	4/245	4/259	—	—	0/245	0/259
756 caBGA (27 x 27 mm ² , 0.8 mm)	—	—	4/365	—	—	—	0/365

2.7. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

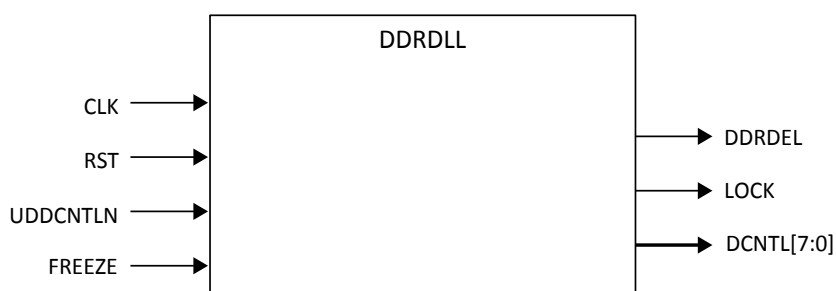


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

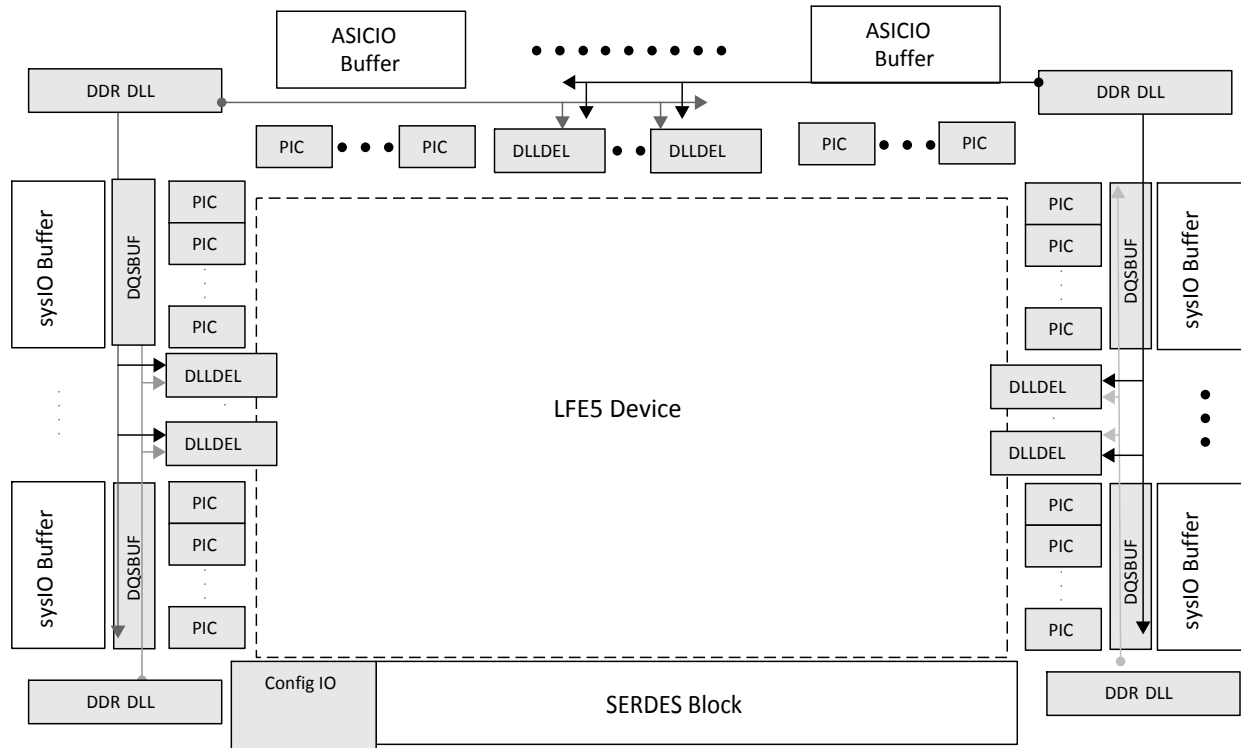


Figure 2.11. ECP5/ECP5-5G DLL Top Level View (For LFE-45 and LFE-85)

2.8. sysMEM Memory

ECP5/ECP5-5G devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

2.8.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in [Table 2.6](#) on page 25. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#).

In [Figure 2.15](#), note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

[Table 2.7](#) shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note:** One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in [DDR Memory Support](#) section on page 35.

Table 2.8. Input Block Port Description

Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers. ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in [Figure 2.19](#). The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

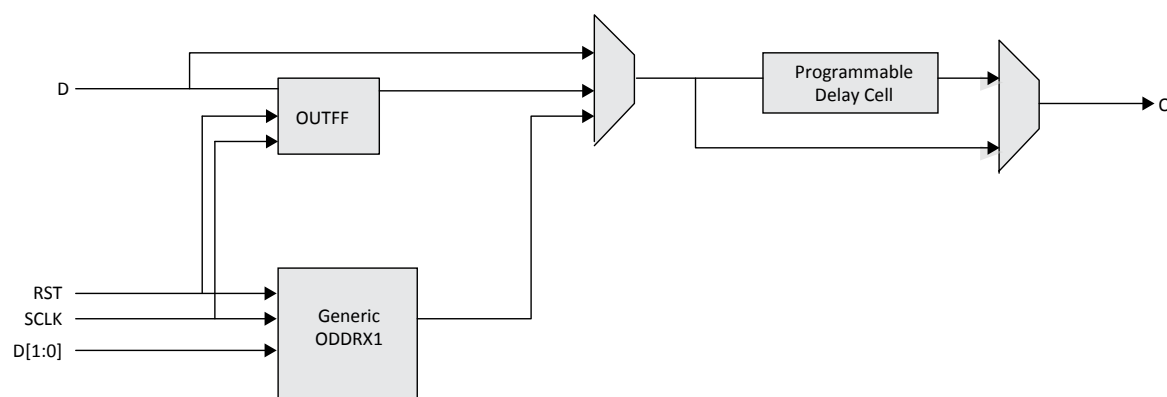


Figure 2.19. Output Register Block on Top Side

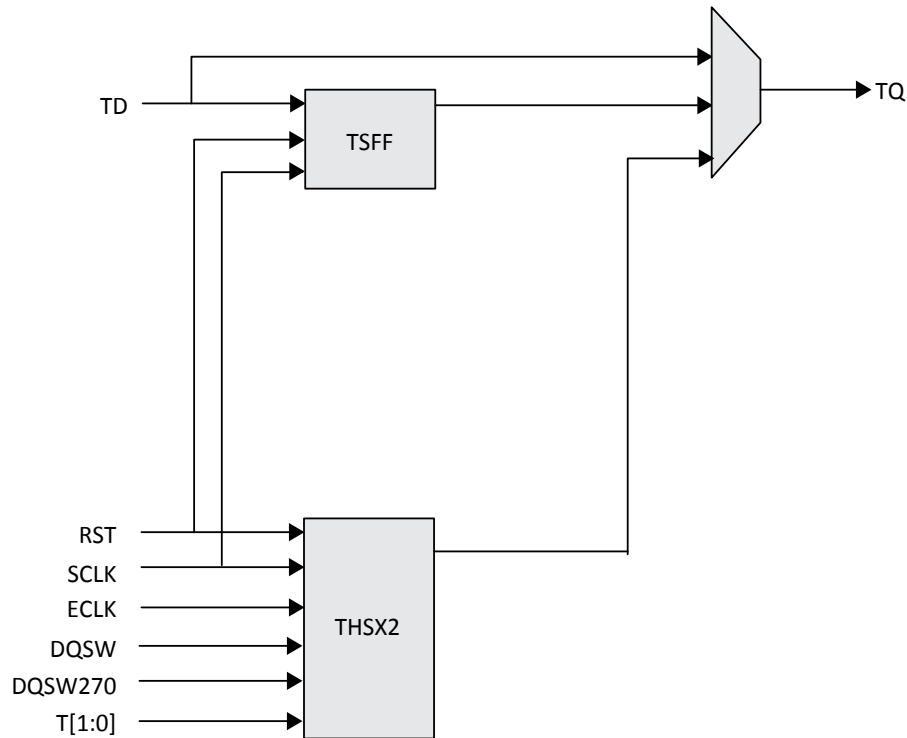


Figure 2.22. Tristate Register Block on Left and Right Sides

Table 2.10. Tristate Block Port Description

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR Register
RST	Input	Reset to the Tristate Block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.13. DDR Memory Support

2.13.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in [Figure 2.23](#) on page 36. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as "virtual" VCCIO, by driving these pins to HIGH, with the user connecting these pins to VCCIO power supply. These connections create "soft" connections to VCCIO thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

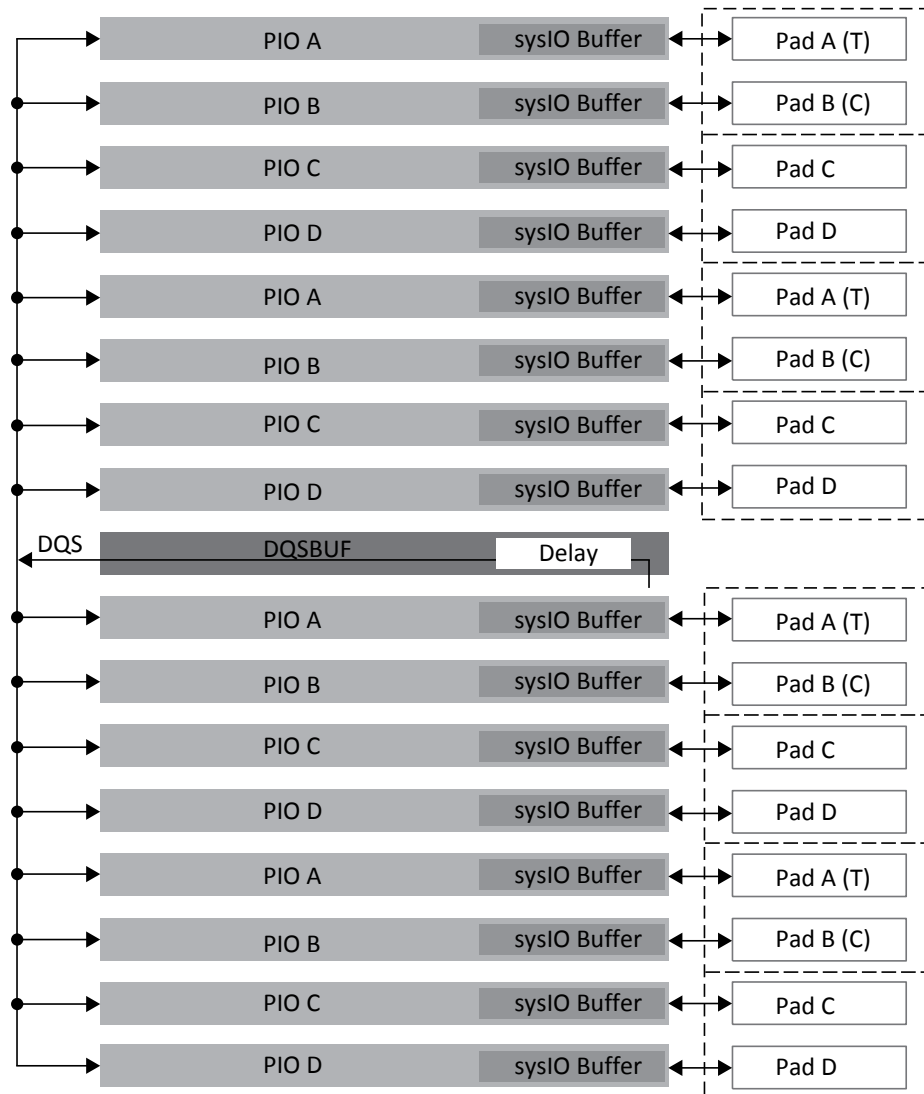


Figure 2.23. DQS Grouping on the Left and Right Edges

2.13.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR2/3, LPDDR2/3), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifted is achieved by using DQSDEL programmable delay line in the DQS Delay Block (DQS read circuit). The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block shown in [Figure 2.24](#) generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. [Table 2.15](#) lists the allowable combination of primary and secondary protocol combinations.

2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

[Table 2.15](#) lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#).

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to [LatticeECP3, ECP5 and ECP5-5G Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide \(TN1184\)](#).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. [Table 2.16](#) lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#) and [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.11. SERDES Power Supply Requirements^{1,2,3}

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I _{CCA-SB}	V _{CCA} Power Supply Current (Per Channel)	4	9.5	mA
I _{CCHRX-SB} ⁴	V _{CCHRX} , Input Buffer Current (Per Channel)	—	0.1	mA
I _{CCHTX-SB}	V _{CCHTX} , Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 3.125 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	43	54	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	40	50	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	34	43	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	28	38	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For I_{CCHRX-SB}, during Standby, input termination on Rx are disabled.
5. For I_{CCHRX-OP}, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics (Continued)

Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
Generic DDR Input									
Generic DDRX1 Inputs With Clock and Data Centered at Pin (GDDR1_RX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{SU_GDDR1_centered}$	Data Setup Before CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$t_{HD_GDDR1_centered}$	Data Hold After CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$f_{DATA_GDDR1_centered}$	GDDR1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX_GDDR1_centered}$	GDDR1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs With Clock and Data Aligned at Pin (GDDR1_RX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.7									
$t_{SU_GDDR1_aligned}$	Data Setup from CLK Input	All Devices	—	–0.55	—	–0.55	—	–0.55	ns + 1/2 UI
$t_{HD_GDDR1_aligned}$	Data Hold from CLK Input	All Devices	0.55	—	0.55	—	0.55	—	ns + 1/2 UI
$f_{DATA_GDDR1_aligned}$	GDDR1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX_GDDR1_aligned}$	GDDR1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Inputs With Clock and Data Centered at Pin (GDDR2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.6									
$t_{SU_GDDR2_centered}$	Data Setup before CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$t_{HD_GDDR2_centered}$	Data Hold after CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$f_{DATA_GDDR2_centered}$	GDDR2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX_GDDR2_centered}$	GDDR2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Inputs With Clock and Data Aligned at Pin (GDDR2_RX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.7									
$t_{SU_GDDR2_aligned}$	Data Setup from CLK Input	All Devices	—	–0.344	—	–0.42	—	–0.495	ns + 1/2 UI
$t_{HD_GDDR2_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	—	0.495	—	ns + 1/2 UI
$f_{DATA_GDDR2_aligned}$	GDDR2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX_GDDR2_aligned}$	GDDR2 CLK Frequency	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Inputs With Clock and Data Aligned at Pin (GDDR71_RX.ECLK) Using PLL Clock Input, Left and Right sides Only Figure 3.11									
$t_{SU_LVDS71_i}$	Data Setup from CLK Input (bit i)	All Devices	—	–0.271	—	–0.39	—	–0.41	ns+(1/2+i) * UI
$t_{HD_LVDS71_i}$	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	—	0.41	—	ns+(1/2+i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	$V_{CCA} + 0.5^2$	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode) ²	0.1	—	$V_{CCA} + 0.2$	V
$T_{RX-RELOCK}$	SCDR re-lock time ¹	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss (without package)	—	—	–10	dB

Notes:

1. This is the typical number of bit times to re-lock to a new phase or frequency within ± 300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Notes:

1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

3.24. SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3.29 specifies reference clock requirements, over the full range of operating conditions.

Table 3.29. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min	Typ	Max	Unit
F_{REF}	Frequency range	50	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance ¹	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock ^{2,4}	200	—	V_{CCAUXA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2 \cdot V_{CCAUXA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	$V_{CCAUXA} + 0.4$	V
D_{REF}	Duty cycle ³	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–30%	100/HiZ	+30%	Ω
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

Notes:

- Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).
- The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
- Measured at 50% amplitude.
- Single-ended clocking is achieved by applying a reference voltage V_{REF} on REFCLKN input, with the clock applied to REFCLKP input pin. V_{REF} should be set to mid-point of the REFCLKP voltage swing.

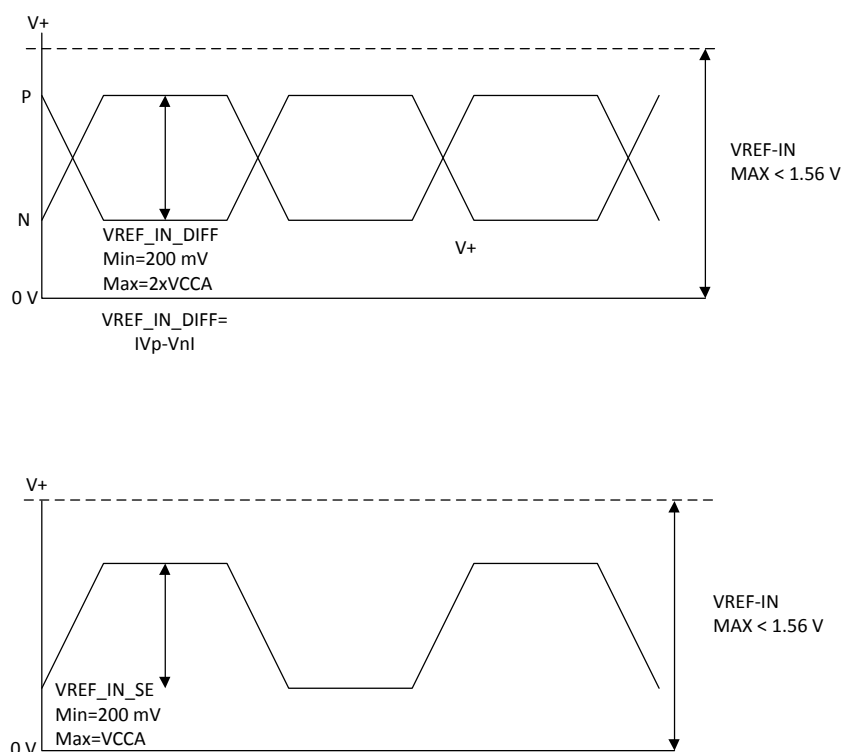
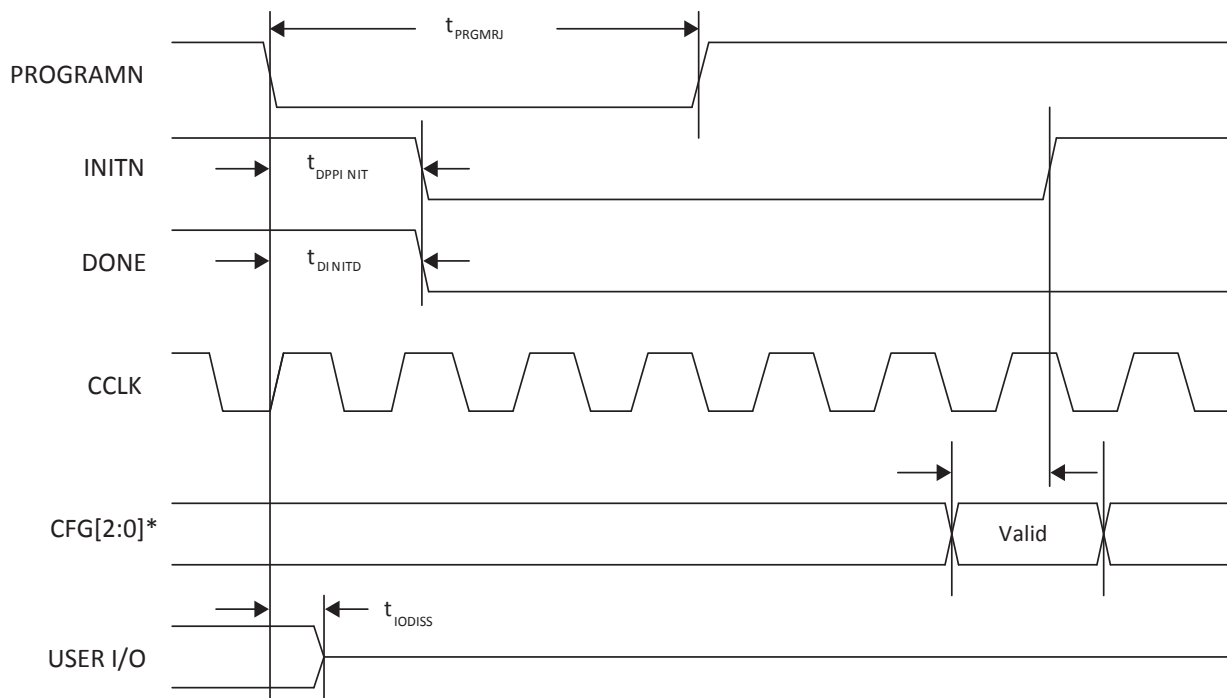


Figure 3.14. SERDES External Reference Clock Waveforms



*The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

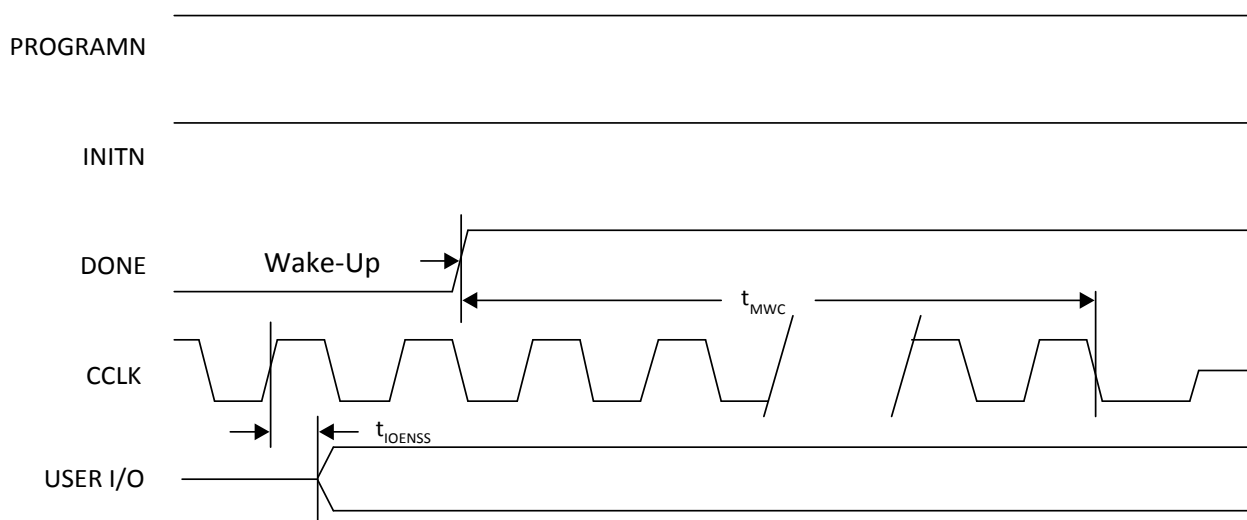


Figure 3.21. Wake-Up Timing

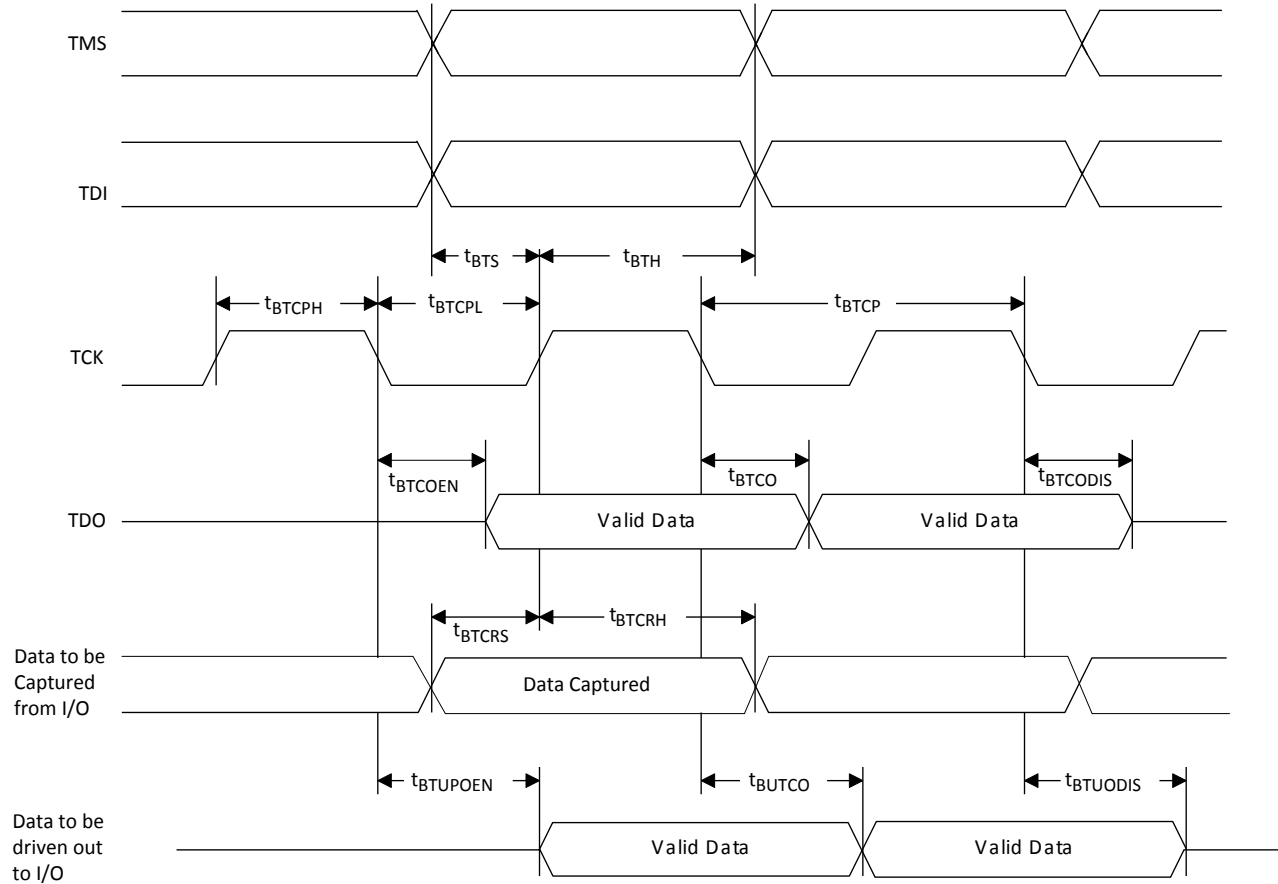
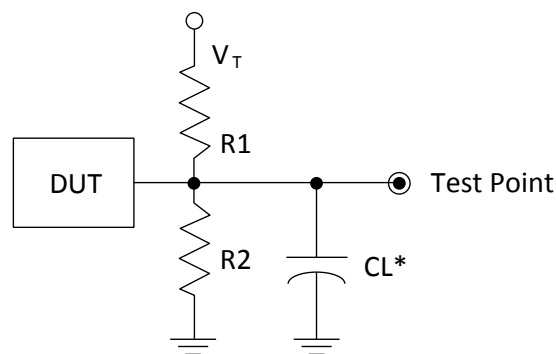


Figure 3.23. JTAG Port Timing Waveforms

3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.



*CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTTL and LVCMOS Standards

4. Pinout Information

4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[L/R] [Group Number]_[A/B/C/D]	I/O	[L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIO A and B are grouped as a pair, and PIO C and D are group as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer. Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω.
P[T/B][Group Number]_[A/B]	I/O	[T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer. PIO A/B forms a pair of emulated differential output buffer.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins. V _{CC} = 1.1 V (ECP5), 1.2 V (ECP5UM5G)
V _{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. V _{CCAUX} = 2.5 V.
V _{CCIOx}	—	Dedicated power supply pins for I/O bank x. V _{CCIO8} is used for configuration and JTAG.
VREF1_x	—	Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as VREF1 input. When not used, they may be used as I/O pins.
PLL, DLL and Clock Functions		
[LOC]_[GPLL[T, C]]_IN	I	General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not configured as GPLL input pads, they can be used as general purpose I/O pins.
GR_PCLK[Bank][num]	I	General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to ECP5 sysClock PLL/DLL Design and Usage Guide (TN1263) . These pins are shared I/O pins. When not configured as GR pins, they can be used as general purpose I/O pins.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/O pins. When not configured as PCLK pins, they can be used as general purpose I/O pins.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section.
			- Deleted Serial RapidIO protocol under Embedded SERDES. - Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3.
			Mentioned transmit de-emphasis “pre- and post-cursors”.
		Architecture	Updated Overview section.
			- Revised description of PFU blocks. - Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section.
			- Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. - Deleted Serial RapidIO protocol. - Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section.
			- Deleted “130 MHz $\pm$15% CMOS” oscillator. - Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA} .
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15_I, SSTL15_II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to $t_{SKEW_PR} V_{CCA}$ and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclk).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.



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