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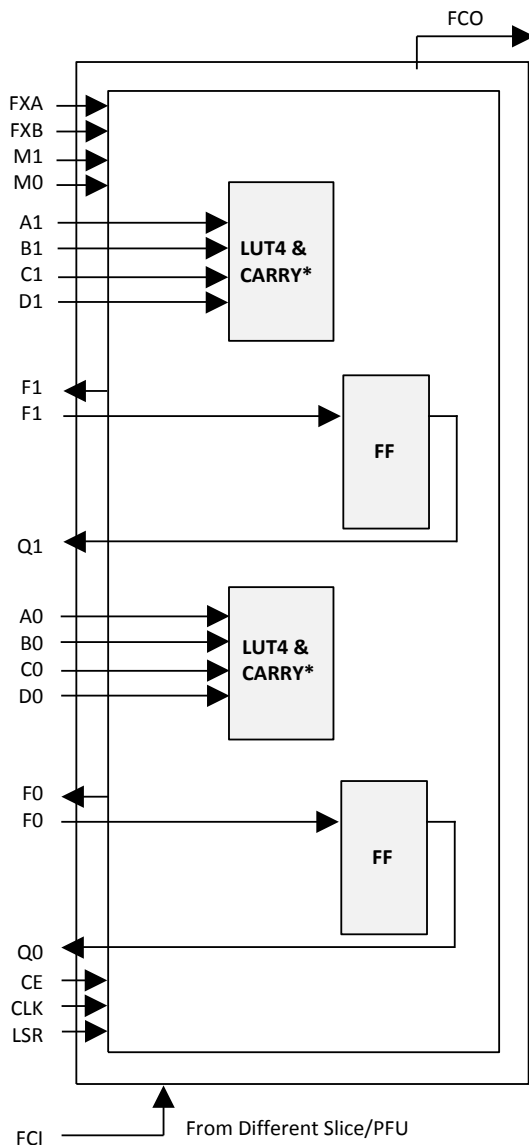
Details

Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-7mg285c

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Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

WCK is CLK

WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2

WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

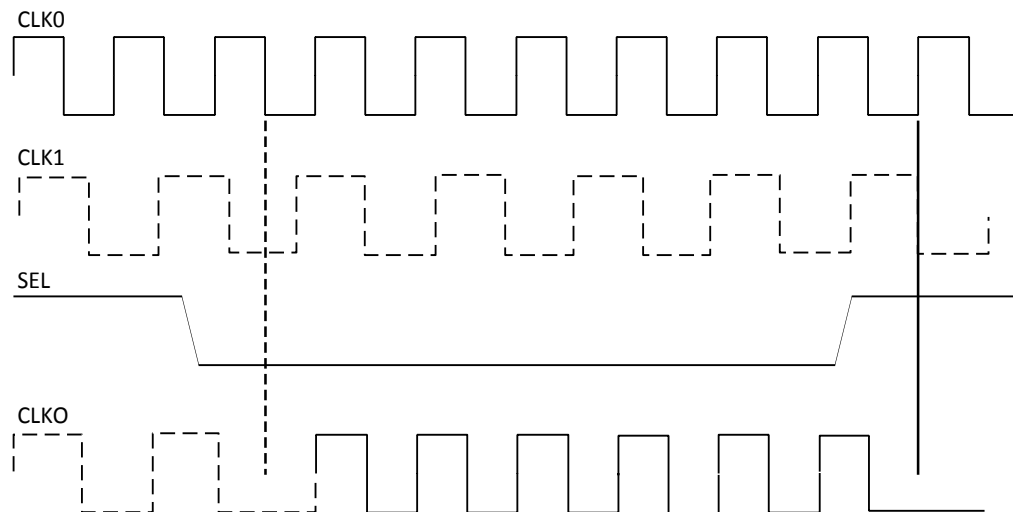


Figure 2.7. DCS Waveforms

2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90°)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

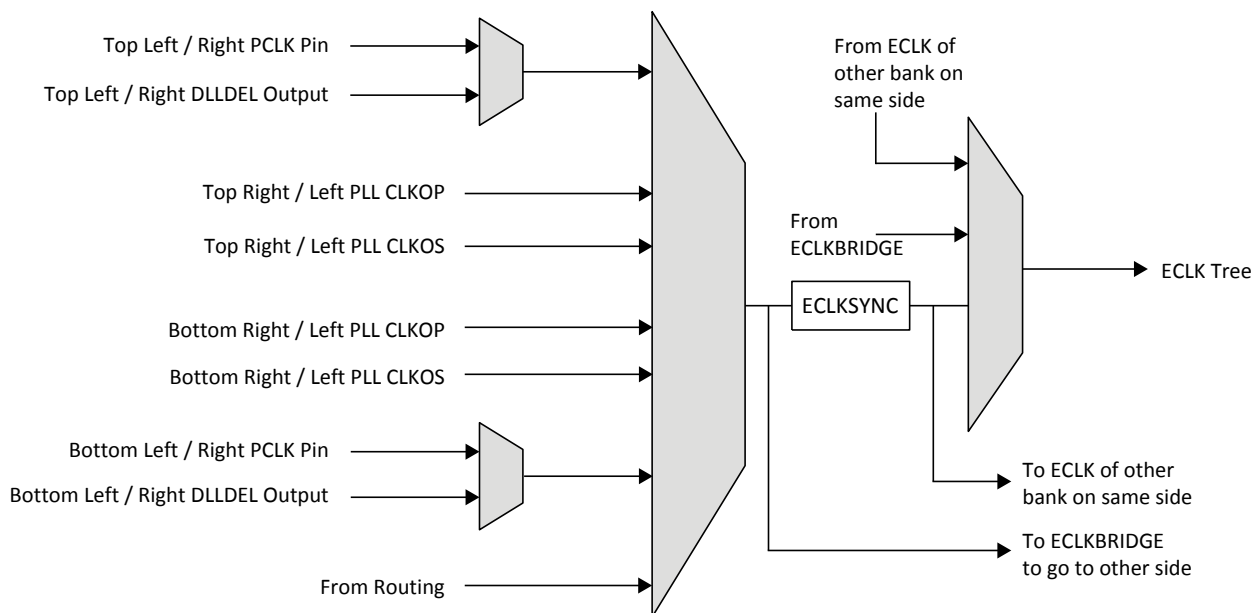


Figure 2.8. Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

2.6. Clock Dividers

ECP5/ECP5-5G devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a $\div 2$, $\div 3.5$ mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal.

The clock dividers can be fed from selected PLL outputs, external primary clock pins multiplexed with the DDRDEL Slave Delay or from routing. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The SLIP signal slips the outputs one cycle relative to the input clock. For further information on clock dividers, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#). Figure 2.9 shows the clock divider connections.

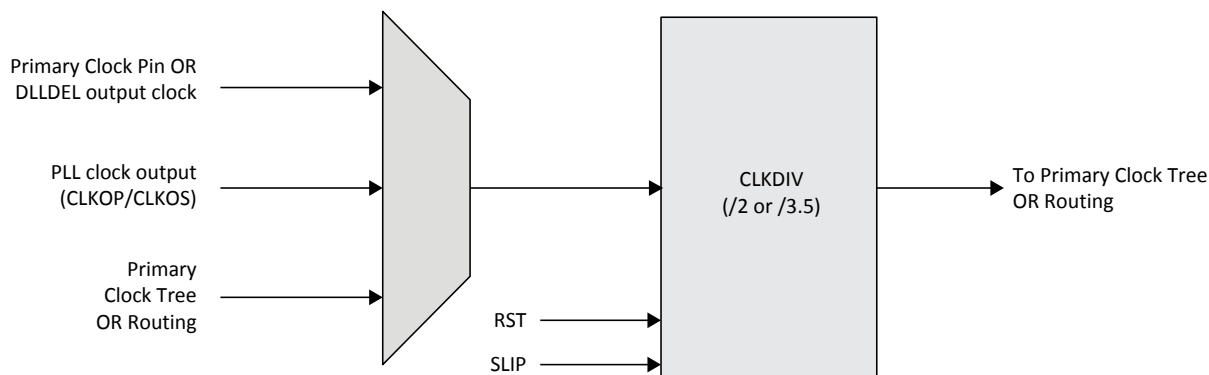


Figure 2.9. ECP5/ECP5-5G Clock Divider Sources

2.7. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

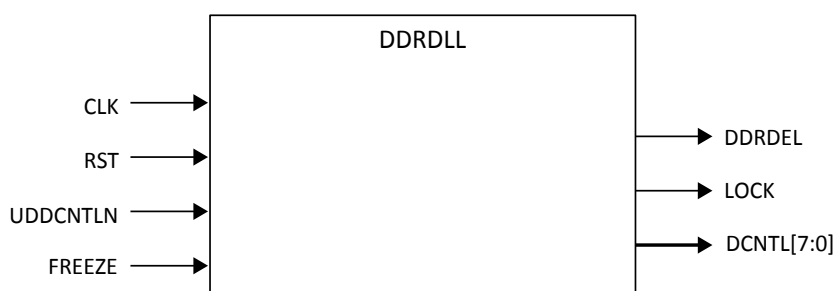


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

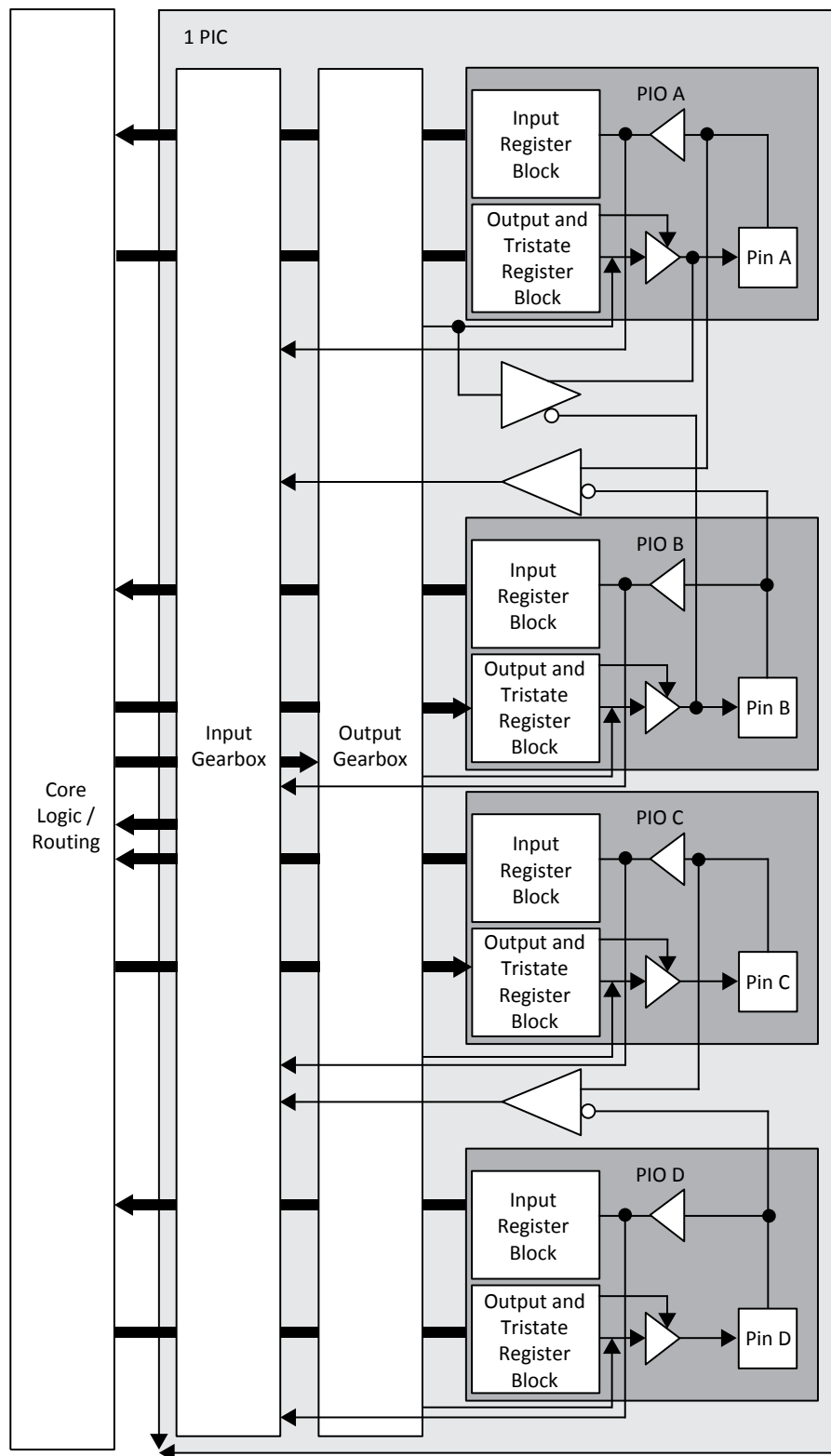
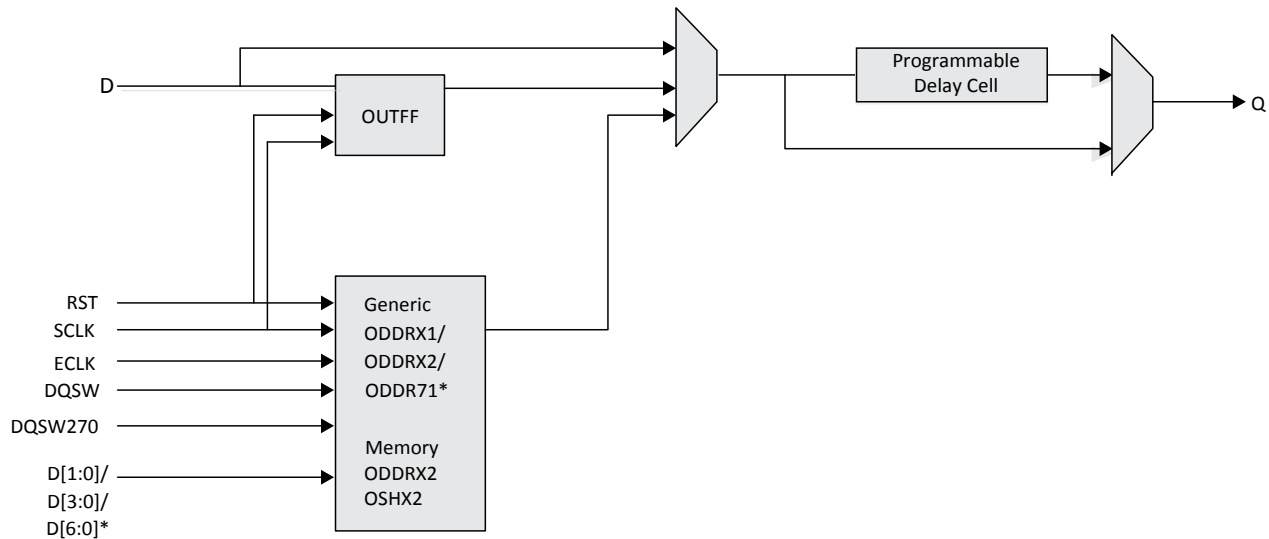


Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Sides



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

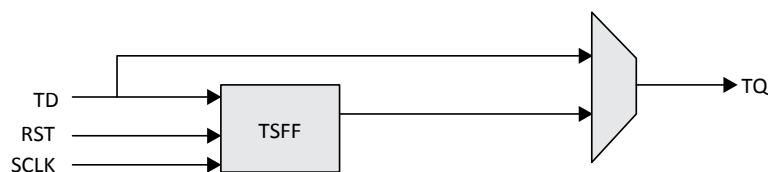


Figure 2.21. Tristate Register Block on Top Side

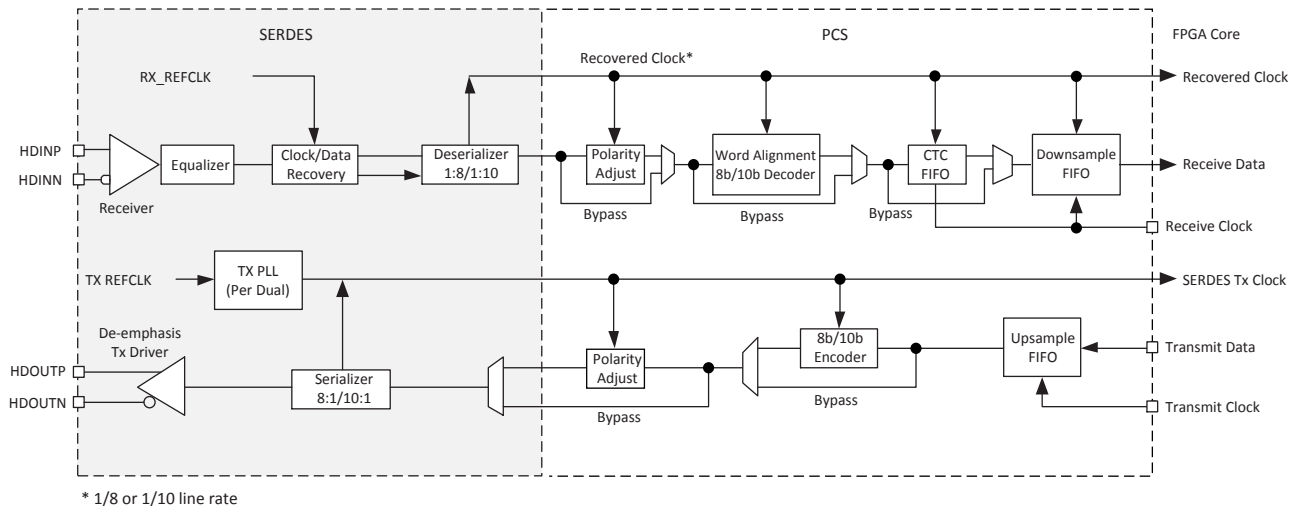
Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).


Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for more information.

2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) – Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to [Minimizing System Interruption During Configuration Using TransFR Technology \(TN1087\)](#) for details.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#).

2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

3.13. sysI/O Single-Ended DC Electrical Characteristics

Table 3.12. Single-Ended DC Characteristics

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max (V)	V _{OH} Min (V)	I _{OL} ¹ (mA)	I _{OH} ¹ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVC MOS33	−0.3	0.8	2.0	3.465	0.4	V _{CCIO} − 0.4	16, 12, 8, 4	−16, −12, −8, −4
LVC MOS25	−0.3	0.7	1.7	3.465	0.4	V _{CCIO} − 0.4	12, 8, 4	−12, −8, −4
LVC MOS18	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	12, 8, 4	−12, −8, −4
LVC MOS15	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	8, 4	−8, −4
LVC MOS12	−0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} − 0.4	8, 4	−8, −4
LVTTL33	−0.3	0.8	2.0	3.465	0.4	V _{CCIO} − 0.4	16, 12, 8, 4	−16, −12, −8, −4
SSTL18_I (DDR2 Memory)	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	3.465	0.4	V _{CCIO} − 0.4	6.7	−6.7
SSTL18_II	−0.3	V _{REF} −	V _{REF} + 0.125	3.465	0.28	V _{CCIO} − 0.28	13.4	−13.4
SSTL15_I (DDR3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} − 0.31	7.5	−7.5
SSTL15_II (DDR3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} − 0.31	8.8	−8.8
SSTL135_I (DDR3L Memory)	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} − 0.27	7	−7
SSTL135_II (DDR3L Memory)	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} − 0.27	8	−8
MIPI D-PHY (LP) ³	−0.3	0.55	0.88	3.465	—	—	—	—
HSUL12 (LPDDR2/3 Memory)	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	3.465	0.3	V _{CCIO} − 0.3	4	−4

Notes:

- For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O (All I/Os used in the same V_{CCIO}).
- Not all IO types are supported in all banks. Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for details.
- MIPI D-PHY LP input can be implemented by powering V_{CCIO} to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVC MOS12 with V_{CCIO} at 1.2V, which would meet V_{IH}/V_{IL} spec on LVC MOS12.

3.14. sysI/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.13. LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	±100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	±10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100\ \Omega$	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100\ \Omega$	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100\ \Omega$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100\ \Omega$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0\text{ V}$ Driver outputs shorted to each other	—	—	12	mA

Note: On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5\text{ V}$ or 3.3 V .

3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO} . The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 3.23. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
f_{VCO}	PLL VCO Frequency	—	400	800	MHz
f_{PFD}^3	Phase Detector Input Frequency	—	10	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_W	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
t_{LOCK}^2	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST/ Pulse Width	—	1	—	ms
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{LOAD_REG}	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain “0” or	—	4	—	VCO cycles

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

3.20. SERDES High-Speed Data Transmitter

Table 3.24. Serial Output Timing and Levels

Symbol	Description	Min	Typ	Max	Unit
V _{TX-DIFF-PP}	Peak-Peak Differential voltage on selected amplitude ^{1, 2}	–25%	—	25%	mV, p-p
V _{TX-CM-DC}	Output common mode voltage	—	V _{CCHTX} / 2	—	mV, p-p
T _{TX-R}	Rise time (20% to 80%)	50	—	—	ps
T _{TX-F}	Fall time (80% to 20%)	50	—	—	ps
T _{TX-CM-AC-P}	RMS AC peak common-mode output voltage	—	—	20	mV
Z _{TX_SE}	Single ended output impedance for 50/75 Ω	–20%	50/75	20%	Ω
	Single ended output impedance for 6K Ω	–25%	6K	25%	Ω
RL _{TX-DIFF}	Differential return loss (with package included) ³	—	—	–10	dB
RL _{TX-COM}	Common mode return loss (with package included) ³	—	—	–6	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at V_{CCHTX}±5%.
2. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for settings of Tx amplitude.
3. Return los = –10 dB (differential), –6 dB (common mode) for 100 MHz ≤ f ≤ 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

Table 3.25. Channel Output Jitter

Description	Frequency	Min	Typ	Max	Unit
Deterministic	5 Gb/s	—	—	TBD	UI, p-p
Random	5 Gb/s	—	—	TBD	UI, p-p
Total	5 Gb/s	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	—	—	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	—	—	0.24	UI, p-p

Notes:

1. Values are measured with PRBS 2⁷–1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.
2. For ECP5-5G family devices only.

3.25. PCI Express Electrical and Timing Characteristics

3.25.1. PCIe (2.5 Gb/s) AC and DC Characteristics

Over recommended operating conditions.

Table 3.30. PCIe (2.5 Gb/s)

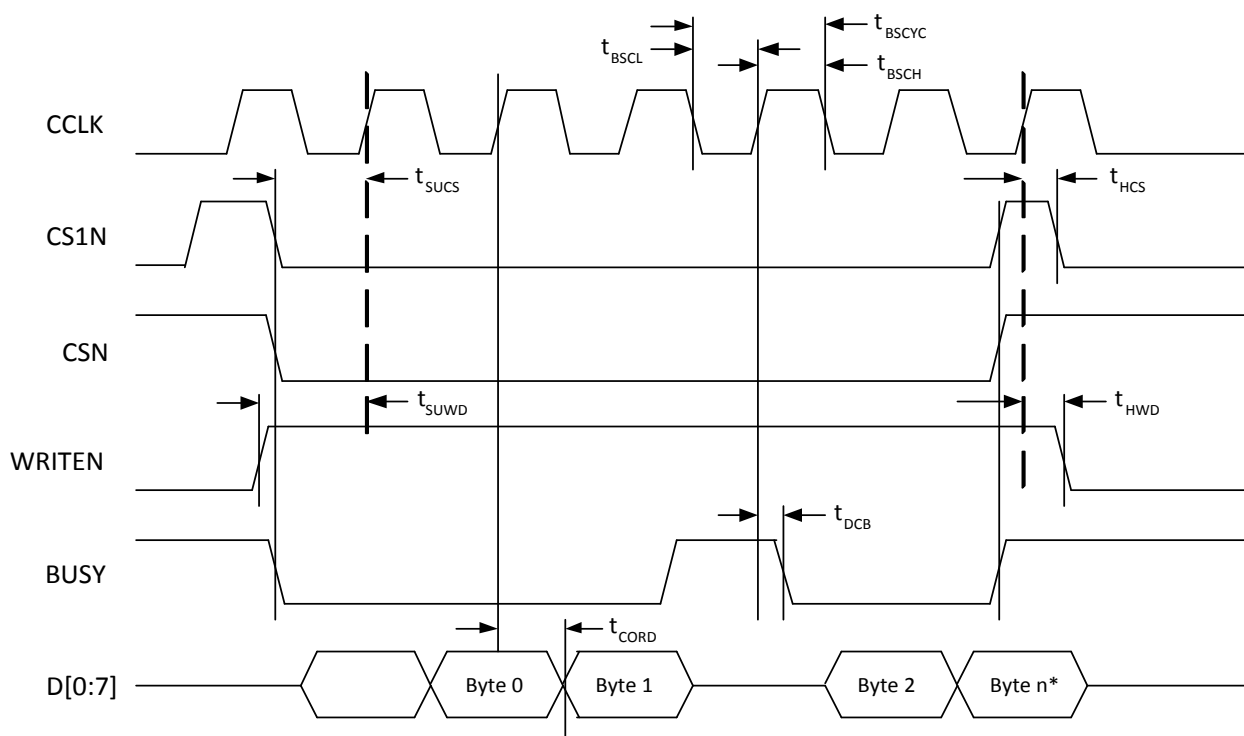
Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit¹						
UI	Unit interval	—	399.88	400	400.12	ps
V _{TX-DIFF_P-P}	Differential peak-to-peak output	—	0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio	—	–3	–3.5	–4	dB
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage	—	—	—	20	mV
V _{TX-RCV-DETECT}	Amount of voltage change allowed during receiver detection	—	—	—	600	mV
V _{TX-CM-DC}	Tx DC common mode voltage	—	0	—	V _{CCHTX}	V
I _{TX-SHORT}	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	—	—	90	mA
Z _{TX-DIFF-DC}	Differential output impedance	—	80	100	120	Ω
RL _{TX-DIFF}	Differential return loss	—	10	—	—	dB
RL _{TX-CM}	Common mode return loss	—	6.0	—	—	dB
T _{TX-RISE}	Tx output rise time	20% to 80%	0.125	—	—	UI
T _{TX-FALL}	Tx output fall time	20% to 80%	0.125	—	—	UI
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link	—	—	—	1.3	ns
T _{TX-EYE}	Transmitter eye width	—	0.75	—	—	UI
T _{TX-EYE-MEDIAN-TO-MAX-JITTER}	Maximum time between jitter median and maximum deviation from median	—	—	—	0.125	UI
Receive^{1,2}						
UI	Unit Interval	—	399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage	—	0.34 ³	—	1.2	V
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage	—	65	—	340 ³	mV
V _{RX-CM-AC_P}	RMS AC peak common-mode input voltage	—	—	—	150	mV
Z _{RX-DIFF-DC}	DC differential input impedance	—	80	100	120	Ω
Z _{RX-DC}	DC input impedance	—	40	50	60	Ω
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance	—	200K	—	—	Ω
RL _{RX-DIFF}	Differential return loss	—	10	—	—	dB
RL _{RX-CM}	Common mode return loss	—	6.0	—	—	dB

Notes:

1. Values are measured at 2.5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express 1.1 standard.

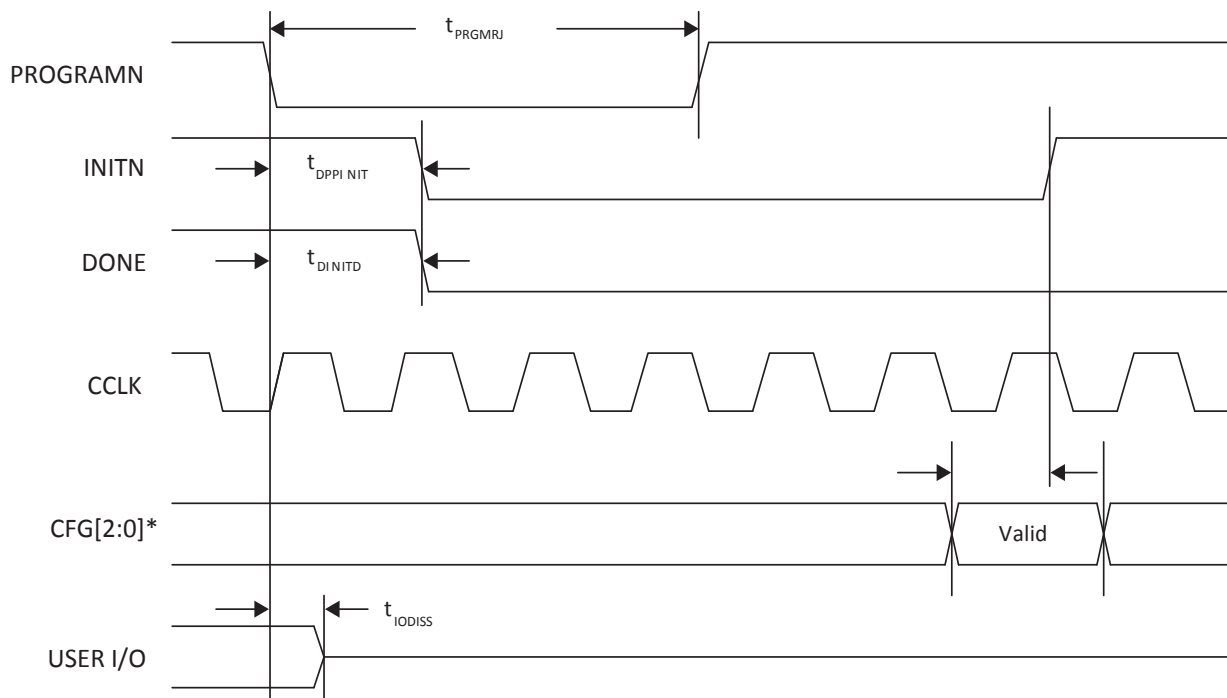
Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications (Continued)

Symbol	Parameter		Min	Max	Unit
Slave Parallel					
f_{CCLK}	CCLK input clock frequency	—	—	50	MHz
t_{BSCH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{BSCL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{CORD}	CCLK to DOUT for Read Data	—	—	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	—	1.5	—	ns
t_{HCBDI}	Data Hold Time to CCLK	—	1.5	—	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK	—	45	—	ns
t_{HCWD}	WRITEN Hold Time to CCLK	—	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	—	12	ns



*n = last byte of read cycle.

Figure 3.15. sysCONFIG Parallel Port Read Cycle



*The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

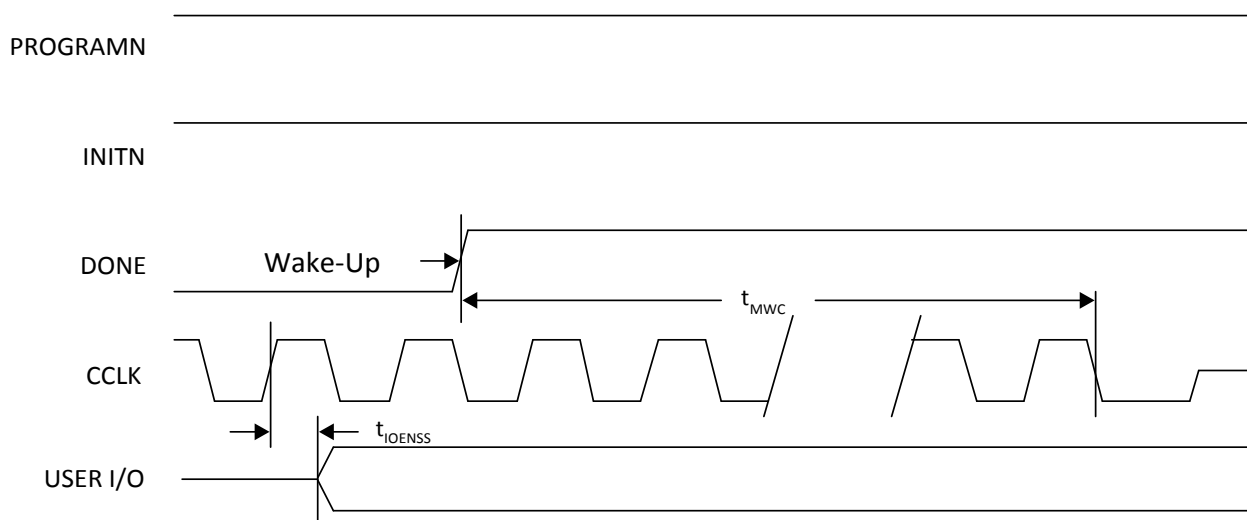


Figure 3.21. Wake-Up Timing

LFE5UM5G - XX - X XXXXX X

Device Family
LFE5UM5G (ECP5-5G FPGA
with SERDES)

Logic Capacity
25F = 25K LUTs
45F = 45K LUTs
85F = 85K LUTs

Speed
8 = Fastest

Grade
C = Commercial
I = Industrial

Package
MG285 = 285-ball csfBGA
BG381 = 381-ball caBGA
BG554 = 554-ball caBGA
BG756 = 756-ball caBGA

5.2. Ordering Part Numbers

5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	-6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	-7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	-8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	-6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	-7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	-8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	-6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	-7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	-8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	-6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	-7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	-8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	-6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	-7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	-8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	No

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclk).
			Modified section heading to XXAU/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.



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