E.J. Lattice Semiconductor Corporation - <u>LFE5U-45F-8BG381I Datasheet</u>



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	203
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-8bg381i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Copyright Notice

Copyright © 2014-2018 Lattice Semiconductor Corporation. All rights reserved. The contents of these materials contain proprietary and confidential information (including trade secrets, copyright, and other Intellectual Property interests) of Lattice Semiconductor Corporation and/or its affiliates. All rights are reserved. You are permitted to use this document and any information contained therein expressly and only for bona fide non-commercial evaluation of products and/or services from Lattice Semiconductor Corporation or its affiliates; and only in connection with your bona fide consideration of purchase or license of products or services from Lattice Semiconductor Corporation or its affiliates, and only in accordance with the terms and conditions stipulated. Contents, (in whole or in part) may not be reproduced, downloaded, disseminated, published, or transferred in any form or by any means, except with the prior written permission of Lattice Semiconductor Corporation and/or its affiliates. Copyright infringement is a violation of federal law subject to criminal and civil penalties. You have no right to copy, modify, create derivative works of, transfer, sublicense, publicly display, distribute or otherwise make these materials available, in whole or in part, to any third party. You are not permitted to reverse engineer, disassemble, or decompile any device or object code provided herewith. Lattice Semiconductor Corporation reserves the right to revoke these permissions and require the destruction or return of any and all Lattice Semiconductor Corporation proprietary materials and/or data.

Patents

The subject matter described herein may contain one or more inventions claimed in patents or patents pending owned by Lattice Semiconductor Corporation and/or its affiliates.

Trademark Acknowledgment

Lattice Semiconductor Corporation[®], the Lattice Semiconductor logo, Silicon Image[®], the Silicon Image logo, Instaport[®], the Instaport logo, InstaPrevue[®], Simplay[®], Simplay HD[®], the Simplay HD logo, Simplay Labs[™], the Simplay Labs logo, the SiBEAM Snap[™], the SiBEAM Snap logo, UltraGig[™], the UltraGig logo are trademarks or registered trademarks of Lattice Semiconductor Corporation in the United States and/or other countries. HDMI[®] and the HDMI logo with High-Definition Multimedia Interface are trademarks or registered trademarks of, and are used under license from, HDMI Licensing, LLC. in the United States or other countries. MHL[®] and the MHL logo with Mobile High-Definition Link are trademarks or registered trademarks of, and are used under license from, MHL, LLC. in the United States and/or other countries. WirelessHD[®], the WirelessHD logo, WiHD[®] and the WiHD logo are trademarks, registered trademarks or service marks of SiBeam, Inc. in the United States or other countries. HDMI Licensing, LLC; Simplay Labs, LLC; and SiBeam, Inc. are wholly owned subsidiaries of Lattice Semiconductor Corporation.

All other trademarks and registered trademarks are the property of their respective owners in the United States or other countries. The absence of a trademark symbol does not constitute a waiver of Lattice Semiconductor's trademarks or other intellectual property rights with regard to a product name, logo or slogan.

Export Controlled Document

This document contains materials that are subject to the U.S. Export Administration Regulations and may also be subject to additional export control laws and regulations (collectively "Export Laws") and may be used only in compliance with such Export Laws. Unless otherwise authorized by an officer of Lattice Semiconductor Corporation in writing, this document and the information contained herein (a) may not be used in relation to nuclear, biological or chemical weapons, or missiles capable of delivering these weapons, and (b) may not be re-exported or otherwise transferred to a third party who is known or suspected to be involved in relation to nuclear, biological or chemical weapons, or missiles capable of delivering these weapons, or to any sanctioned persons or entities.

Further Information

To request other materials, documentation, and information, contact your local Lattice Semiconductor sales office or visit the Lattice Semiconductor web site at <u>www.latticesemi.com</u>.

Disclaimers

These materials are provided on an "AS IS" basis. Lattice Semiconductor Corporation and its affiliates disclaim all representations and warranties (express, implied, statutory or otherwise), including but not limited to: (i) all implied warranties of merchantability, fitness for a particular purpose, and/or non-infringement of third party rights; (ii) all warranties arising out of course-of-dealing, usage, and/or trade; and (iii) all warranties that the information or results provided in, or that may be obtained from use of, the materials are accurate, reliable, complete, up-to-date, or produce specific outcomes. Lattice Semiconductor Corporation and its affiliates assume no liability or responsibility for any errors or omissions in these materials, makes no commitment or warranty to correct any such errors or omissions or update or keep current the information contained in these materials, and expressly disclaims all direct, indirect, special, incidental, consequential, reliance and punitive damages, including WITHOUT LIMITATION any loss of profits arising out of your access to, use or interpretation of, or actions taken or not taken based on the content of these materials. Lattice Semiconductor Corporation and its affiliates reserve the right, without notice, to periodically modify the information in these materials, and to add to, delete, and/or change any of this information.

Products and Services

The products and services described in these materials, and any other information, services, designs, know-how and/or products provided by Lattice Semiconductor Corporation and/or its affiliates are provided on "AS IS" basis, except to the extent that Lattice Semiconductor Corporation and/or its affiliates provides an applicable written limited warranty in its standard form license agreements, standard Terms and Conditions of Sale and Service or its other applicable standard form agreements, in which case such limited warranty shall apply and shall govern in lieu of all other warranties (express, statutory, or implied). EXCEPT FOR SUCH LIMITED WARRANTY, LATTICE SEMICONDUCTOR CORPORATION AND ITS AFFILIATES DISCLAIM ALL REPRESENTATIONS AND WARRANTIES (EXPRESS, IMPLIED, STATUTORY OR OTHERWISE), REGARDING THE INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS PROVIDED BY LATTICE SEMICONDUCTOR CORPORATION AND/OR ITS AFFILIATES, INCLUDING BUT NOT LIMITED TO, ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND/OR NON-INFRINGEMENT OF THIRD PARTY RIGHTS. YOU ACKNOWLEDGE AND AGREE THAT SUCH INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS HAVE NOT BEEN DESIGNED, TESTED, OR MANUFACTURED FOR USE OR RESALE IN SYSTEMS WHERE THE FAILURE, MALFUNCTION, OR ANY INACCURACY OF THESE ITEMS CARRIES A RISK OF DEATH OR SERIOUS BODILY INJURY, INCLUDING, BUT NOT LIMITED TO, USE IN NUCLEAR FACILITIES, AIRCRAFT NAVIGATION OR COMMUNICATION, EMERGENCY SYSTEMS, OR OTHER SYSTEMS WITH A SIMILAR DEGREE OF POTENTIAL HAZARD. NO PERSON IS AUTHORIZED TO MAKE ANY OTHER WARRANTY OR REPRESENTATION CONCERNING THE PERFORMANCE OF THE INFORMATION, PRODUCTS, KNOW-HOW, DESIGNS OR SERVICES OTHER THAN AS PROVIDED IN THESE TERMS AND CONDITIONS.



2. Architecture

2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and rows of sysDSP[™] Digital Signal Processing slices, as shown in Figure 2.1 on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG[™] ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.





Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows: WCK is CLK

WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2 WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.



2.3. Routing

There are many resources provided in the ECP5/ECP5-5G devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The ECP5/ECP5-5G family has an enhanced routing architecture that produces a compact design. The Diamond design software tool suites take the output of the synthesis tool and places and routes the design.

2.4. Clocking Structure

ECP5/ECP5-5G clocking structure consists of clock synthesis blocks (sysCLOCK PLL); balanced clock tree networks (PCLK and ECLK trees); and efficient clock logic modules (CLOCK DIVIDER and Dynamic Clock Select (DCS), Dynamic Clock Control (DCC) and DLL). All of these functions are described below.

2.4.1. sysCLOCK PLL

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the ECP5/ECP5-5G family support two to four full-featured General Purpose PLLs. The sysCLOCK PLLs provide the ability to synthesize clock frequencies.

The architecture of the PLL is shown in Figure 2.5. A description of the PLL functionality follows.

CLKI is the reference frequency input to the PLL and its source can come from two different external CLK inputs or from internal routing. A non-glitchless 2-to-1 input multiplexor is provided to dynamically select between two different external reference clock sources. The CLKI input feeds into the input Clock Divider block.

CLKFB is the feedback signal to the PLL which can come from internal feedback path, routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLL has four clock outputs CLKOP, CLKOS, CLKOS2 and CLKOS3. Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the primary clock network. Only CLKOP and CLKOS outputs can go to the edge clock network.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the PHASESEL, PHASEDIR, PHASESTEP, and PHASELOADREG ports.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected.







2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).



Figure 2.7. DCS Waveforms

2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.



2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.



Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

2.9. sysDSP[™] Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.











2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. Figure 2.27 shows the position of the dual blocks for the LFE5-85. Table 2.13 shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).



Table 3.10. ECP5-5G

Symbol	Description	Тур	Max	Unit			
Standby (Power Down)							
I _{CCA-SB}	V _{CCA} Power Supply Current (Per Channel)	4	9.5	mA			
I _{CCHRX-SB} ⁴	V _{CCHRX} , Input Buffer Current (Per Channel)	_	0.1	mA			
I _{CCHTX-SB}	V _{CCHTX} , Output Buffer Current (Per Channel)	_	0.9	mA			
Operating (Data	Rate = 5 Gb/s)						
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	58	67	mA			
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA			
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA			
Operating (Data	Rate = 3.2 Gb/s)						
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	48	57	mA			
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA			
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA			
Operating (Data	Rate = 2.5 Gb/s)						
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	44	53	mA			
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA			
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA			
Operating (Data	Rate = 1.25 Gb/s)						
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	36	46	mA			
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA			
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA			
Operating (Data	Rate = 270 Mb/s)						
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	30	40	mA			
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA			
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	8	10	mA			

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled

2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.

3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.

4. For ICCHRX-SB, during Standby, input termination on Rx are disabled.

5. For ICCHRX-OP, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.



3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard		Vccio		V _{REF} (V)			
Stanuaru	Min	Тур	Max	Min	Тур	Max	
LVCMOS331	3.135	3.3	3.465	—	—	—	
LVCMOS33D ³ Output	3.135	3.3	3.465	_	—	—	
LVCMOS251	2.375	2.5	2.625	—	—	—	
LVCMOS18	1.71	1.8	1.89	—	—	—	
LVCMOS15	1.425	1.5	1.575	—	—	—	
LVCMOS12 ¹	1.14	1.2	1.26	—	—	—	
LVTTL33 ¹	3.135	3.3	3.465	—	—	—	
SSTL15_I, _II ²	1.43	1.5	1.57	0.68	0.75	0.9	
SSTL18_I, _II ²	1.71	1.8	1.89	0.833	0.9	0.969	
SSTL135_I, _II ²	1.28	1.35	1.42	0.6	0.675	0.75	
HSUL12 ²	1.14	1.2	1.26	0.588	0.6	0.612	
MIPI D-PHY LP Input ^{3, 5}	1.425	1.5	1.575	—	—	—	
LVDS25 ^{1, 3} Output	2.375	2.5	2.625	—	—	—	
subLVS ³ (Input only)	—	—	—	—	—	—	
SLVS ³ (Input only)	—	—	—	—	—	—	
LVDS25E ³ Output	2.375	2.5	2.625	—	—	—	
MLVDS ³ Output	2.375	2.5	2.625	—	—	—	
LVPECL33 ^{1, 3} Output	3.135	3.3	3.465	—	—	—	
BLVDS25 ^{1, 3} Output	2.375	2.5	2.625	—	—	—	
HSULD12D ^{2, 3}	1.14	1.2	1.26	—	—	—	
SSTL135D_I, II ^{2, 3}	1.28	1.35	1.42	_	_	_	
SSTL15D_I, II ^{2, 3}	1.43	1.5	1.57	—	—	—	
SSTL18D_I ^{1, 2, 3} , II ^{1, 2, 3}	1.71	1.8	1.89	_	_	_	

Notes:

1. For input voltage compatibility, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).

2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.

3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power

4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.

5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL} . It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.



3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.



Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V _{CCIO}	Output Driver Supply (±5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
Rs	Driver Series Resistor (±1%)	158	Ω
R _P	Driver Parallel Resistor (±1%)	140	Ω
R _T	Receiver Termination (±1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
ZBACK	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.





3.14.7. MLVDS25

The ECP5/ECP5-5G devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.



Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Deverenter	Description	Тур	11	
Parameter	Description	Zo=50 Ω	Zo=70 Ω	Onit
V _{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
Rs	Driver Series Resistor (±1%)	35.00	35.00	Ω
R _{TL}	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
R _{TR}	Receiver Termination (±1%)	50.00	70.00	Ω
V _{OH}	Output High Voltage	1.52	1.60	V
V _{OL}	Output Low Voltage	0.98	0.90	V
V _{OD}	Output Differential Voltage	0.54	0.70	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	21.74	20.00	mA

Table 3.17. MLVDS25 DC Conditions

Note: For input buffer, see LVDS Table 3.13 on page 55.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.



3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Devementer	Provinciation -8		8	-7		-6		11	
Parameter	Description	Device	Min	Max	Min	Max	Min	Max	Unit
Clocks									
Primary Clock	Primary Clock								
f _{MAX_PRI}	Frequency for Primary Clock Tree	_	—	370	—	303	_	257	MHz
t _{w_pri}	Clock Pulse Width for Primary Clock	-	0.8	—	0.9	_	1.0	-	ns
t _{skew_pri}	Primary Clock Skew within a Device	-	_	420	_	462	-	505	ps
Edge Clock									
f _{MAX_EDGE}	Frequency for Edge Clock Tree		_	400	—	350		312	MHz
tw_edge	Clock Pulse Width for Edge Clock	_	1.175	—	1.344	—	1.50	-	ns
t _{skew_edge}	Edge Clock Skew within a Bank	_	—	160	—	180	-	200	ps
Generic SDR Input									
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ithout PL	L					
t _{co}	Clock to Output - PIO Output Register	All Devices	_	5.4	_	6.1	-	6.8	ns
t _{su}	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	_	0	_	ns
t _H	Clock to Data Hold - PIO Input Register	All Devices	2.7	_	3	_	3.3	Ι	ns
t _{su_del}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	_	1.33	_	1.46	-	ns
t _{h_del}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	_	0	_	0	-	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	_	400	_	350	_	312	MHz
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ith PLL						
t _{copll}	Clock to Output - PIO Output Register	All Devices	_	3.5	_	3.8	_	4.1	ns
t _{supll}	Clock to Data Setup - PIO Input Register	All Devices	0.7	-	0.78	_	0.85	_	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	_	0.89	_	0.98	_	ns
t _{su_delpll}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	_	1.78	_	1.95	_	ns

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.





Figure 3.11. Receiver DDRX71_RX Waveforms



Figure 3.12. Transmitter DDRX71_TX Waveforms

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.



3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.2	26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit ³	
Transmit Data Latency ¹								
T 1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	-	1	byte clk	
11	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk	
Т2	8b10b Encoder	_	—	—	2	1	byte clk	
Т3	SERDES Bridge transmit	_	—	—	2	1	byte clk	
тл	Serializer: 8-bit mode	_	—	—	15 + ∆1	—	UI + ps	
14	Serializer: 10-bit mode	_	—	—	18 + Δ 1	—	UI + ps	
тс	Pre-emphasis ON	_	—	—	1 + Δ 2	—	UI + ps	
Pre-emphasis OFF		_	—	—	0 + ∆3	—	UI + ps	
Receive	Data Latency ²							
D1	Equalization ON	_	—	—	Δ1	—	UI + ps	
KI .	Equalization OFF	_	—	—	Δ2	—	UI + ps	
22	Deserializer: 8-bit mode	_	—	—	10 + ∆3	—	UI + ps	
R2	Deserializer: 10-bit mode	_	—	—	12 + ∆3	—	UI + ps	
R3	SERDES Bridge receive	_	—	—	2	—	byte clk	
R4	Word alignment	3.1	—	4	—	1	byte clk	
R5	8b10b decoder	_	—	—	1	0	byte clk	
R6	Clock Tolerance Compensation	7	15	23	_	1	byte clk	
57	FPGA Bridge - Gearing disabled with same clocks	4	_	5	_	1	byte clk	
К/	FPGA Bridge - Gearing enabled	7	_	9	_	_	word clk	

Notes:

1. $\Delta 1 = -245 \text{ ps}, \Delta 2 = +88 \text{ ps}, \Delta 3 = +112 \text{ ps}.$

2. $\Delta 1 = +118 \text{ ps}, \Delta 2 = +132 \text{ ps}, \Delta 3 = +700 \text{ ps}.$

3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).







Table 3.31. PCIe (5 Gb/s) (Continued)

Symbol	Description	Test Conditions	Min	Тур	Мах	Unit
Receive ^{1, 2}		' 				
UI	Unit Interval	—	199.94	200	200.06	ps
V _{RX-DIFF-PP}	Differential Rx peak-peak voltage	—	0.34 ³	_	1.2	V, p-p
T _{RX-RJ-RMS}	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	_	Ι	4.2	ps, RMS
T _{RX-DJ}	Receiver deterministic jitter tolerance	—	—	_	88	ps
V _{RX-CM-AC}	Common mode noise from Rx	_	_	Ι		тV <i>,</i> p-р
D	Receiver differential Return Loss,	50 MHz < freq < 1.25 GHz	10	Ι	Ι	dB
NLRX-DIFF	package plus silicon	1.25 GHz < freq < 2.5 GHz	8	Ι	Ι	dB
R _{LRX-CM}	Receiver common mode Return Loss, package plus silicon	_	6	Ι	Ι	dB
Z _{RX-DC}	Receiver DC single ended impedance	—	40		60	Ω
Z _{RX-HIGH-IMP-DC}	Receiver DC single ended impedance when powered down	_	200K		I	Ω
V _{RX-CM-AC-P}	Rx AC peak common mode voltage	_	_	_		mV <i>,</i> peak
V _{RX-IDLE-DET-DIFF-PP}	Electrical Idle Detect Threshold	_	65	-	340 ³	mv,
L _{RX-SKEW}	Receiver lane-lane skew	_	_	_	8	ns

Notes:

1. Values are measured at 5 Gb/s.

2. Measured with external AC-coupling on the receiver.

3. Not in compliance with PCI Express standard.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.





*The CFG pins are normally static (hardwired).









4. Pinout Information

4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[L/R] [Group Number]_[A/B/C/D]	1/0	 [L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIO A and B are grouped as a pair, and PIO C and D are group as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer. Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω.
P[T/B][Group Number]_[A/B]	I/O	 [T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer. PIO A/B forms a pair of emulated differential output buffer.
GSRN	1	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	_	No connect.
RESERVED	_	This pin is reserved and should not be connected to anything on the board.
GND	_	Ground. Dedicated pins.
V _{cc}	_	Power supply pins for core logic. Dedicated pins. V _{CC} = 1.1 V (ECP5), 1.2 V (ECP5UM5G)
Vccaux	_	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. $V_{CCAUX} = 2.5 V$.
V _{CCIOx}	_	Dedicated power supply pins for I/O bank x. V_{CCIO8} is used for configuration and JTAG.
VREF1_x	-	Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as VREF1 input. When not used, they may be used as I/O pins.
PLL, DLL and Clock Functions	1	
[LOC][_GPLL[T, C]_IN	I	General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not configured as GPLL input pads, they can be used as general purpose I/O pins.
GR_PCLK[Bank][num]	I	General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to ECP5 sysClock PLL/DLL Design and Usage Guide (TN1263). These pins are shared I/O pins. When not configured as GR pins, they can be used as general purpose I/O pins.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/ O pins. When not configured as PCLK pins, they can be used as general purpose I/O pins.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.





5.2. Ordering Part Numbers

5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	-6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	-7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	-8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	-6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	-7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	-8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	-6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	-7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	-8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	-6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	-7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	-8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	-6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	-7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	-8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	No

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.



(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.