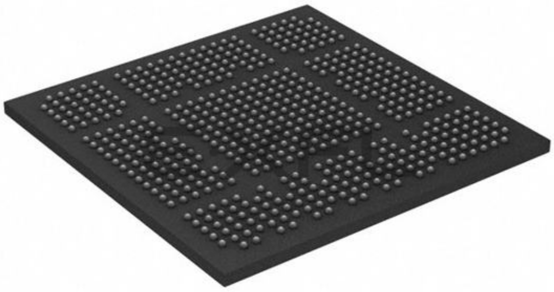


Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 11000 |
| Number of Logic Elements/Cells | 44000 |
| Total RAM Bits | 1990656 |
| Number of I/O | 245 |
| Number of Gates | - |
| Voltage - Supply | 1.045V ~ 1.155V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 554-FBGA |
| Supplier Device Package | 554-CABGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-45f-8bg554i |

# Figures



© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

# 2. Architecture

## 2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2.1 on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG™ ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

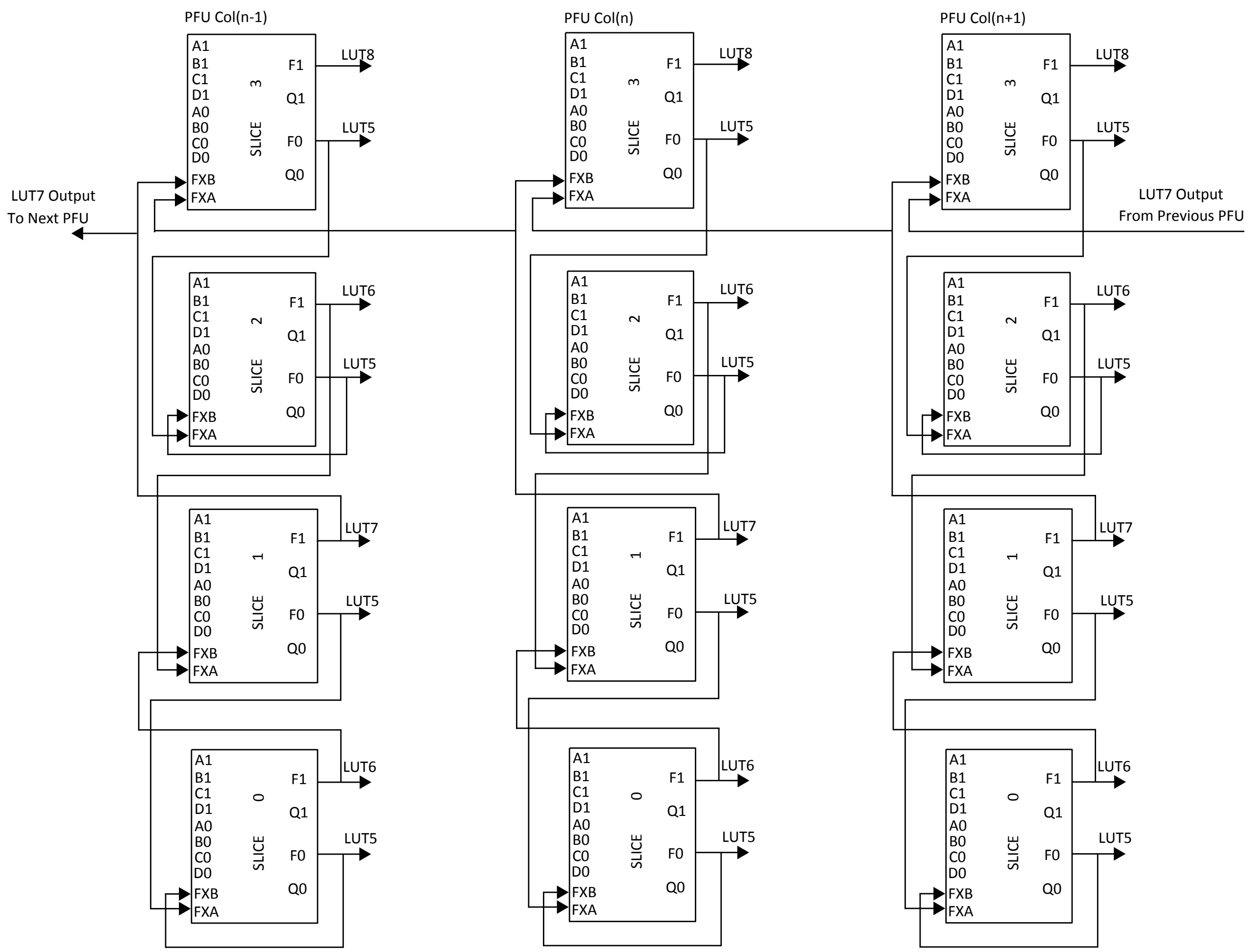



**Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8**

**Table 2.2. Slice Signal Descriptions**

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCI | Fast Carry-in[1] |
| Input | Inter-slice signal | FXA | Intermediate signal to generate LUT6, LUT7 and LUT8[2] |
| Input | Inter-slice signal | FXB | Intermediate signal to generate LUT6, LUT7 and LUT8[2] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Inter-PFU signal | FCO | Fast carry chain output[1] |

**Notes**:

1. See Figure 2.3 on page 15 for connection details.
2. Requires two adjacent PFUs.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

### 2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

**Logic Mode**

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

**Ripple Mode**

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

**RAM Mode**

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

**Table 2.3. Number of Slices Required to Implement Distributed RAM**

| | SPR 16 X 4 | PDPR 16 X 4 |
|---|---|---|
| Number of slices | 3 | 6 |

**Note**: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

**ROM Mode**

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

#### 2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

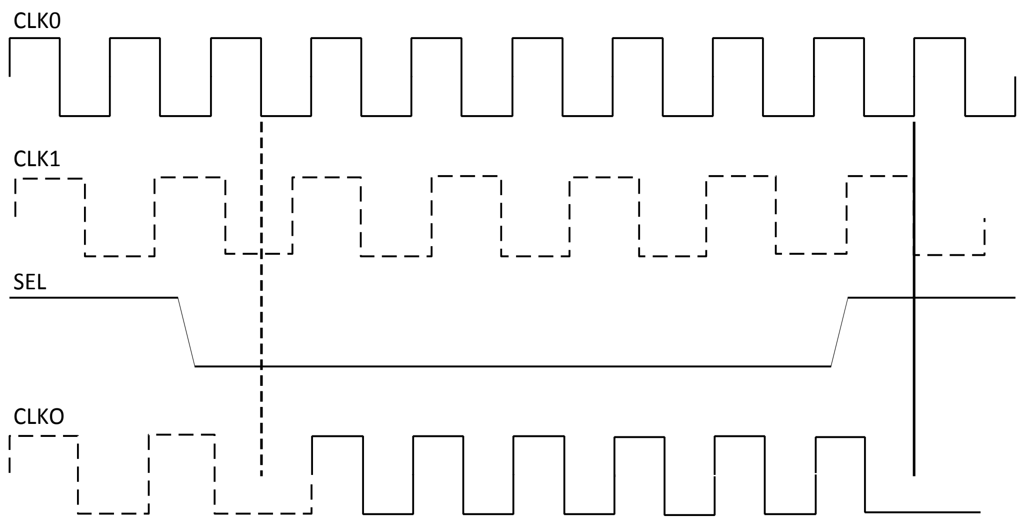



**Figure 2.7. DCS Waveforms**

### 2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- 5*5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
    - Minimizes fabric use for common DSP and ALU functions
    - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
    - Provides matching pipeline registers
    - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
    - Dynamically selectable ALU OPCODE
    - Ternary arithmetic (addition/subtraction of three inputs)
    - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
    - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
    - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5/ ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.

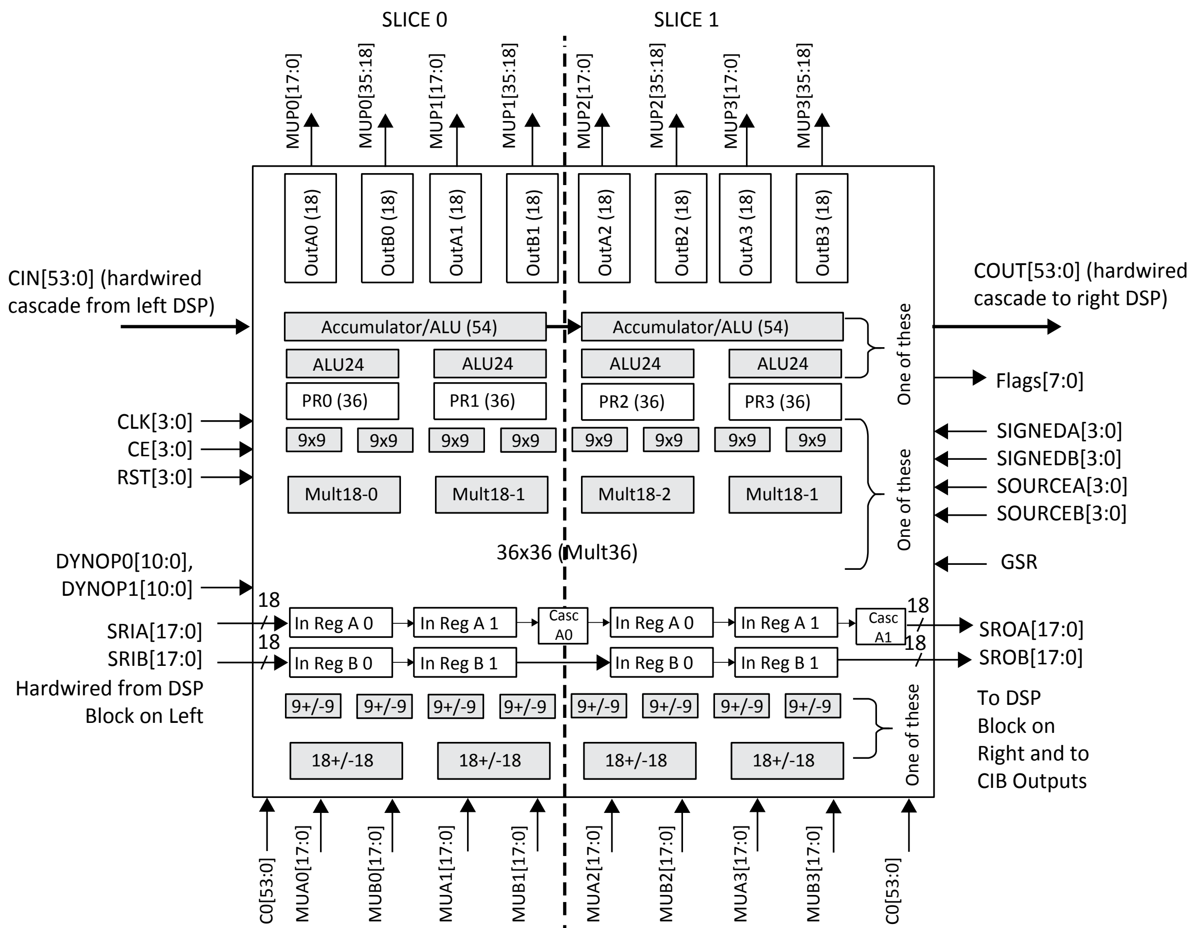



**Figure 2.14. Simplified sysDSP Slice Block Diagram**

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

## 2.11. PIO

The PIO contains three blocks: an input register block, output register block, and tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

### 2.11.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers to shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers samples the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The top side of the device supports IDDRX1 gearing function. For more information on gearing function, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

Figure 2.17 shows the input register block for the PIOs on the top edge.

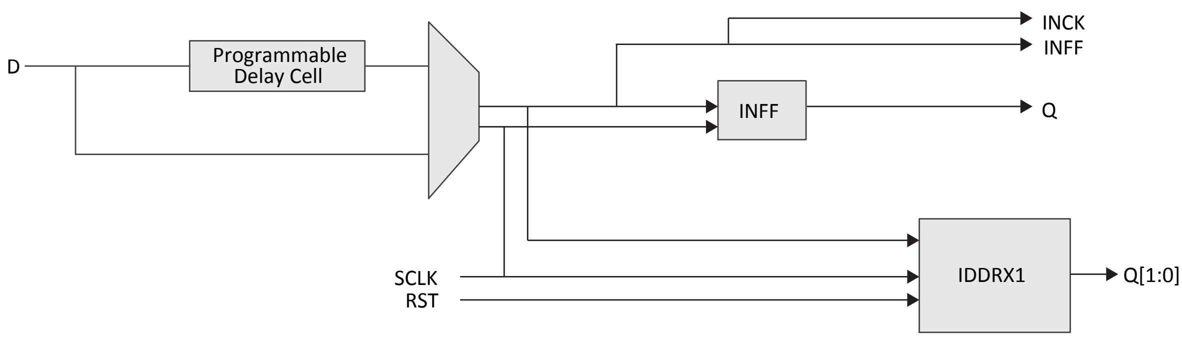
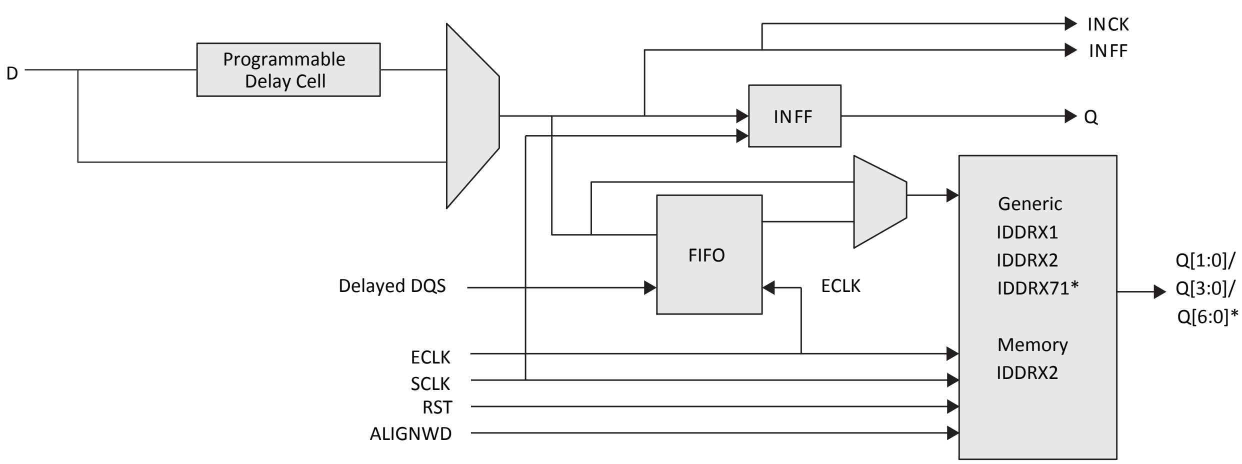



**Figure 2.17. Input Register Block for PIO on Top Side of the Device**

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.




*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

**Figure 2.18. Input Register Block for PIO on Left and Right Side of the Device**

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

#### 2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in DDR Memory Support section on page 35.

**Table 2.8. Input Block Port Description**

| Name | Type | Description |
|---|---|---|
| D | Input | High Speed Data Input |
| Q[1:0]/Q[3:0]/Q[6:0] | Output | Low Speed Data to the device core |
| RST | Input | Reset to the Output Block |
| SCLK | Input | Slow Speed System Clock |
| ECLK | Input | High Speed Edge Clock |
| DQS | Input | Clock from DQS control Block used to clock DDR memory data |
| ALIGNWD | Input | Data Alignment signal from device core. |

### 2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in Figure 2.19. The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

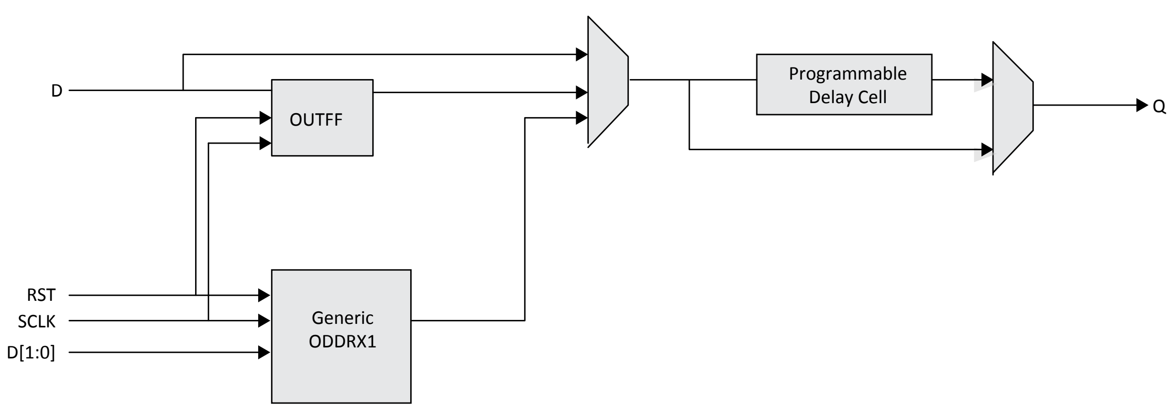



**Figure 2.19. Output Register Block on Top Side**

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

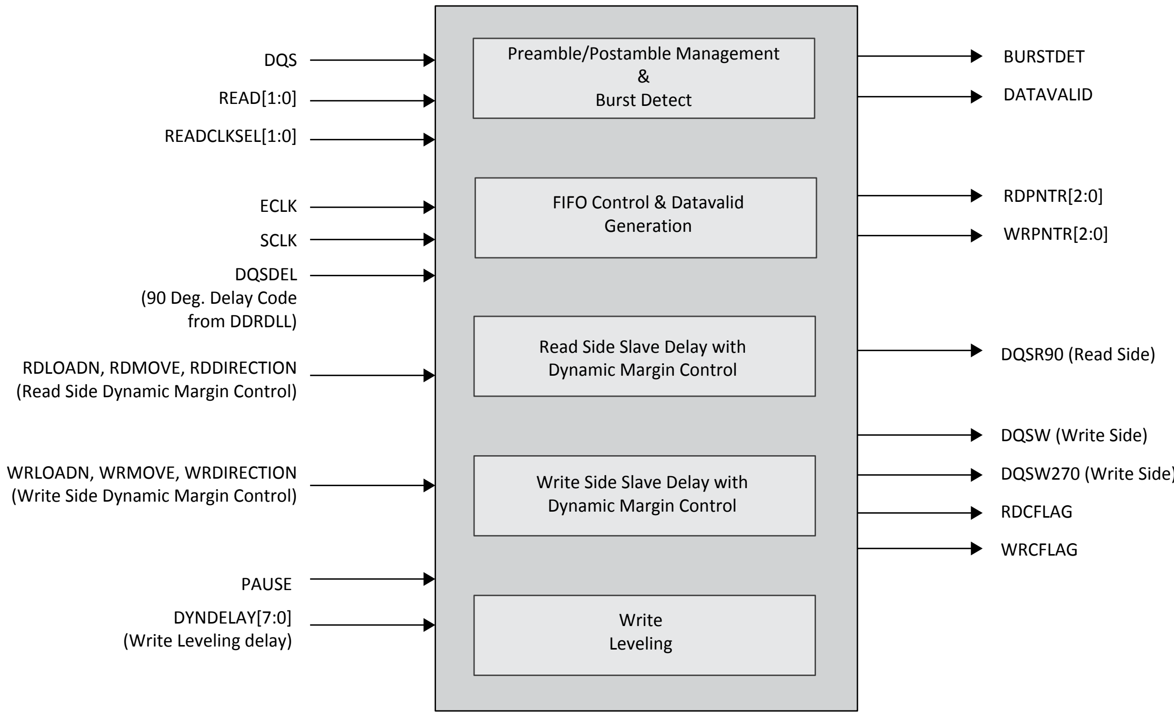



**Figure 2.24. DQS Control and Delay Block (DQSBUF)**

**Table 2.11. DQSBUF Port List Description**

| Name | Type | Description |
|---|---|---|
| DQS | Input | DDR memory DQS strobe |
| READ[1:0] | Input | Read Input from DDR Controller |
| READCLKSEL[1:0] | Input | Read pulse selection |
| SCLK | Input | Slow System Clock |
| ECLK | Input | High Speed Edge Clock (same frequency as DDR memory) |
| DQSDEL | Input | 90° Delay Code from DDRDLL |
| RDLOADN, RDMOVE, RDDIRECTION | Input | Dynamic Margin Control ports for Read delay |
| WRLOADN, WRMOVE, WRDIRECTION | Input | Dynamic Margin Control ports for Write delay |
| PAUSE | Input | Used by DDR Controller to Pause write side signals during DDRDLL Code update or Write Leveling |
| DYNDELAY[7:0] | Input | Dynamic Write Leveling Delay Control |
| DQSR90 | Output | 90° delay DQS used for Read |
| DQSW270 | Output | 90° delay clock used for DQ Write |
| DQSW | Output | Clock used for DQS Write |
| RDPNTR[2:0] | Output | Read Pointer for IFIFO module |
| WRPNTR[2:0] | Output | Write Pointer for IFIFO module |
| DATAVALID | Output | Signal indicating start of valid data |
| BURSTDET | Output | Burst Detect indicator |
| RDFLAG | Output | Read Dynamic Margin Control output to indicate max value |
| WRFLAG | Output | Write Dynamic Margin Control output to indicate max value |

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

- Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the $V_{CCIO}$ voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

  Bank 4 I/O only exists in the LFE5-85 device.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Diamond tool.

- Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

### 2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when $V_{CC}$, $V_{CCIO8}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. $V_{CCIO}$ supplies should be powered-up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies.

### 2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

**Table 3.20. Register-to-Register Performance**

| Function | –8 Timing | Unit |
|---|---|---|
| **Basic Functions** | | |
| 16-Bit Decoder | 441 | MHz |
| 32-Bit Decoder | 441 | MHz |
| 64-Bit Decoder | 332 | MHz |
| 4:1 Mux | 441 | MHz |
| 8:1 Mux | 441 | MHz |
| 16:1 Mux | 441 | MHz |
| 32:1 Mux | 441 | MHz |
| 8-Bit Adder | 441 | MHz |
| 16-Bit Adder | 441 | MHz |
| 64-Bit Adder | 441 | MHz |
| 16-Bit Counter | 384 | MHz |
| 32-Bit Counter | 317 | MHz |
| 64-Bit Counter | 263 | MHz |
| 64-Bit Accumulator | 288 | MHz |
| **Embedded Memory Functions** | | |
| 1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers | 272 | MHz |
| 1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers | 214 | MHz |
| **Distributed Memory Functions** | | |
| 16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU) | 441 | MHz |
| 16 x 4 Pseudo-Dual Port (Two PFUs) | 441 | MHz |
| **DSP Functions** | | |
| 9 x 9 Multiplier (All Registers) | 225 | MHz |
| 18 x 18 Multiplier (All Registers) | 225 | MHz |
| 36 x 36 Multiplier (All Registers) | 225 | MHz |
| 18 x 18 Multiply-Add/Sub (All Registers) | 225 | MHz |
| 18 x 18 Multiply/Accumulate (Input and Output Registers) | 225 | MHz |

**Notes**:

1. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

## 3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

## 3.18. External Switching Characteristics

Over recommended commercial operating conditions.

**Table 3.22. ECP5/ECP5-5G External Switching Characteristics**

| Parameter | Description | Device | –8 | | –7 | | –6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| **Clocks** | | | | | | | | | |
| **Primary Clock** | | | | | | | | | |
| $f_{MAX\_PRI}$ | Frequency for Primary Clock Tree | — | — | 370 | — | 303 | — | 257 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | — | 0.8 | — | 0.9 | — | 1.0 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew within a Device | — | — | 420 | — | 462 | — | 505 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX\_EDGE}$ | Frequency for Edge Clock Tree | — | — | 400 | — | 350 | — | 312 | MHz |
| $t_{W\_EDGE}$ | Clock Pulse Width for Edge Clock | — | 1.175 | — | 1.344 | — | 1.50 | — | ns |
| $t_{SKEW\_EDGE}$ | Edge Clock Skew within a Bank | — | — | 160 | — | 180 | — | 200 | ps |
| **Generic SDR Input** | | | | | | | | | |
| **General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL** | | | | | | | | | |
| $t_{CO}$ | Clock to Output - PIO Output Register | All Devices | — | 5.4 | — | 6.1 | — | 6.8 | ns |
| $t_{SU}$ | Clock to Data Setup - PIO Input Register | All Devices | 0 | — | 0 | — | 0 | — | ns |
| $t_{H}$ | Clock to Data Hold - PIO Input Register | All Devices | 2.7 | — | 3 | — | 3.3 | — | ns |
| $t_{SU\_DEL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | All Devices | 1.2 | — | 1.33 | — | 1.46 | — | ns |
| $t_{H\_DEL}$ | Clock to Data Hold - PIO Input Register with Data Input Delay | All Devices | 0 | — | 0 | — | 0 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | All Devices | — | 400 | — | 350 | — | 312 | MHz |
| **General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | All Devices | — | 3.5 | — | 3.8 | — | 4.1 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | All Devices | 0.7 | — | 0.78 | — | 0.85 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | All Devices | 0.8 | — | 0.89 | — | 0.98 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | All Devices | 1.6 | — | 1.78 | — | 1.95 | — | ns |

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

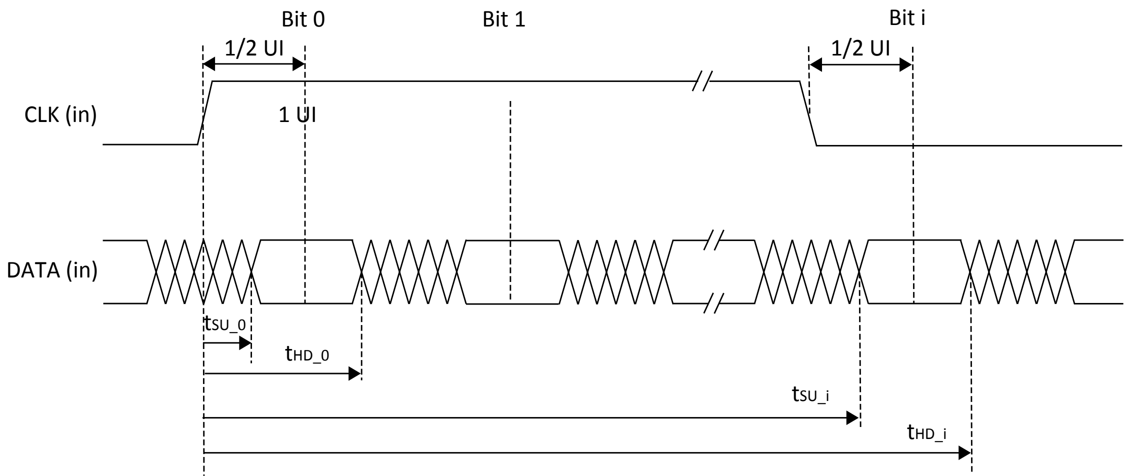



**Figure 3.11. Receiver DDRX71_RX Waveforms**

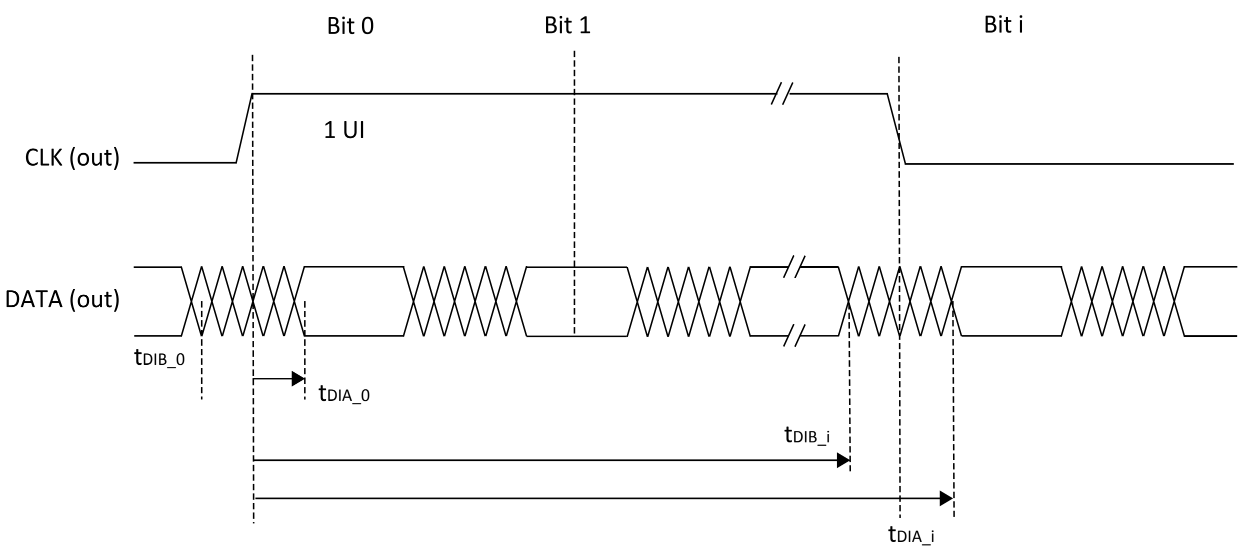



**Figure 3.12. Transmitter DDRX71_TX Waveforms**

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

## 3.20. SERDES High-Speed Data Transmitter

**Table 3.24. Serial Output Timing and Levels**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{TX-DIFF-PP}$ | Peak-Peak Differential voltage on selected amplitude[1, 2] | –25% | — | 25% | mV, p-p |
| $V_{TX-CM-DC}$ | Output common mode voltage | — | $V_{CCHTX}$ / 2 | — | mV, p-p |
| $T_{TX-R}$ | Rise time (20% to 80%) | 50 | — | — | ps |
| $T_{TX-F}$ | Fall time (80% to 20%) | 50 | — | — | ps |
| $T_{TX-CM-AC-P}$ | RMS AC peak common-mode output voltage | — | — | 20 | mV |
| $Z_{TX\_SE}$ | Single ended output impedance for 50/75 Ω | –20% | 50/75 | 20% | Ω |
| | Single ended output impedance for 6K Ω | –25% | 6K | 25% | Ω |
| $RL_{TX\_DIFF}$ | Differential return loss (with package included) [3] | — | — | –10 | dB |
| $RL_{TX\_COM}$ | Common mode return loss (with package included) [3] | — | — | –6 | dB |

**Notes**:

1. Measured with 50 Ω Tx Driver impedance at $V_{CCHTX}$±5%.
2. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for settings of Tx amplitude.
3. Return los = −10 dB (differential), –6 dB (common mode) for 100 MHz ≤ f <= 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

**Table 3.25. Channel Output Jitter**

| Description | Frequency | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Deterministic | 5 Gb/s | — | — | TBD | UI, p-p |
| Random | 5 Gb/s | — | — | TBD | UI, p-p |
| Total | 5 Gb/s | — | — | TBD | UI, p-p |
| Deterministic | 3.125 Gb/s | — | — | 0.17 | UI, p-p |
| Random | 3.125 Gb/s | — | — | 0.25 | UI, p-p |
| Total | 3.125 Gb/s | — | — | 0.35 | UI, p-p |
| Deterministic | 2.5 Gb/s | — | — | 0.17 | UI, p-p |
| Random | 2.5 Gb/s | — | — | 0.20 | UI, p-p |
| Total | 2.5 Gb/s | — | — | 0.35 | UI, p-p |
| Deterministic | 1.25 Gb/s | — | — | 0.10 | UI, p-p |
| Random | 1.25 Gb/s | — | — | 0.22 | UI, p-p |
| Total | 1.25 Gb/s | — | — | 0.24 | UI, p-p |

**Notes**:

1. Values are measured with PRBS $2^7$-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.
2. For ECP5-5G family devices only.

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

## 3.24. SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3.29 specifies reference clock requirements, over the full range of operating conditions.

**Table 3.29. External Reference Clock Specification (refclkp/refclkn)**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{REF}$ | Frequency range | 50 | — | 320 | MHz |
| $F_{REF-PPM}$ | Frequency tolerance[1] | –1000 | — | 1000 | ppm |
| $V_{REF-IN-SE}$ | Input swing, single-ended clock[2, 4] | 200 | — | $V_{CCAUXA}$ | mV, p-p |
| $V_{REF-IN-DIFF}$ | Input swing, differential clock | 200 | — | $2*V_{CCAUXA}$ | mV, p-p differential |
| $V_{REF-IN}$ | Input levels | 0 | — | $V_{CCAUXA} + 0.4$ | V |
| $D_{REF}$ | Duty cycle[3] | 40 | — | 60 | % |
| $T_{REF-R}$ | Rise time (20% to 80%) | 200 | 500 | 1000 | ps |
| $T_{REF-F}$ | Fall time (80% to 20%) | 200 | 500 | 1000 | ps |
| $Z_{REF-IN-TERM-DIFF}$ | Differential input termination | –30% | 100/HiZ | +30% | Ω |
| $C_{REF-IN-CAP}$ | Input capacitance | — | — | 7 | pF |

**Notes**:

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
3. Measured at 50% amplitude.
4. Single-ended clocking is achieved by applying a reference voltage $V_{REF}$ on REFCLKN input, with the clock applied to REFCLKP input pin. $V_{REF}$ should be set to mid-point of the REFCLKP voltage swing.

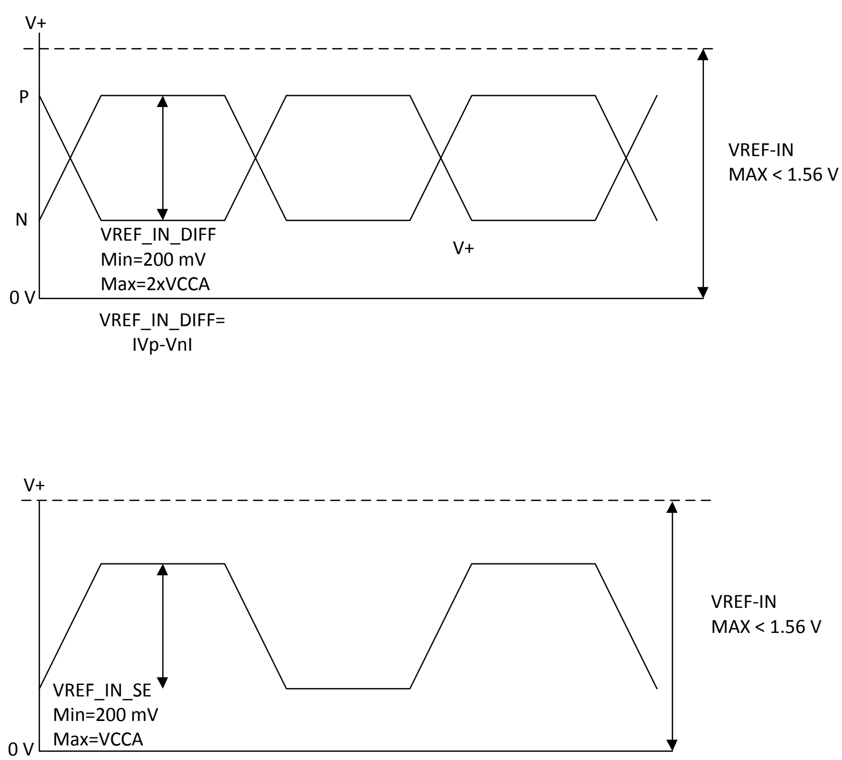
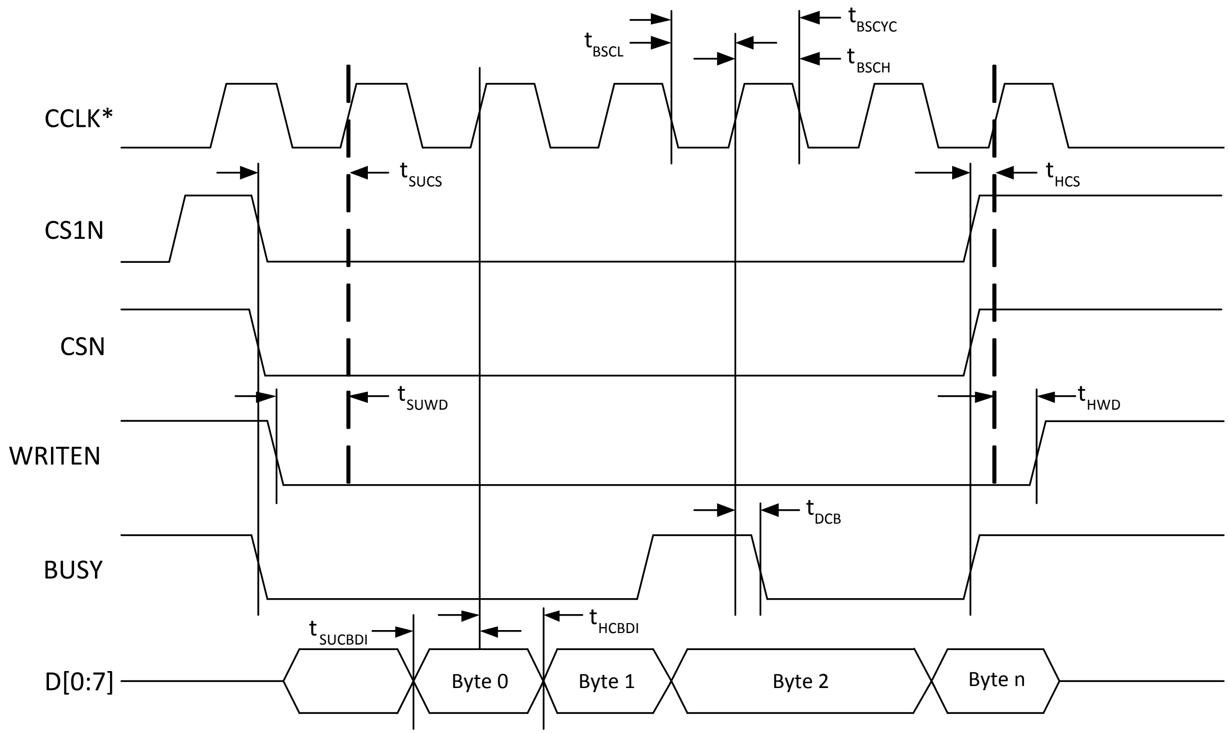



**Figure 3.14. SERDES External Reference Clock Waveforms**

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.




*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

**Figure 3.16. sysCONFIG Parallel Port Write Cycle**

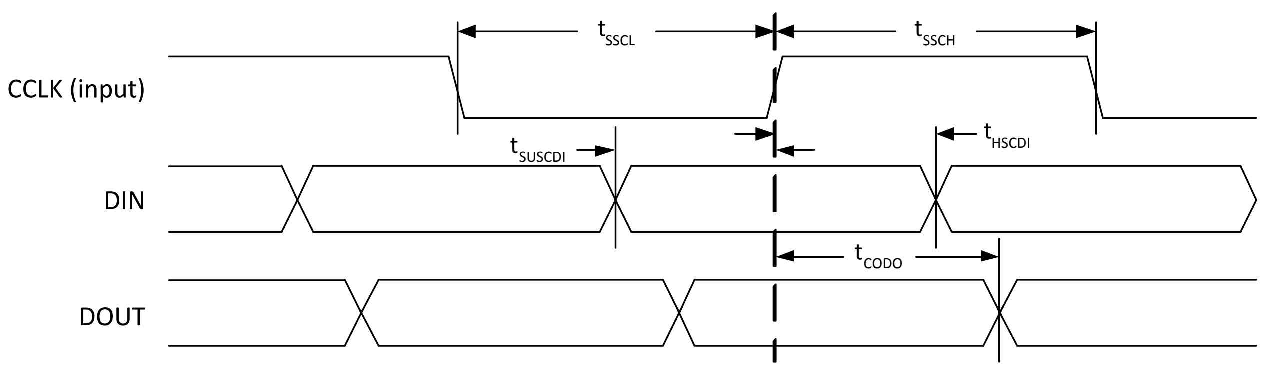
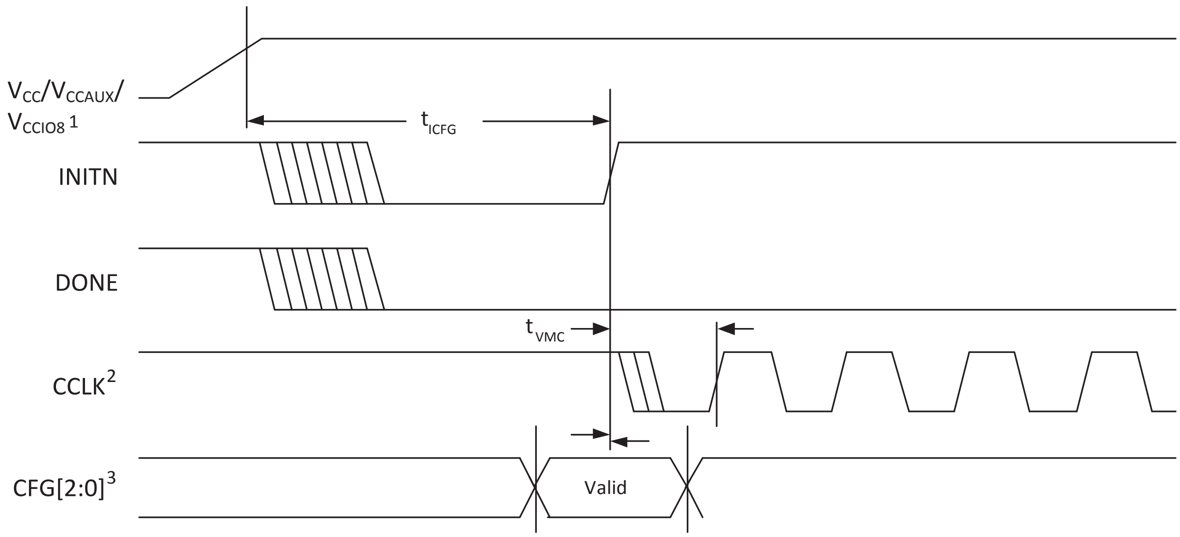



**Figure 3.17. sysCONFIG Slave Serial Port Timing**

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.




1. Time taken from $V_{CC}$, $V_{CCAUX}$ or $V_{CCIO8}$, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hardwired).

**Figure 3.18. Power-On-Reset (POR) Timing**

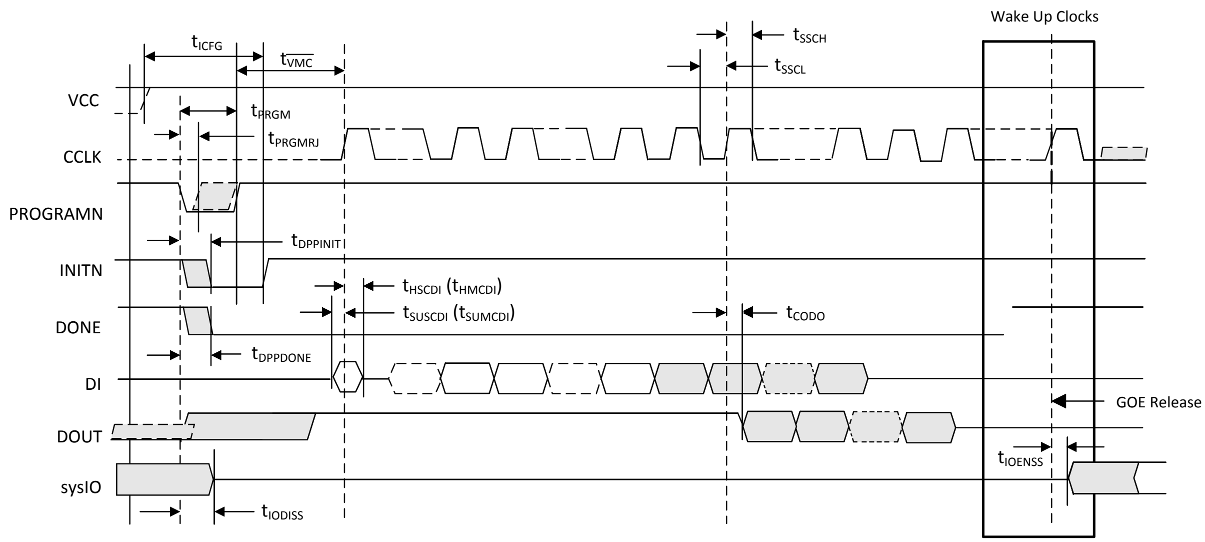



**Figure 3.19. sysCONFIG Port Timing**

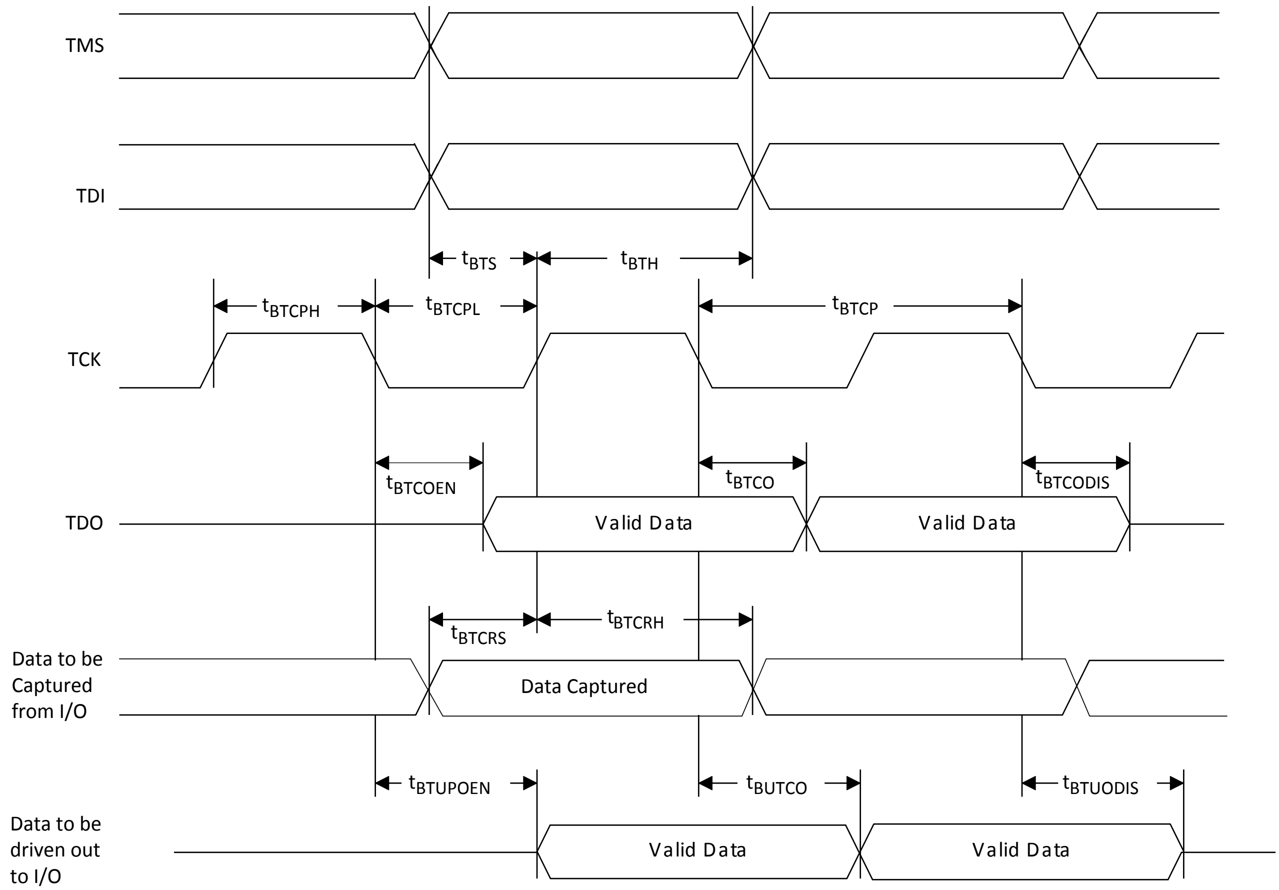
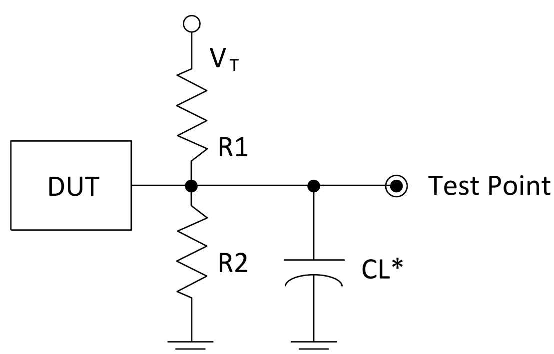



**Figure 3.23. JTAG Port Timing Waveforms**

## 3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.




*CL Includes Test Fixture and Probe Capacitance

**Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards**

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

*(Continued)*

| Date | Version | Section | Change Summary |
|---|---|---|---|
| November 2015 | 1.5 | All | Added ECP5-5G device family. |
| | | | Changed document title to ECP5 and ECP5-5G Family Data Sheet. |
| | 1.4 | General Description | Updated Features section. Added support for eDP in RDR and HDR. |
| | | Architecture | Updated Overview section.<br>Revised Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level). Modified Flexible sysIO description and Note. |
| | | | Updated SERDES and Physical Coding Sublayer section.<br>• Changed E.24.V in CPRI protocol to E.24.LV.<br>• Removed "1.1 V" from paragraph on unused Dual. |
| | | DC and Switching Characteristics | Updated Hot Socketing Requirements section. Revised $V_{CCHTX}$ in table notes 1 and 3. Indicated $V_{CCHTX}$ in table note 4. |
| | | | Updated SERDES High-Speed Data Transmitter section. Revised $V_{CCHTX}$ in table note 1. |
| | | Ordering Information | Updated ECP5/ECP5-5G Part Number Description section. Changed "LFE5 FPGA" under Device Family to "ECP5 FPGA". |
| August 2015 | 1.3 | General Description | Updated Features section.<br>• Removed SMPTE3G under Embedded SERDES.<br>• Added Single Event Upset (SEU) Mitigation Support.<br>Removed SMPTE protocol in fifth paragraph. |
| | | Architecture | General update. |
| | | DC and Switching Characteristics | General update. |
| | | Pinout Information | Updated Signal Descriptions section. Revised the descriptions of the following signals:<br>• P[L/R] [Group Number]_[A/B/C/D]<br>• P[T/B][Group Number]_[A/B]<br>• D4/IO4 (Previously named D4/MOSI2/IO4)<br>• D5/IO5 (Previously named D5/MISO/IO5)<br>• VCCHRX_D[dual_num]CH[chan_num]<br>• VCCHTX_D[dual_num]CH[chan_num] |
| | | Supplemental Information | Added TN1184 reference. |

© 2014-2018 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com