Lattice Semiconductor Corporation - LFE5U-85F-6BG554I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	259
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-85f-6bg554i

  - Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 18/15 I, II
  - HSUL12
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
  - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
  - Shared bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
  - Soft Error Detect – Embedded hard macro
  - Soft Error Correction – Without stopping user operation
  - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - On-chip oscillator for initialization and general use
  - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U-12	LFE5U-25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels / IO Count)							
256 caBGA (14 x 14 mm², 0.8 mm)	—	—	—	0/197	0/197	0/197	—
285 csfBGA (10 x 10 mm², 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm², 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm², 0.8 mm)	—	4/245	4/259	—	—	0/245	0/259
756 caBGA (27 x 27 mm², 0.8 mm)	—	—	4/365	—	—	—	0/365

Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.

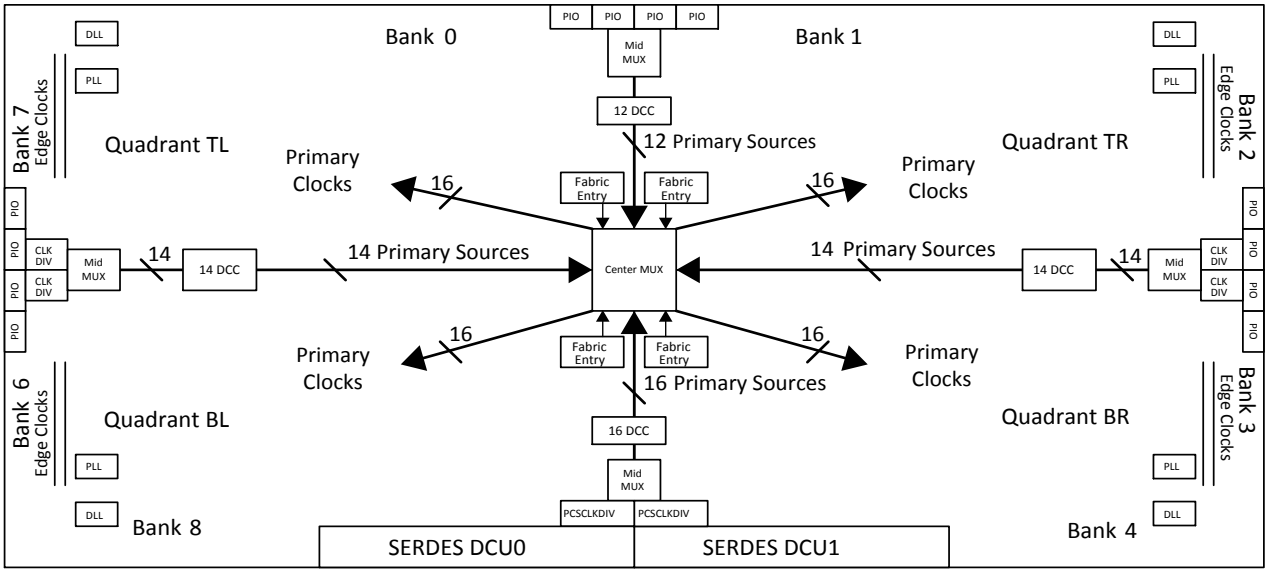


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

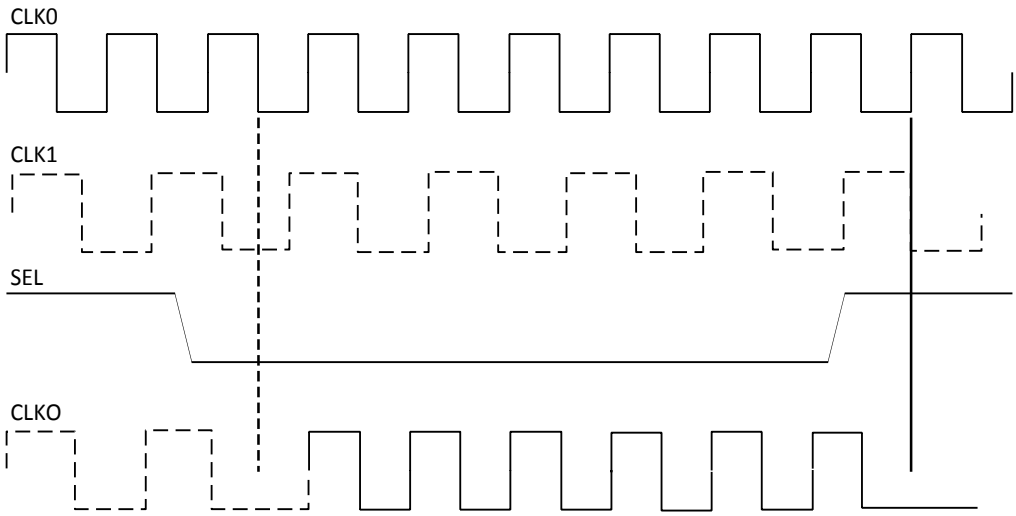


Figure 2.7. DCS Waveforms

2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

- 5*5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5/ ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.

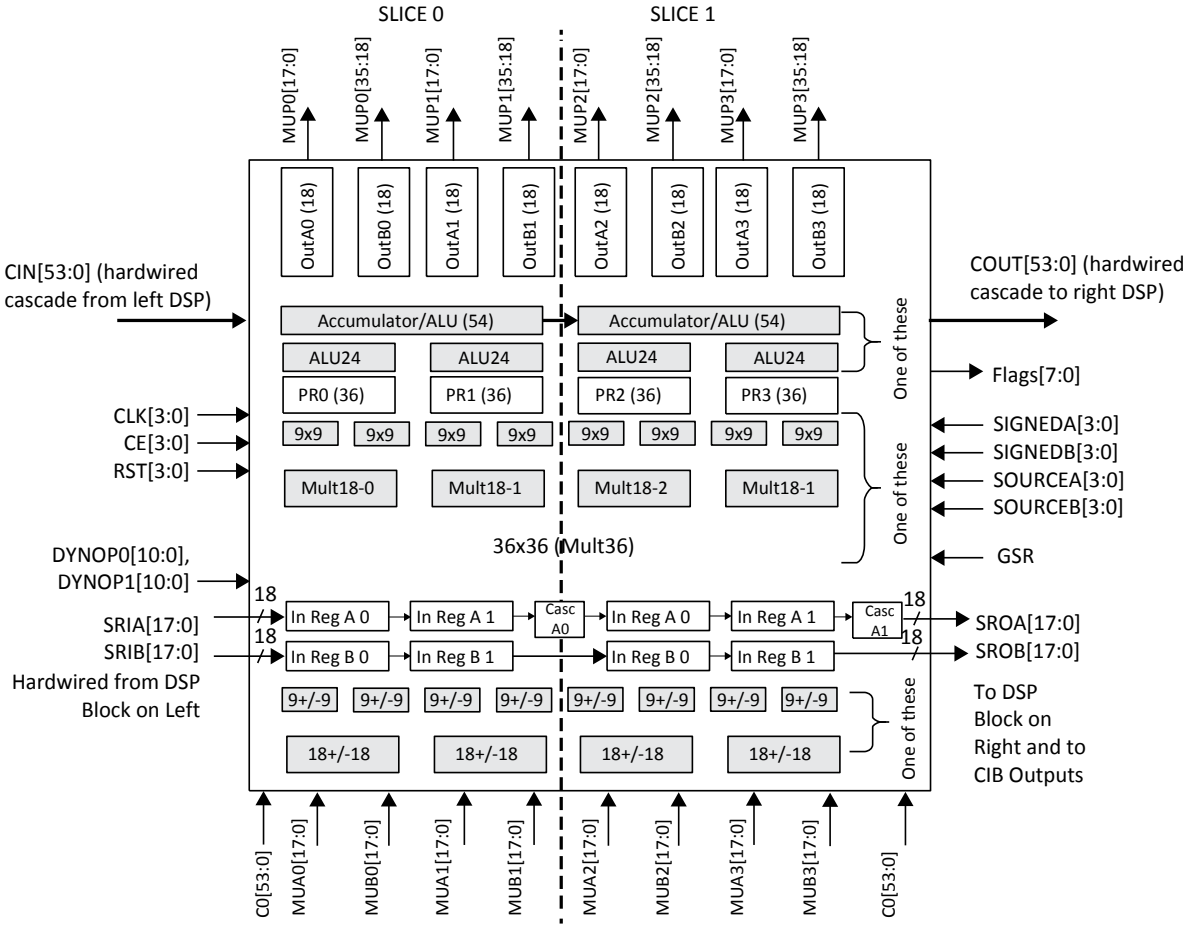


Figure 2.14. Simplified sysDSP Slice Block Diagram

In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note**: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

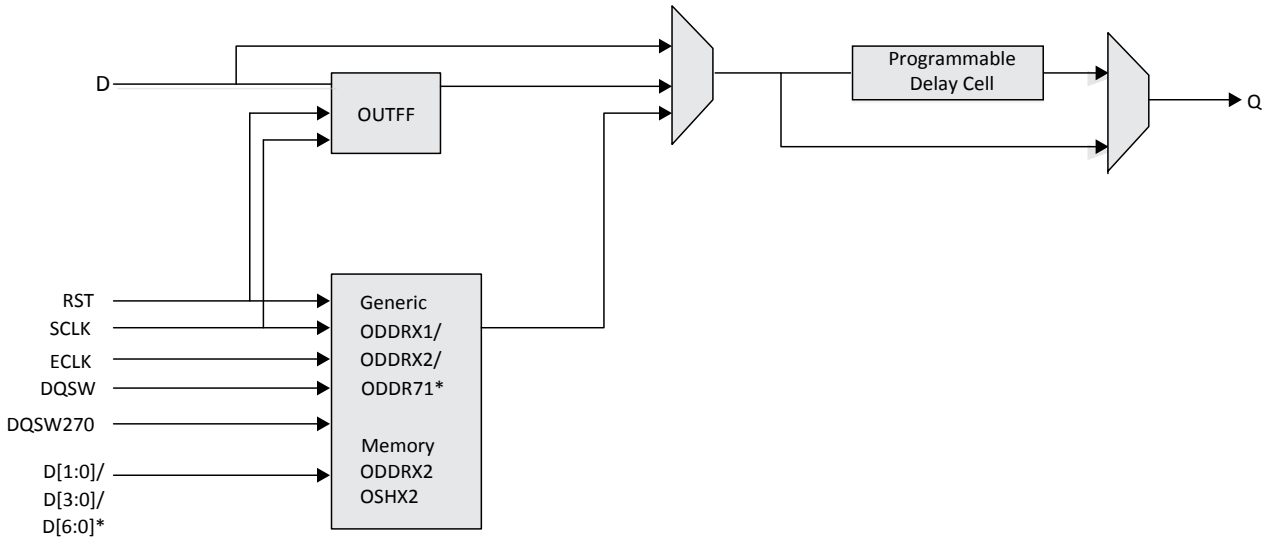
- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

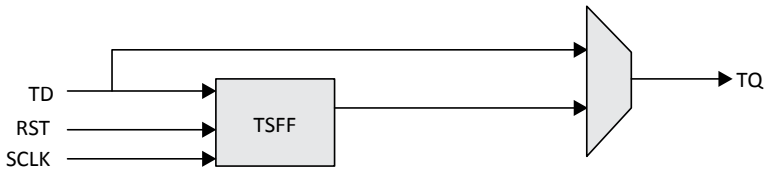


Figure 2.21. Tristate Register Block on Top Side

2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2.15 lists the allowable combination of primary and secondary protocol combinations.

2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

Table 2.15 lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter			Min	Typ	Max	Unit
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC}, and V_{CCAUX}	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIOs} do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC}, V_{CCAUX}, and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash.

For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA}, before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \le V_{IN} \le V_{IH}$ (Max)	—	—	±1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \le V_{IN} < V_{CCIO}$	—	—	±1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5$ V	—	18	—	mA

Notes:

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ±1 mA.

3.10. Supply Current (Standby)

Over recommended operating conditions.

Table 3.8. ECP5/ECP5-5G Supply Current (Standby)

Symbol	Parameter	Device	Typical	Unit
I_{CC}	Core Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F	77	mA
		LFE5UM5G-25F	77	mA
		LFE5U-45F/ LFE5UM-45F	116	mA
		LFE5UM5G-45F	116	mA
		LFE5U-85F/ LFE5UM-85F	212	mA
		LFE5UM5G-85F	212	mA
I_{CCAUX}	Auxiliary Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	16	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	17	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	26	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	0.5	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	0.5	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	0.5	mA
I_{CCA}	SERDES Power Supply Current (Per Dual)	LFE5UM-25F	11	mA
		LFE5UM5G-25F	12	mA
		LFE5UM-45F	9.5	mA
		LFE5UM5G-45F	11	mA
		LFE5UM-85F	9.5	mA
		LFE5UM5G-85F	11	mA

Notes:

- For further information on supply current, see the list of technical documentation in Supplemental Information section on page 102.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 Hz.
- Pattern represents a “blank” configuration data file.
- T_J = 85 °C, power supplies at nominal voltage.
- To determine the ECP5/ECP5-5G peak start-up current, use the Power Calculator tool in the Lattice Diamond Design Software.

3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3, 5]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

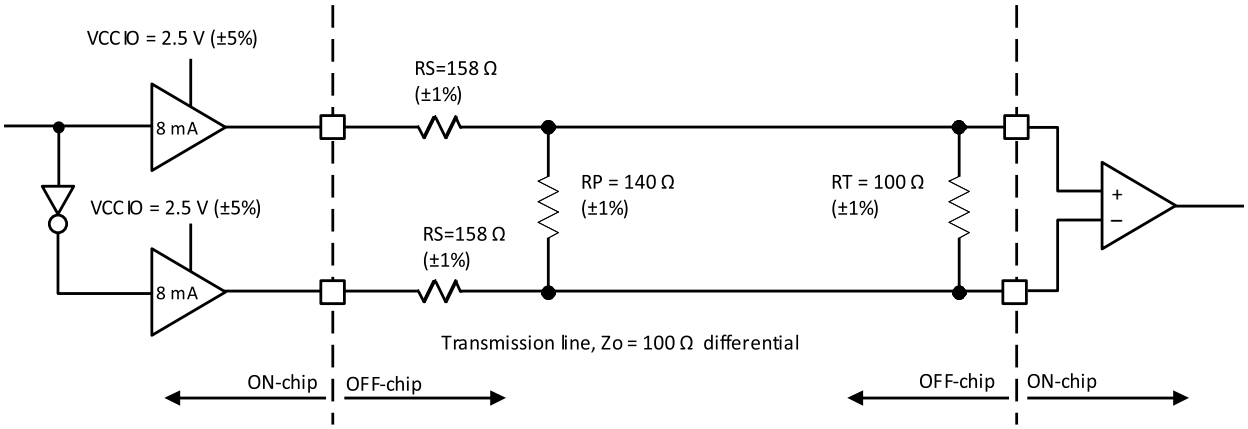


Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (±1%)	158	Ω
R_P	Driver Parallel Resistor (±1%)	140	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
Generic DDR Input									
Generic DDRX1 Inputs With Clock and Data Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{SU\_GDDRX1\_centered}$	Data Setup Before CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$t_{HD\_GDDRX1\_centered}$	Data Hold After CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs With Clock and Data Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.7									
$t_{SU\_GDDRX1\_aligned}$	Data Setup from CLK Input	All Devices	—	–0.55	—	–0.55	—	–0.55	ns + 1/2 UI
$t_{HD\_GDDRX1\_aligned}$	Data Hold from CLK Input	All Devices	0.55	—	0.55	—	0.55	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Inputs With Clock and Data Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.6									
$t_{SU\_GDDRX2\_centered}$	Data Setup before CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$t_{HD\_GDDRX2\_centered}$	Data Hold after CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Inputs With Clock and Data Aligned at Pin (GDDRX2_RX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.7									
$t_{SU\_GDDRX2\_aligned}$	Data Setup from CLK Input	All Devices	—	–0.344	—	–0.42	—	-0.495	ns + 1/2 UI
$t_{HD\_GDDRX2\_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	—	0.495	—	ns + 1/2 UI
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Inputs With Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) Using PLL Clock Input, Left and Right sides Only Figure 3.11									
$t_{SU\_LVDS71\_i}$	Data Setup from CLK Input (bit i)	All Devices	—	–0.271	—	–0.39	—	–0.41	ns+(1/2+i) * UI
$t_{HD\_LVDS71\_i}$	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	—	0.41	—	ns+(1/2+i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz

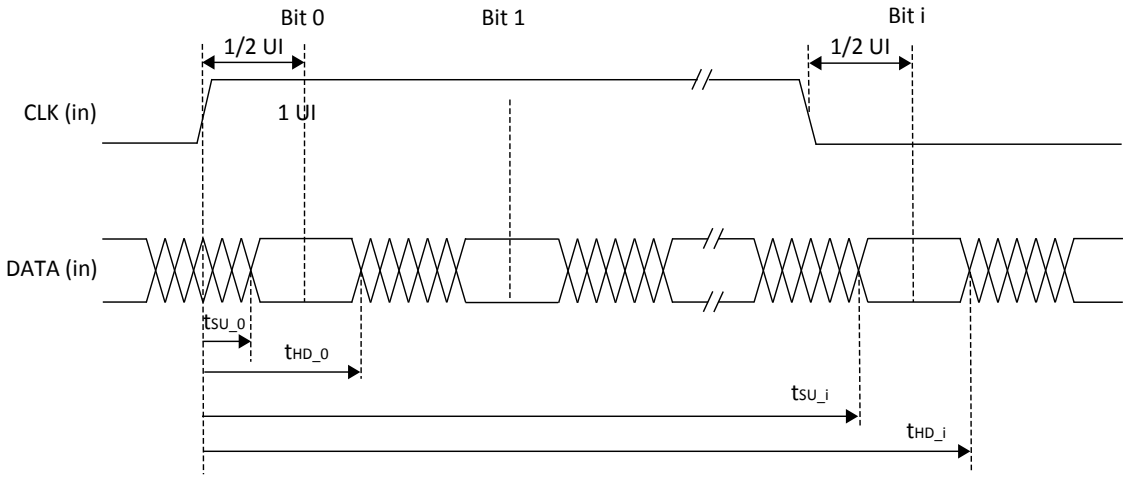


Figure 3.11. Receiver DDRX71_RX Waveforms

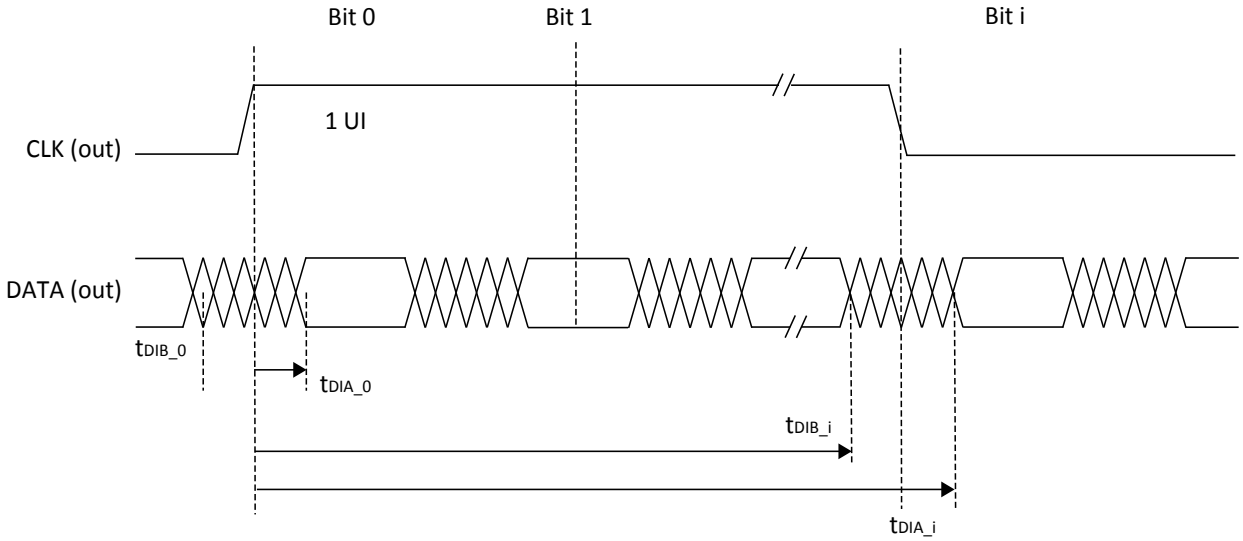


Figure 3.12. Transmitter DDRX71_TX Waveforms

Table 3.31. PCIe (5 Gb/s) *(Continued)*

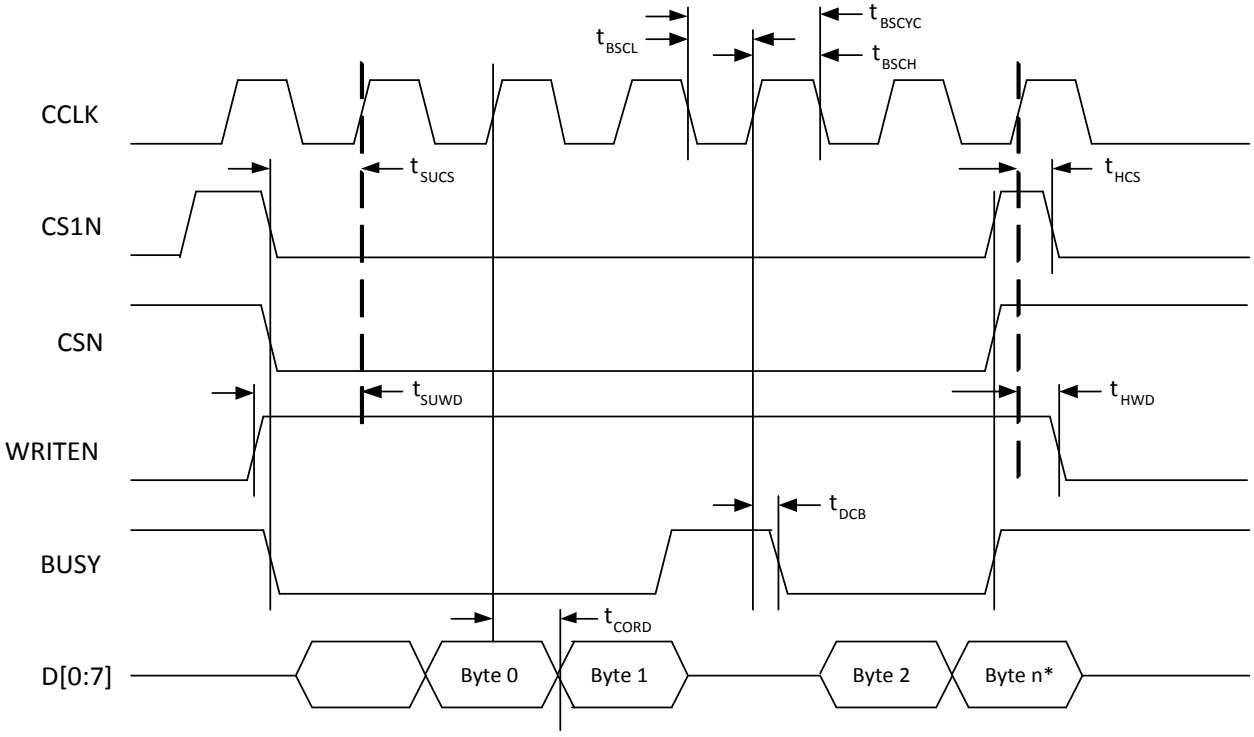
Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Receive[1, 2]						
UI	Unit Interval	—	199.94	200	200.06	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	0.34[3]	—	1.2	V, p-p
$T_{RX-RJ-RMS}$	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	—	—	4.2	ps, RMS
T_{RX-DJ}	Receiver deterministic jitter tolerance	—	—	—	88	ps
$V_{RX-CM-AC}$	Common mode noise from Rx	—	—	—		mV, p-p
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z_{RX-DC}	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Receiver DC single ended impedance when powered down	—	200K	—	—	Ω
$V_{RX-CM-AC-P}$	Rx AC peak common mode voltage	—	—	—		mV, peak
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect Threshold	—	65	—	340[3]	mv,
$L_{RX-SKEW}$	Receiver lane-lane skew	—	—	—	8	ns

Notes:

1. Values are measured at 5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express standard.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications *(Continued)*

Symbol	Parameter		Min	Max	Unit
Slave Parallel					
f_{CCLK}	CCLK input clock frequency	—	—	50	MHz
t_{BSCH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{BSCL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{CORD}	CCLK to DOUT for Read Data	—	—	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	—	1.5	—	ns
t_{HCBDI}	Data Hold Time to CCLK	—	1.5	—	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK	—	45	—	ns
t_{HCWD}	WRITEN Hold Time to CCLK	—	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	—	12	ns



*n = last byte of read cycle.

Figure 3.15. sysCONFIG Parallel Port Read Cycle

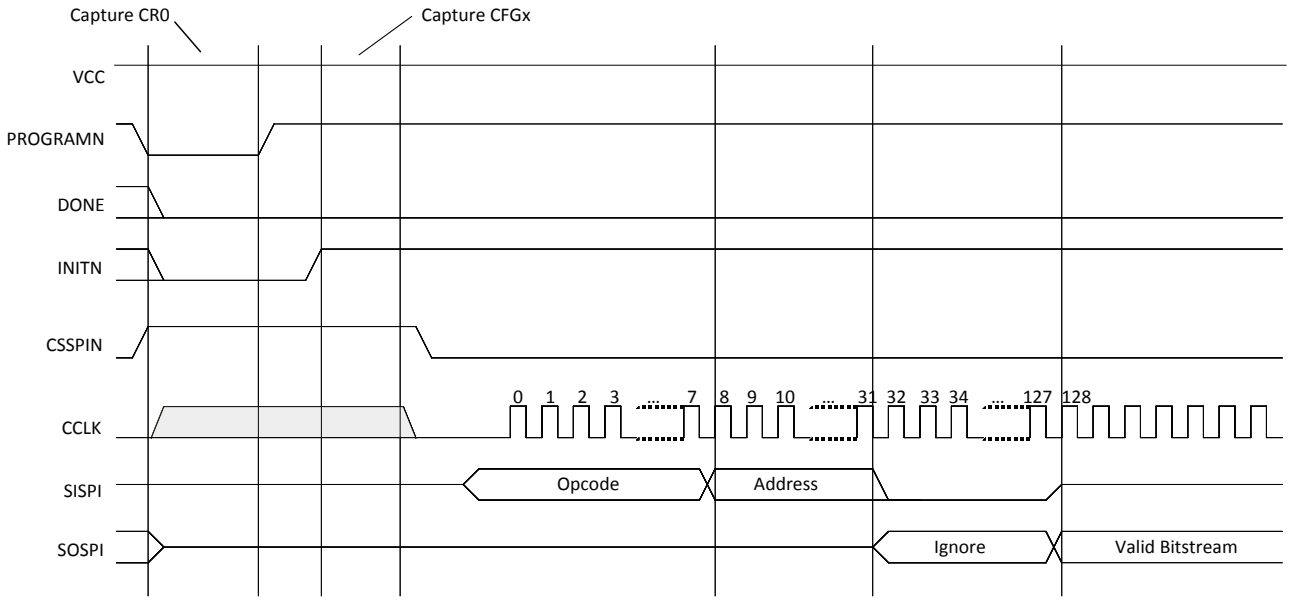


Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Pin Information Summary		LFE5UM/ LFE5UM5G-25		LFE5UM/LFE5UM5G-45			LFE5UM/LFE5UM5G-85			
Pin Type		285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA
TAP		4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated Pins		7	7	7	7	7	7	7	7	7
GND		83	59	83	59	113	83	59	113	166
NC		1	8	1	2	33	1	0	17	29
Reserved		0	2	0	2	4	0	2	4	4
SERDES		14	28	14	28	28	14	28	28	28
VCCA (SERDES)	VCCA0	2	2	2	2	6	2	2	6	8
	VCCA1	0	2	0	2	6	0	2	6	9
VCCAUX (SERDES)	VCCAUXA0	2	2	2	2	2	2	2	2	2
	VCCAUXA1	0	2	0	2	2	0	2	2	2
GNDA (SERDES)		26	26	26	26	49	26	26	49	60
Total Balls		285	381	285	381	554	285	381	554	756
High Speed Differential Input / Output Pairs	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	10/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8	24/12
	Bank 3	14/7	16/8	14/7	16/8	24/12	14/7	16/8	24/12	32/16
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	13/6	16/8	13/6	16/8	24/12	13/6	16/8	24/12	32/16
	Bank 7	8/6	16/8	8/6	16/8	16/8	8/6	16/8	16/8	24/12
	Bank 8	0	0	0	0	0	0	0	0	0
Total High Speed Differential I/O Pairs		45/2	64/32	45/27	64/3	80/40	45/27	65/3	80/40	112/5
DQS Groups (> 11 pins in group)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	1	2	1	2	2	1	2	2	3
	Bank 3	2	2	2	2	3	2	2	3	4
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	2	2	2	2	3	2	2	3	4
	Bank 7	1	2	1	2	2	1	2	2	3
	Bank 8	0	0	0	0	0	0	0	0	0
Total DQS Groups		6	8	6	8	10	6	8	10	14

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	No
LFE5U-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	No
LFE5UM-25F-6MG285C	–6	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-7MG285C	–7	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-6BG381C	–6	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-7BG381C	–7	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-45F-6MG285C	–6	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-7MG285C	–7	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-6BG381C	–6	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-7BG381C	–7	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-6BG554C	–6	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-7BG554C	–7	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes
LFE5UM5G-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM5G-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM5G-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM5G-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM5G-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM5G-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes