Lattice Semiconductor Corporation - LFE5U-85F-6MG285I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-85f-6mg285i

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Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.

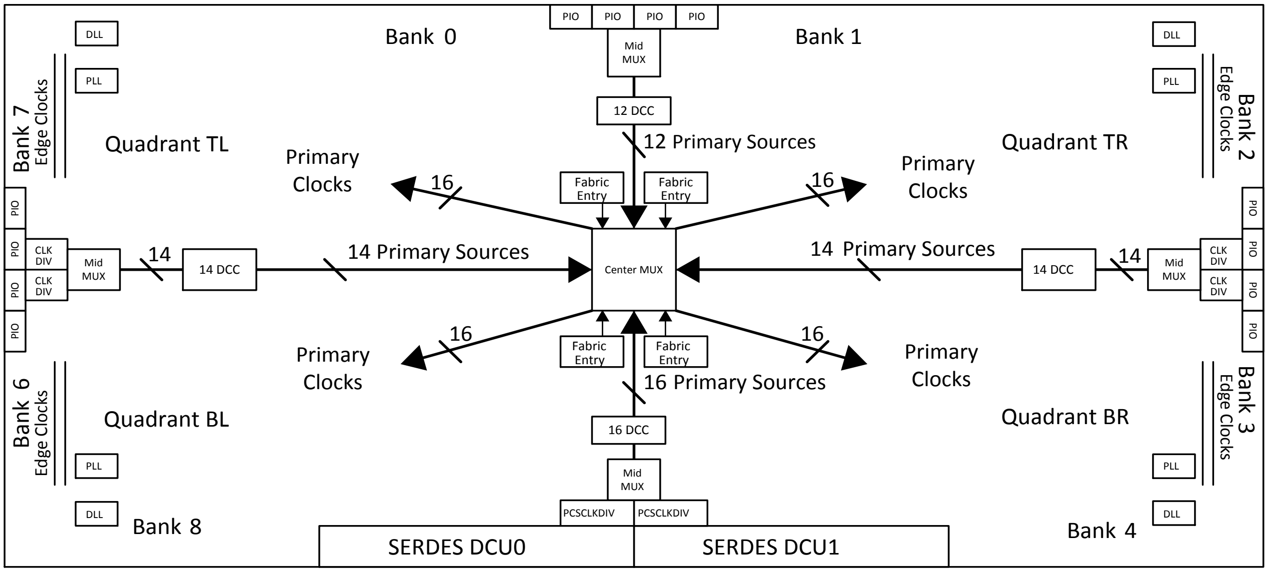


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

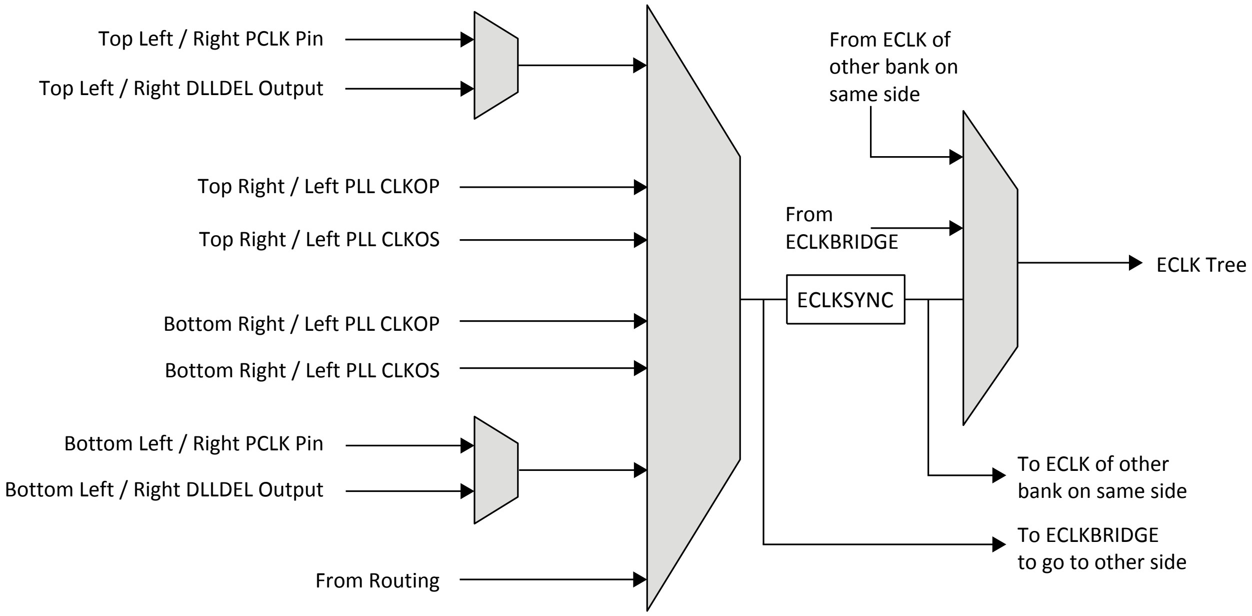


Figure 2.8. Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.6. Clock Dividers

ECP5/ECP5-5G devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷3.5 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal.

The clock dividers can be fed from selected PLL outputs, external primary clock pins multiplexed with the DDRDEL Slave Delay or from routing. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The SLIP signal slips the outputs one cycle relative to the input clock. For further information on clock dividers, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263). Figure 2.9 shows the clock divider connections.

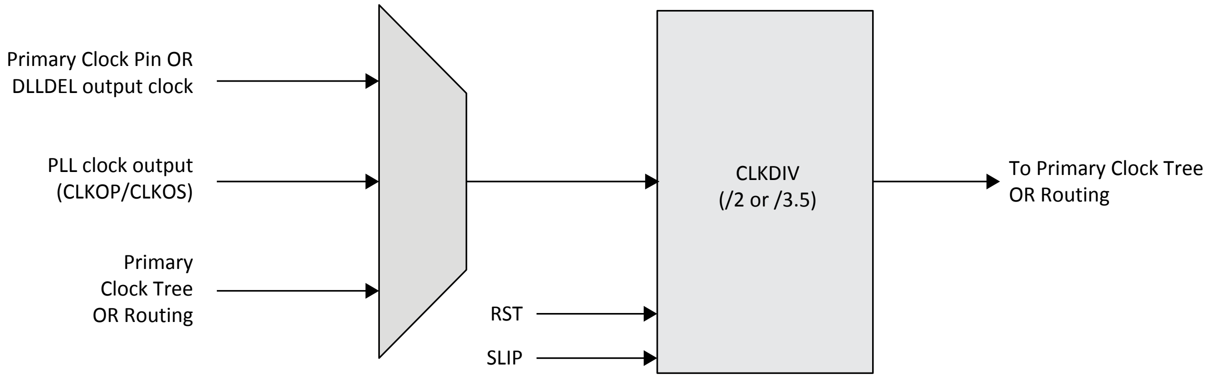


Figure 2.9. ECP5/ECP5-5G Clock Divider Sources

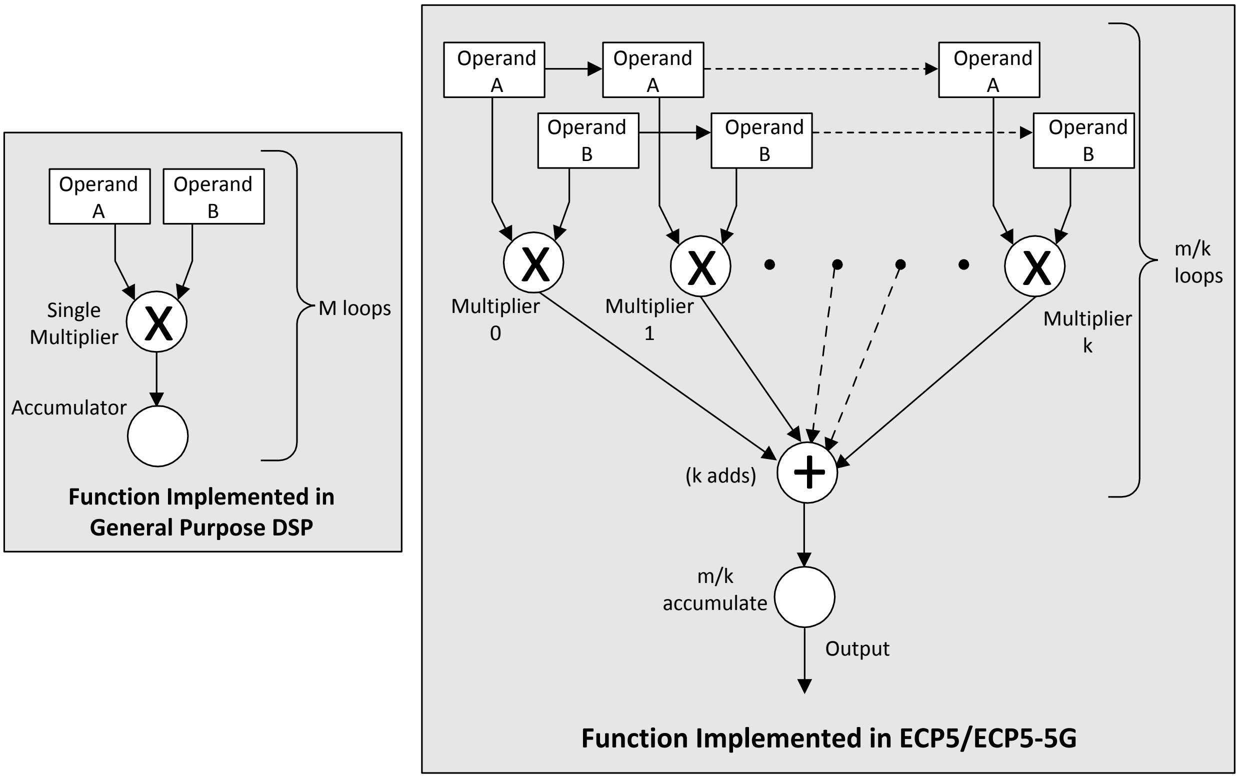


Figure 2.13. Comparison of General DSP and ECP5/ECP5-5G Approaches

2.9.2. sysDSP Slice Architecture Features

The ECP5/ECP5-5G sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The ECP5/ECP5-5G sysDSP Slice supports many functions that include the following:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
  - Two dimensional (2D) symmetry mode – supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture
- Fully cascadable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)
- Multiply (36x36 by cascading across two sysDSP slices)
- Multiply Accumulate (supports one 18x36 multiplier result accumulation or two 18x18 multiplier result accumulation)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
  - 3*3 and 3*5 – Internal DSP Slice support

In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note**: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

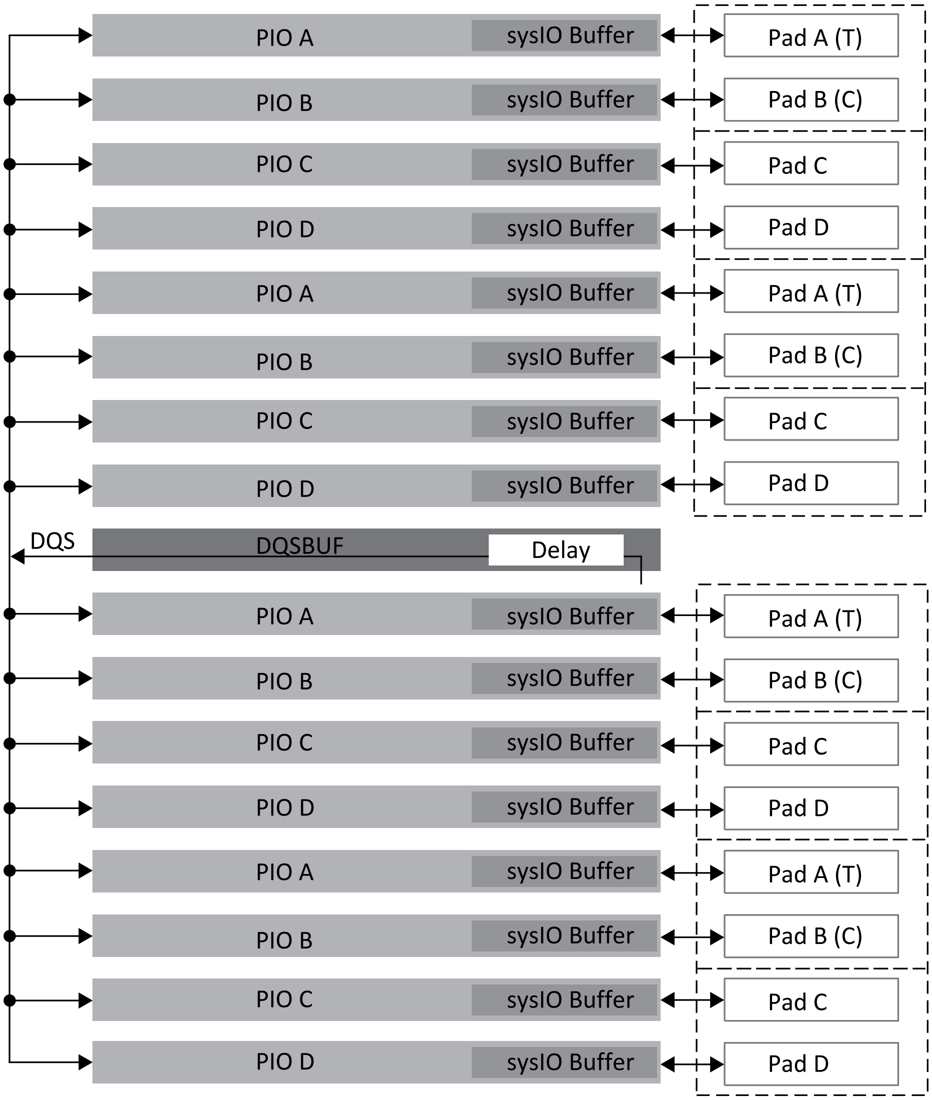


Figure 2.23. DQS Grouping on the Left and Right Edges

2.13.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR2/3, LPDDR2/3), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifted is achieved by using DQSDEL programmable delay line in the DQS Delay Block (DQS read circuit). The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block shown in Figure 2.24 generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

- Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

  Bank 4 I/O only exists in the LFE5-85 device.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Diamond tool.

- Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.5	1.32	V
V_{CCA}	Supply Voltage	–0.5	1.32	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	–0.5	2.75	V
V_{CCIO}	Supply Voltage	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CCHRX}, V_{CCHTX}	SERDES RX/TX Buffer Supply Voltages	–0.5	1.32	V
—	Voltage Applied on SERDES Pins	–0.5	1.80	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
$V_{CC}{}^{2}$	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
$V_{CCAUX}{}^{2,4}$	Auxiliary Supply Voltage	—	2.375	2.625	V
$V_{CCIO}{}^{2,3}$	I/O Driver Supply Voltage	—	1.14	3.465	V
$V_{REF}{}^{1}$	Input Reference Voltage	—	0.5	1.0	V
t_{JCOM}	Junction Temperature, Commercial Operation	—	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	—	–40	100	°C
SERDES External Power Supply[5]					
V_{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V_{CCAUXA}	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
$V_{CCHRX}{}^{6}$	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V_{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 on page 48.
4. V_{CCAUX} ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
5. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter			Min	Typ	Max	Unit
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC}, and V_{CCAUX}	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIOs} do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC}, V_{CCAUX}, and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash.

For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA}, before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \le V_{IN} \le V_{IH}$ (Max)	—	—	±1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \le V_{IN} < V_{CCIO}$	—	—	±1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5$ V	—	18	—	mA

Notes:

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ±1 mA.

3.11. SERDES Power Supply Requirements[1,2,3]

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
$I_{CCA\text{-}SB}$	V_{CCA} Power Supply Current (Per Channel)	4	9.5	mA
$I_{CCHRX\text{-}SB}$[4]	V_{CCHRX}, Input Buffer Current (Per Channel)	—	0.1	mA
$I_{CCHTX\text{-}SB}$	V_{CCHTX}, Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 3.125 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	43	54	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	40	50	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	34	43	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	28	38	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For $I_{CCHRX\text{-}SB}$, during Standby, input termination on Rx are disabled.
5. For $I_{CCHRX\text{-}OP}$, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

Table 3.10. ECP5-5G

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
$I_{CCA\text{-}SB}$	V_{CCA} Power Supply Current (Per Channel)	4	9.5	mA
$I_{CCHRX\text{-}SB}$[4]	V_{CCHRX}, Input Buffer Current (Per Channel)	—	0.1	mA
$I_{CCHTX\text{-}SB}$	V_{CCHTX}, Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 5 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	58	67	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 3.2 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	48	57	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	44	53	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	36	46	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	30	40	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For $I_{CCHRX\text{-}SB}$, during Standby, input termination on Rx are disabled.
5. For $I_{CCHRX\text{-}OP}$, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

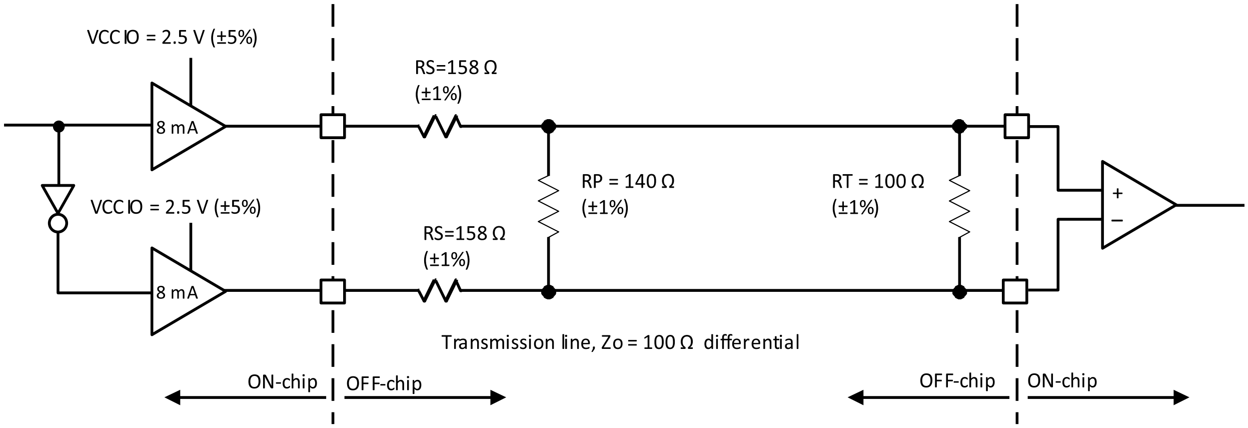


Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (±1%)	158	Ω
R_P	Driver Parallel Resistor (±1%)	140	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.24. SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3.29 specifies reference clock requirements, over the full range of operating conditions.

Table 3.29. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min	Typ	Max	Unit
F_{REF}	Frequency range	50	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2, 4]	200	—	V_{CCAUXA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCAUXA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	$V_{CCAUXA} + 0.4$	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–30%	100/HiZ	+30%	Ω
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

Notes:

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
3. Measured at 50% amplitude.
4. Single-ended clocking is achieved by applying a reference voltage V_{REF} on REFCLKN input, with the clock applied to REFCLKP input pin. V_{REF} should be set to mid-point of the REFCLKP voltage swing.

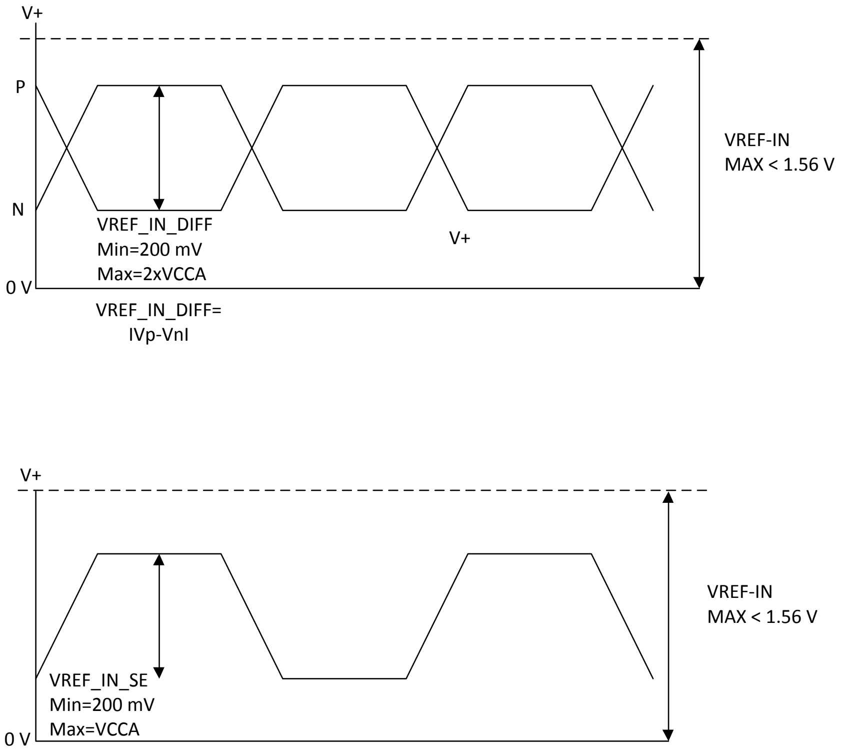


Figure 3.14. SERDES External Reference Clock Waveforms

3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

Table 3.31. PCIe (5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit[1]						
UI	Unit Interval	—	199.94	200	200.06	ps
$B_{WTX-PKG-PLL2}$	Tx PLL bandwidth corresponding to PKGTX-PLL2	—	5	—	16	MHz
$P_{KGTX-PLL2}$	Tx PLL Peaking	—	—	—	1	dB
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width	—		—	—	UI
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—		—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T_{TX-DJ}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T_{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
$T_{RF-MISMATCH}$	Tx rise/fall time mismatch	—	—	—		UI
$R_{LTX-DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX-CM-AC-PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—		mV, p-p
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Output peak voltage	—	—	—		mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—		ps

3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.39. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDO}	Serial data rate	—	270	—	2975	Mb/s
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	270 Mb/s[6]	—	—	0.2	UI
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	1485 Mb/s	—	—	0.2	UI
$T_{JALIGNMENT}$[1, 2]	Serial output jitter, alignment	2970 Mb/s	—	—	0.3	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mb/s[6]	—	—	0.2	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mb/s	—	—	1	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mb/s	—	—	2	UI

Notes:

1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice SERDES device configured to 50 Ω output impedance connecting to the external cable driver with differential signaling.
4. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mb/s.
5. All LFE5UM/LFE5UM5G devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.
6. 270 Mb/s is supported with Rate Divider only.

Table 3.40. Receive

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDI}	Serial input data rate	—	270	—	2970	Mb/s

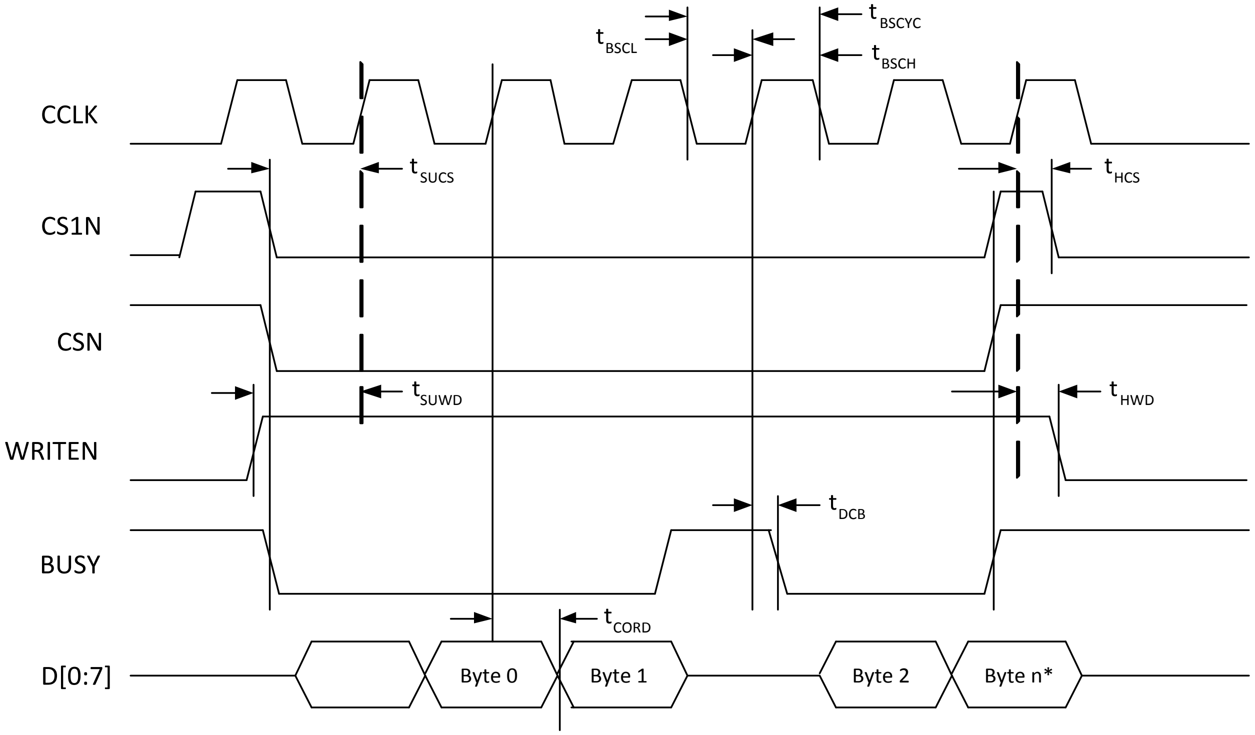
Table 3.41. Reference Clock

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F_{VCLK}	Video output clock frequency	—	54	—	148.5	MHz
DC_V	Duty cycle, video clock	—	45	50	55	%

Note: SD-SDI (270 Mb/s) is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications *(Continued)*

Symbol	Parameter		Min	Max	Unit
Slave Parallel					
f_{CCLK}	CCLK input clock frequency	—	—	50	MHz
t_{BSCH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{BSCL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{CORD}	CCLK to DOUT for Read Data	—	—	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	—	1.5	—	ns
t_{HCBDI}	Data Hold Time to CCLK	—	1.5	—	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK	—	45	—	ns
t_{HCWD}	WRITEN Hold Time to CCLK	—	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	—	12	ns



*n = last byte of read cycle.

Figure 3.15. sysCONFIG Parallel Port Read Cycle

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	No
LFE5U-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	No
LFE5UM-25F-6MG285C	–6	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-7MG285C	–7	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-6BG381C	–6	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-7BG381C	–7	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-45F-6MG285C	–6	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-7MG285C	–7	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-6BG381C	–6	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-7BG381C	–7	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-6BG554C	–6	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-7BG554C	–7	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes
LFE5UM5G-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM5G-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM5G-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM5G-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM5G-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM5G-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section. • Deleted Serial RapidIO protocol under Embedded SERDES. • Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3. Mentioned transmit de-emphasis “pre- and post-cursors”.
		Architecture	Updated Overview section. • Revised description of PFU blocks. • Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section. • Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. • Deleted Serial RapidIO protocol. • Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section. • Deleted “130 MHz ±15% CMOS” oscillator. • Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA}.
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to t_{SKEW_PR} V_{CCA} and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.

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