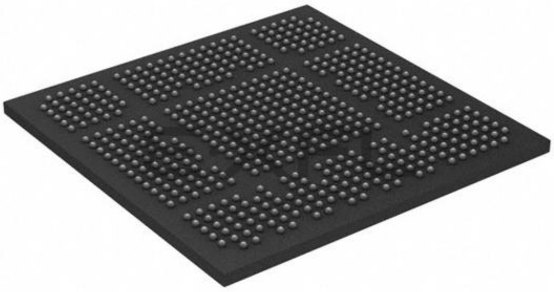

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	259
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-85f-7bg554i

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay-Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLL	Phase-Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SERDES	Serializer/Deserializer
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing

1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 84K LUTs
  - 197 to 365 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 3.744 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs

    - Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
    - DDR registers in I/O cells
    - Dedicated read/write levelling functionality
    - Dedicated gearing logic
    - Source synchronous standards support
        - ADC/DAC, 7:1 LVDS, XGMII
        - High Speed ADC/DAC devices
    - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
    - On-chip termination
    - LVTTL and LVCMOS 33/25/18/15/12
    - SSTL 18/15 I, II
    - HSUL12
    - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
    - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
    - Shared bank for configuration I/Os
    - SPI boot flash interface
    - Dual-boot images supported
    - Slave SPI
    - TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
    - Soft Error Detect – Embedded hard macro
    - Soft Error Correction – Without stopping user operation
    - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
    - IEEE 1149.1 and IEEE 1532 compliant
    - Reveal Logic Analyzer
    - On-chip oscillator for initialization and general use
    - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U-12	LFE5U-25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels / IO Count)							
256 caBGA (14 x 14 mm², 0.8 mm)	—	—	—	0/197	0/197	0/197	—
285 csfBGA (10 x 10 mm², 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm², 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm², 0.8 mm)	—	4/245	4/259	—	—	0/245	0/259
756 caBGA (27 x 27 mm², 0.8 mm)	—	—	4/365	—	—	—	0/365

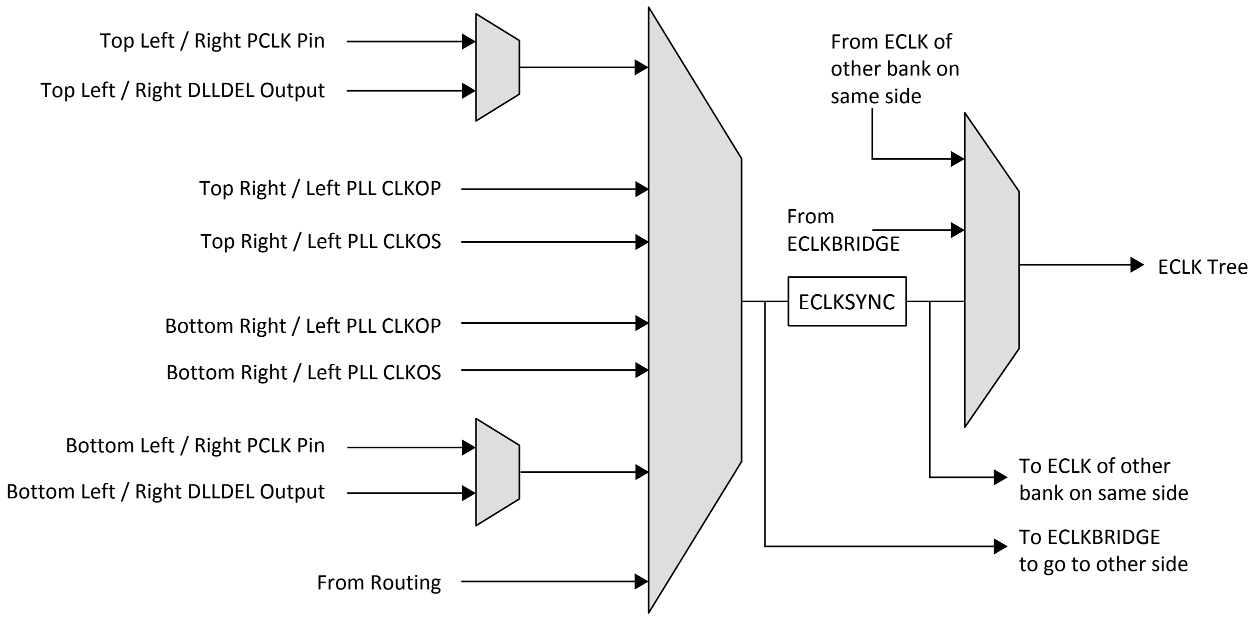


Figure 2.8. Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.6. Clock Dividers

ECP5/ECP5-5G devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷3.5 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal.

The clock dividers can be fed from selected PLL outputs, external primary clock pins multiplexed with the DDRDEL Slave Delay or from routing. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The SLIP signal slips the outputs one cycle relative to the input clock. For further information on clock dividers, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263). Figure 2.9 shows the clock divider connections.

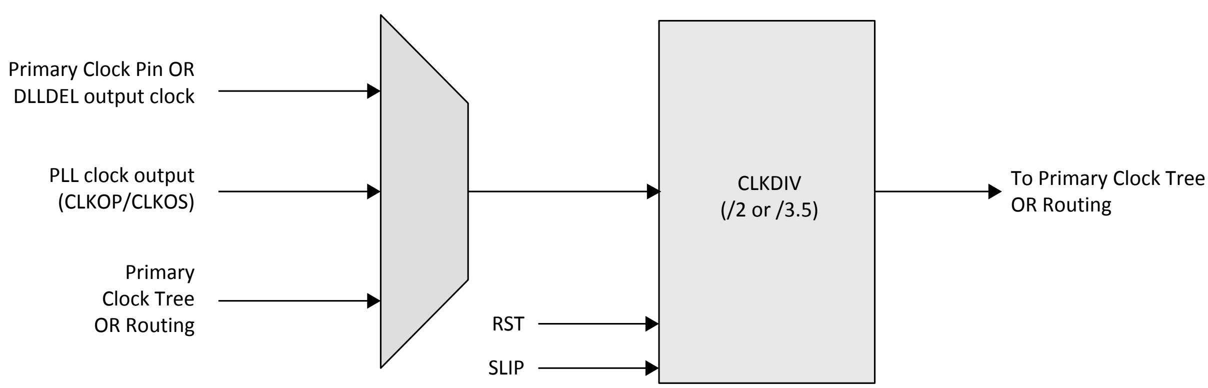


Figure 2.9. ECP5/ECP5-5G Clock Divider Sources

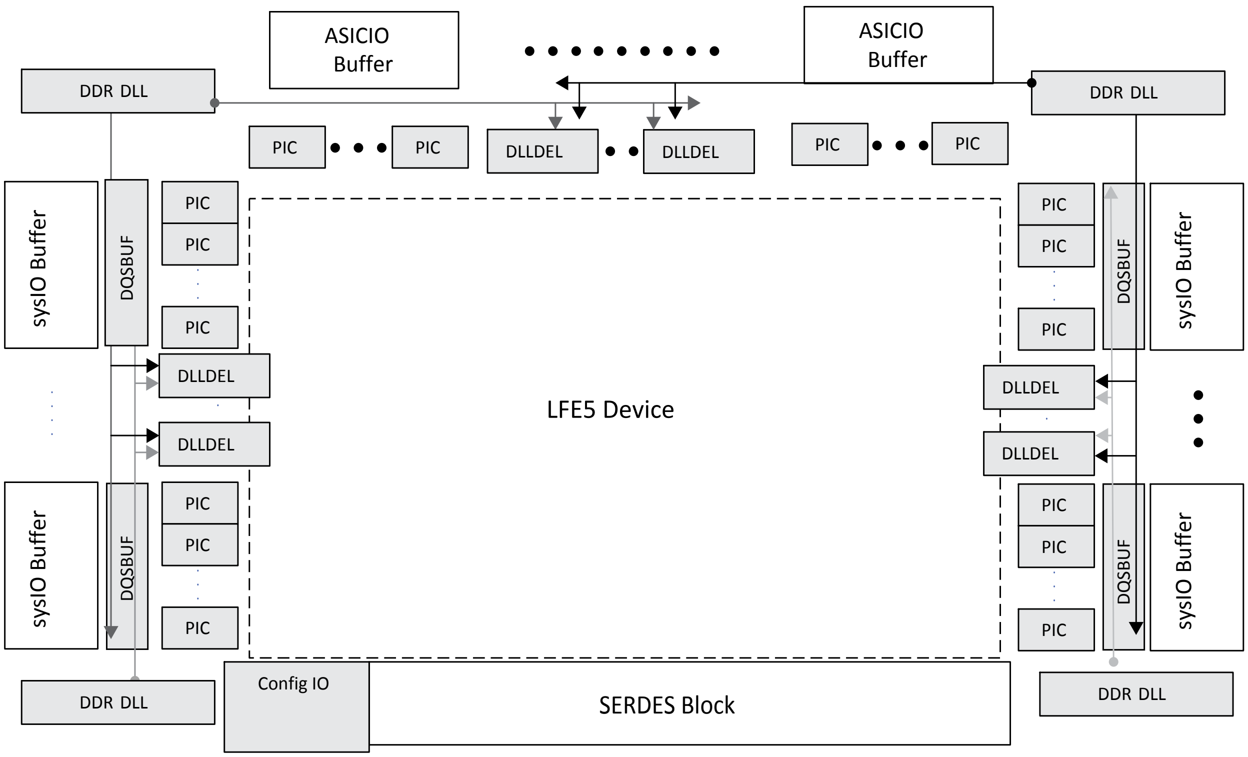


Figure 2.11. ECP5/ECP5-5G DLL Top Level View (For LFE-45 and LFE-85)

2.8. sysMEM Memory

ECP5/ECP5-5G devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

2.8.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.6 on page 25. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

- 5*5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5/ ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.

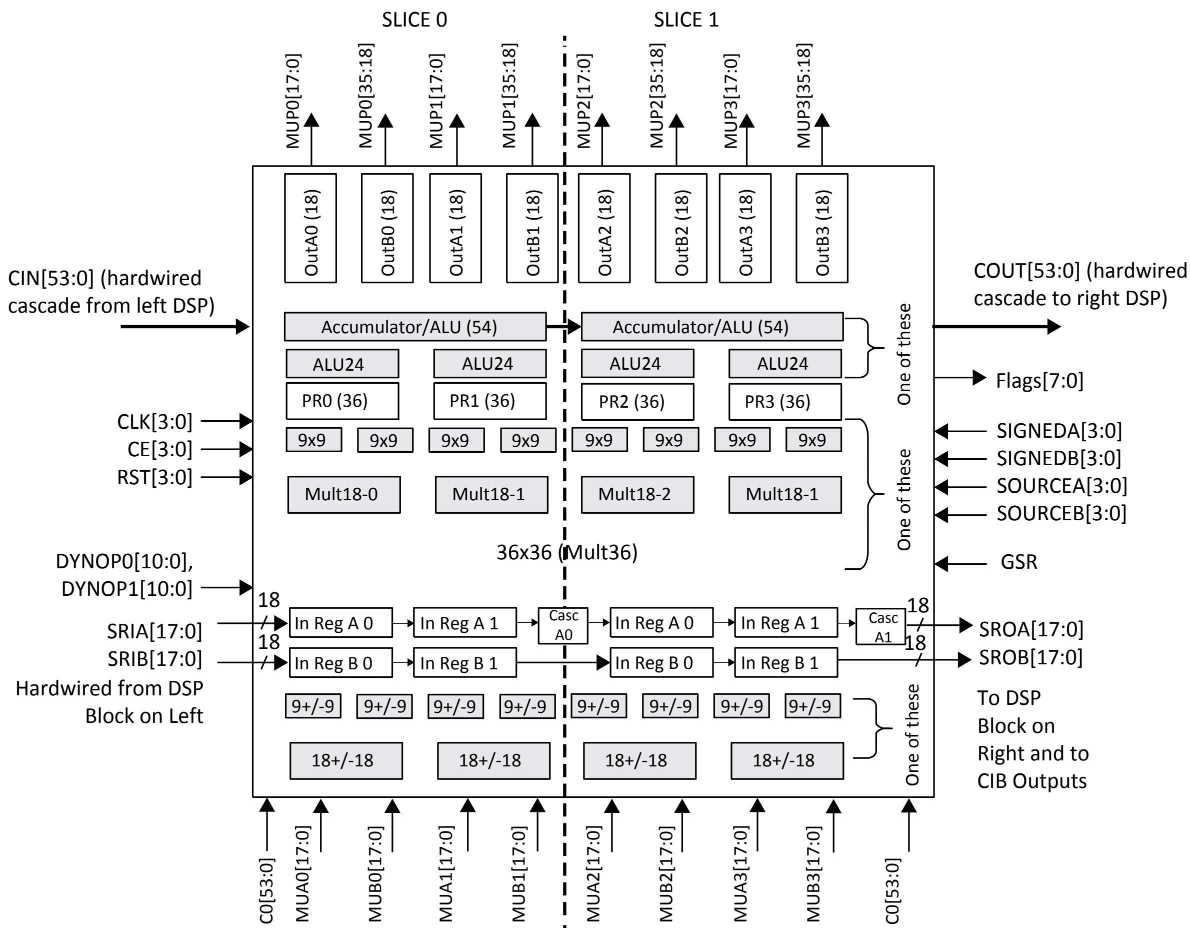


Figure 2.14. Simplified sysDSP Slice Block Diagram

2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2.15 lists the allowable combination of primary and secondary protocol combinations.

2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

Table 2.15 lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

3.14.5. BLVDS25

The ECP5/ECP5-5G devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

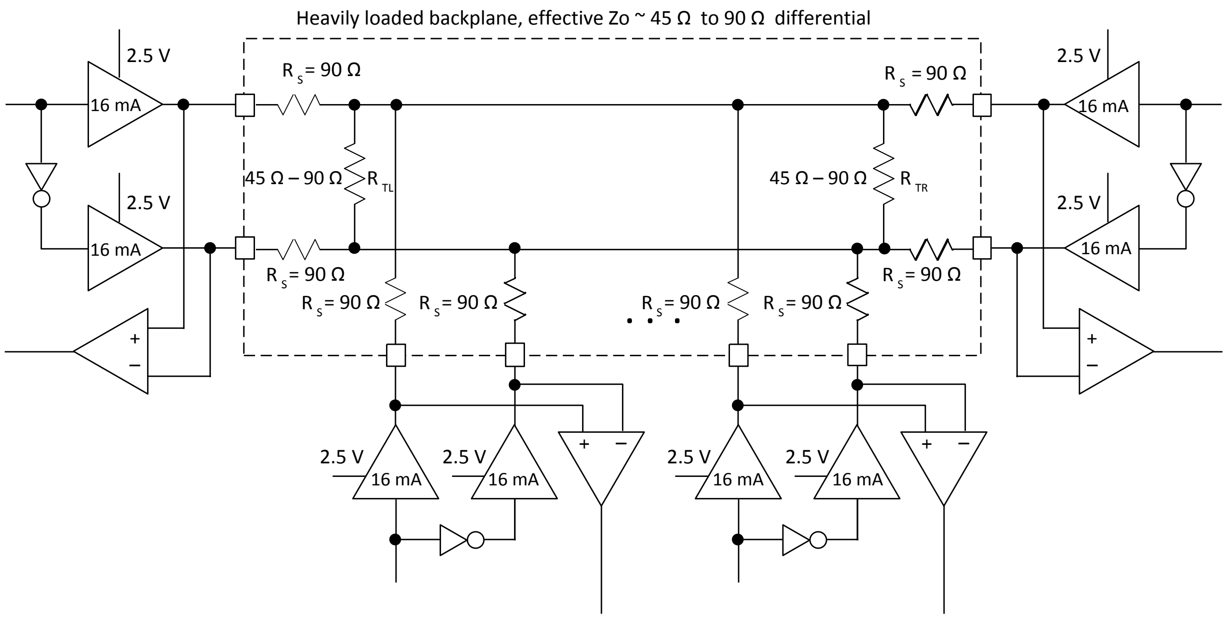


Figure 3.2. BLVDS25 Multi-point Output Example

Over recommended operating conditions.

Table 3.15. BLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo = 45 Ω	Zo = 90 Ω	
V_{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (±1%)	90.00	90.00	Ω
R_{TL}	Driver Parallel Resistor (±1%)	45.00	90.00	Ω
R_{TR}	Receiver Termination (±1%)	45.00	90.00	Ω
V_{OH}	Output High Voltage	1.38	1.48	V
V_{OL}	Output Low Voltage	1.12	1.02	V
V_{OD}	Output Differential Voltage	0.25	0.46	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	11.24	10.20	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

Table 3.20. Register-to-Register Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	441	MHz
32-Bit Decoder	441	MHz
64-Bit Decoder	332	MHz
4:1 Mux	441	MHz
8:1 Mux	441	MHz
16:1 Mux	441	MHz
32:1 Mux	441	MHz
8-Bit Adder	441	MHz
16-Bit Adder	441	MHz
64-Bit Adder	441	MHz
16-Bit Counter	384	MHz
32-Bit Counter	317	MHz
64-Bit Counter	263	MHz
64-Bit Accumulator	288	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	214	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	441	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	441	MHz
DSP Functions		
9 x 9 Multiplier (All Registers)	225	MHz
18 x 18 Multiplier (All Registers)	225	MHz
36 x 36 Multiplier (All Registers)	225	MHz
18 x 18 Multiply-Add/Sub (All Registers)	225	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	225	MHz

Notes:

1. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
Generic DDR Output									
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDRX1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{DVB\_GDDRX1\_centered}$	Data Output Valid before CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$t_{DVA\_GDDRX1\_centered}$	Data Output Valid after CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9									
$t_{DIB\_GDDRX1\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.3	—	–0.3	—	–0.3	—	ns
$t_{DIA\_GDDRX1\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.3	—	0.3	—	0.3	ns
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8									
$t_{DVB\_GDDRX2\_centered}$	Data Output Valid Before CLK Output	All Devices	–0.442	—	–0.56	—	–0.676	—	ns + 1/2 UI
$t_{DVA\_GDDRX2\_centered}$	Data Output Valid After CLK Output	All Devices	—	0.442	—	0.56	—	0.676	ns + 1/2 UI
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9									
$t_{DIB\_GDDRX2\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns
$t_{DIA\_GDDRX2\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDRX71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12									
$t_{DIB\_LVDS71\_i}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns + (i) * UI
$t_{DIA\_LVDS71\_i}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns + (i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz
Memory Interface									
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)									
t_{DVBDQ_DDR2} t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	–0.26	—	–0.317	—	–0.374	ns + 1/2 UI
t_{DVADQ_DDR2} t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.26	—	0.317	—	0.374	—	ns + 1/2 UI

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

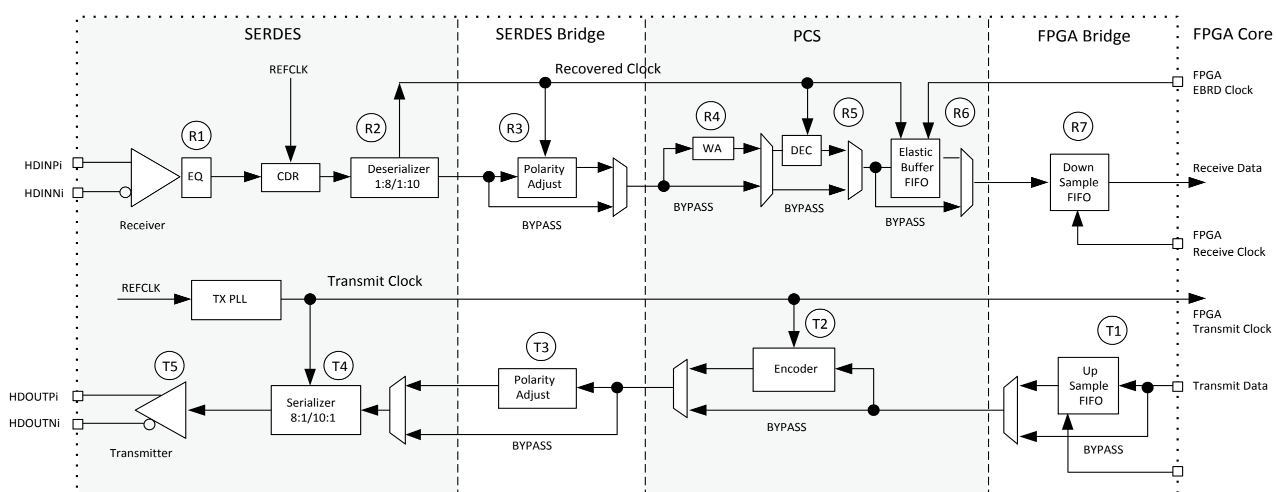


Figure 3.13. Transmitter and Receiver Latency Block Diagram

3.24. SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3.29 specifies reference clock requirements, over the full range of operating conditions.

Table 3.29. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min	Typ	Max	Unit
F_{REF}	Frequency range	50	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2, 4]	200	—	V_{CCAUXA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCAUXA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	$V_{CCAUXA} + 0.4$	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–30%	100/HiZ	+30%	Ω
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

Notes:

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
3. Measured at 50% amplitude.
4. Single-ended clocking is achieved by applying a reference voltage V_{REF} on REFCLKN input, with the clock applied to REFCLKP input pin. V_{REF} should be set to mid-point of the REFCLKP voltage swing.

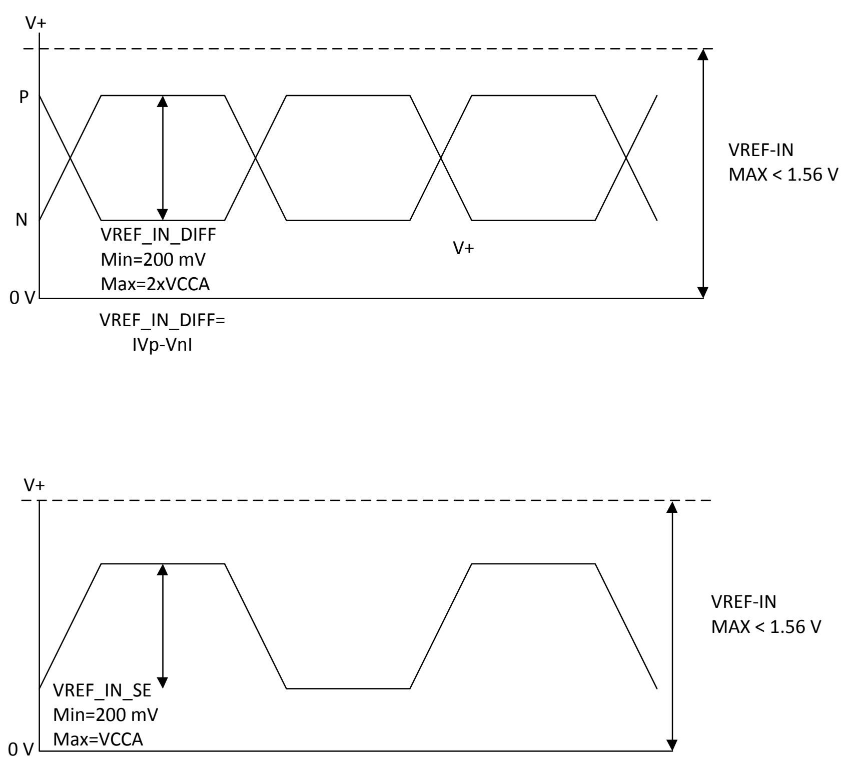


Figure 3.14. SERDES External Reference Clock Waveforms

3.27. XAUI/CPRI LV E.30 Electrical and Timing Characteristics

3.27.1. AC and DC Characteristics

Over recommended operating conditions.

Table 3.33. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	Ω
J_{TX_DDJ}[2, 3]	Output data deterministic jitter	—	—	—	0.17	UI
J_{TX_TJ}[1, 2, 3]	Total output data jitter	—	—	—	0.35	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Over recommended operating conditions.

Table 3.34. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J_{RX_DJ}[1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J_{RX_RJ}[1, 2, 3]	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J_{RX_SJ}[1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J_{RX_TJ}[1, 2, 3]	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening	—	0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

3.28. CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics

3.28.1. AC and DC Characteristics

Table 3.35. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}[1]	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	Ω
J_{TX_DDJ}[3, 4]	Output data deterministic jitter	—	—	—	0.17	UI
J_{TX_TJ}[2, 3, 4]	Total output data jitter	—	—	—	0.35	UI

Notes:

1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications *(Continued)*

Symbol	Parameter		Min	Max	Unit
Slave Parallel					
f_{CCLK}	CCLK input clock frequency	—	—	50	MHz
t_{BSCH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{BSCL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{CORD}	CCLK to DOUT for Read Data	—	—	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	—	1.5	—	ns
t_{HCBDI}	Data Hold Time to CCLK	—	1.5	—	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK	—	45	—	ns
t_{HCWD}	WRITEN Hold Time to CCLK	—	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	—	12	ns

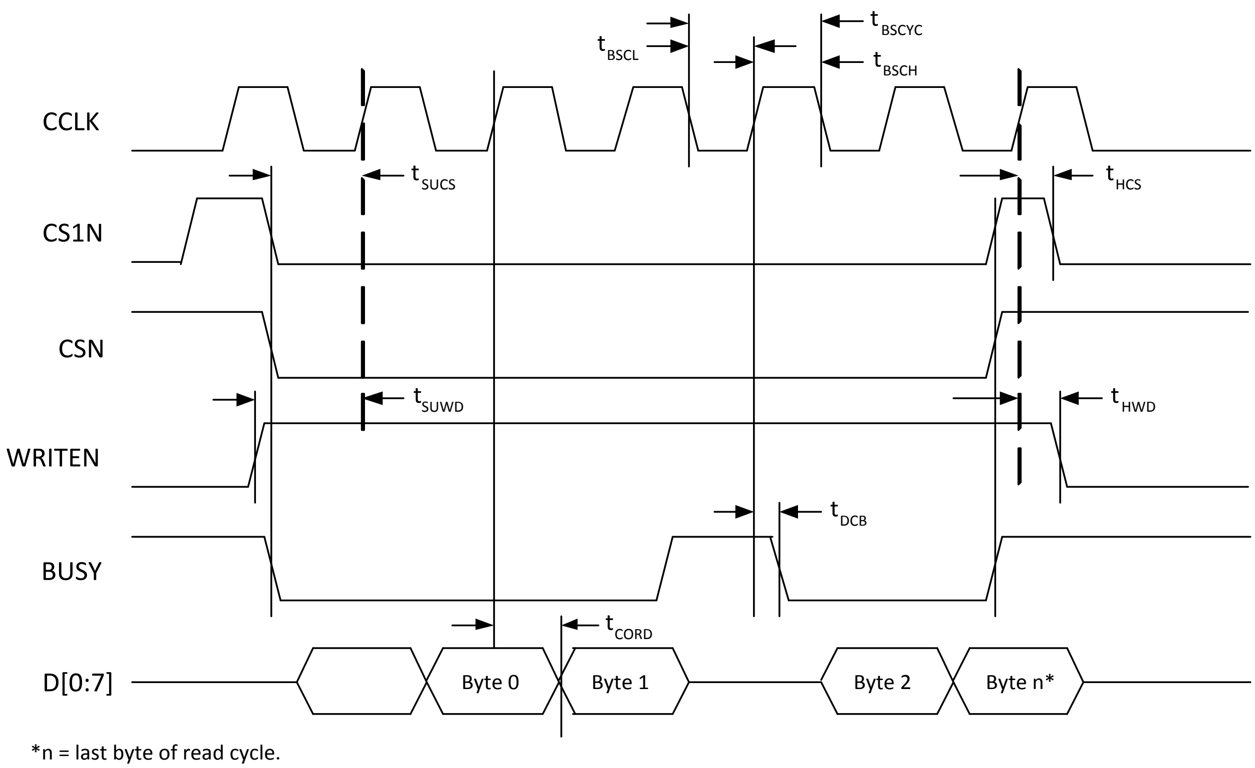
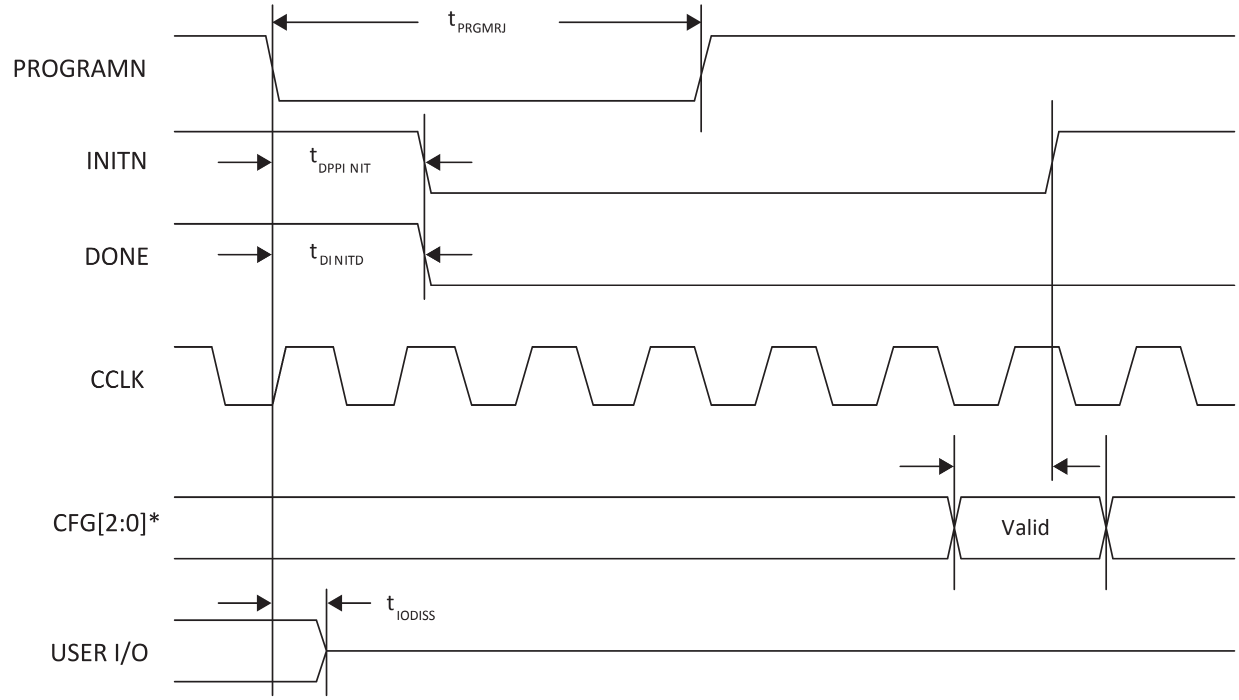


Figure 3.15. sysCONFIG Parallel Port Read Cycle



*The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

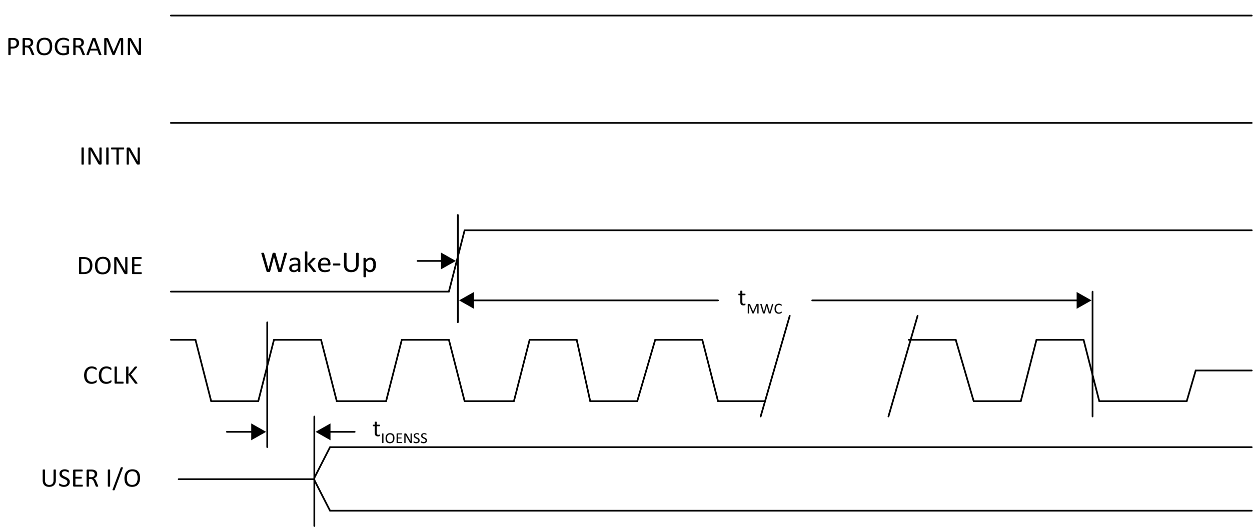


Figure 3.21. Wake-Up Timing

Revision History

Date	Version	Section	Change Summary
March 2018	1.9	All	Updated formatting and page referencing.
		General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-45.
		Architecture	Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support. Updated footnote #1.
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions.
			Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics.
			Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby).
			Updated Table 3.11. sysI/O Recommended Operating Conditions.
			Updated Table 3.12. Single-Ended DC Characteristics.
			Updated Table 3.13. LVDS.
			Updated Table 3.14. LVDS25E DC Conditions.
			Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed.
			Updated Table 3.28. Receiver Total Jitter Tolerance Specification.
			Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics.
			Updated header name of section 3.29 Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics
		Pinout Information	Updated table in section 4.3.2 LFE5U.
		Ordering Information	Added table rows in 5.2.1 Commercial.
			Added table rows in 5.2.2 Industrial.
		Supplemental Information	Updated For Further Information section.
November 2017	1.8	General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-12 and LFE5U-25.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section. • Deleted Serial RapidIO protocol under Embedded SERDES. • Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3. Mentioned transmit de-emphasis “pre- and post-cursors”.
		Architecture	Updated Overview section. • Revised description of PFU blocks. • Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section. • Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. • Deleted Serial RapidIO protocol. • Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section. • Deleted “130 MHz ±15% CMOS” oscillator. • Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA}.
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to t_{SKEW_PR} V_{CCA} and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.

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