Lattice Semiconductor Corporation - LFE5U-85F-7BG756I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

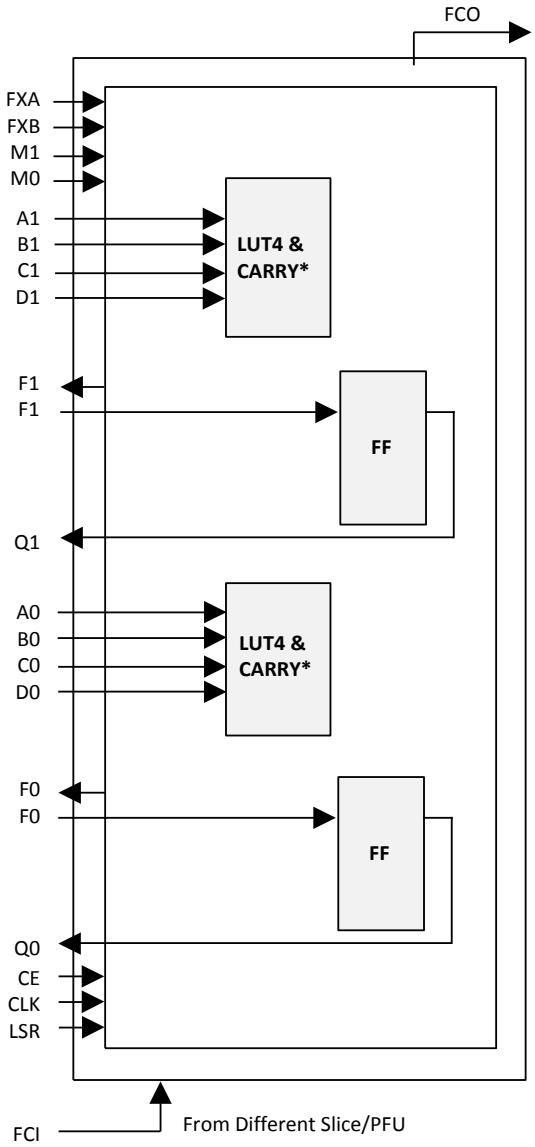
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	365
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	756-FBGA
Supplier Device Package	756-CABGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-85f-7bg756i

Figures



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

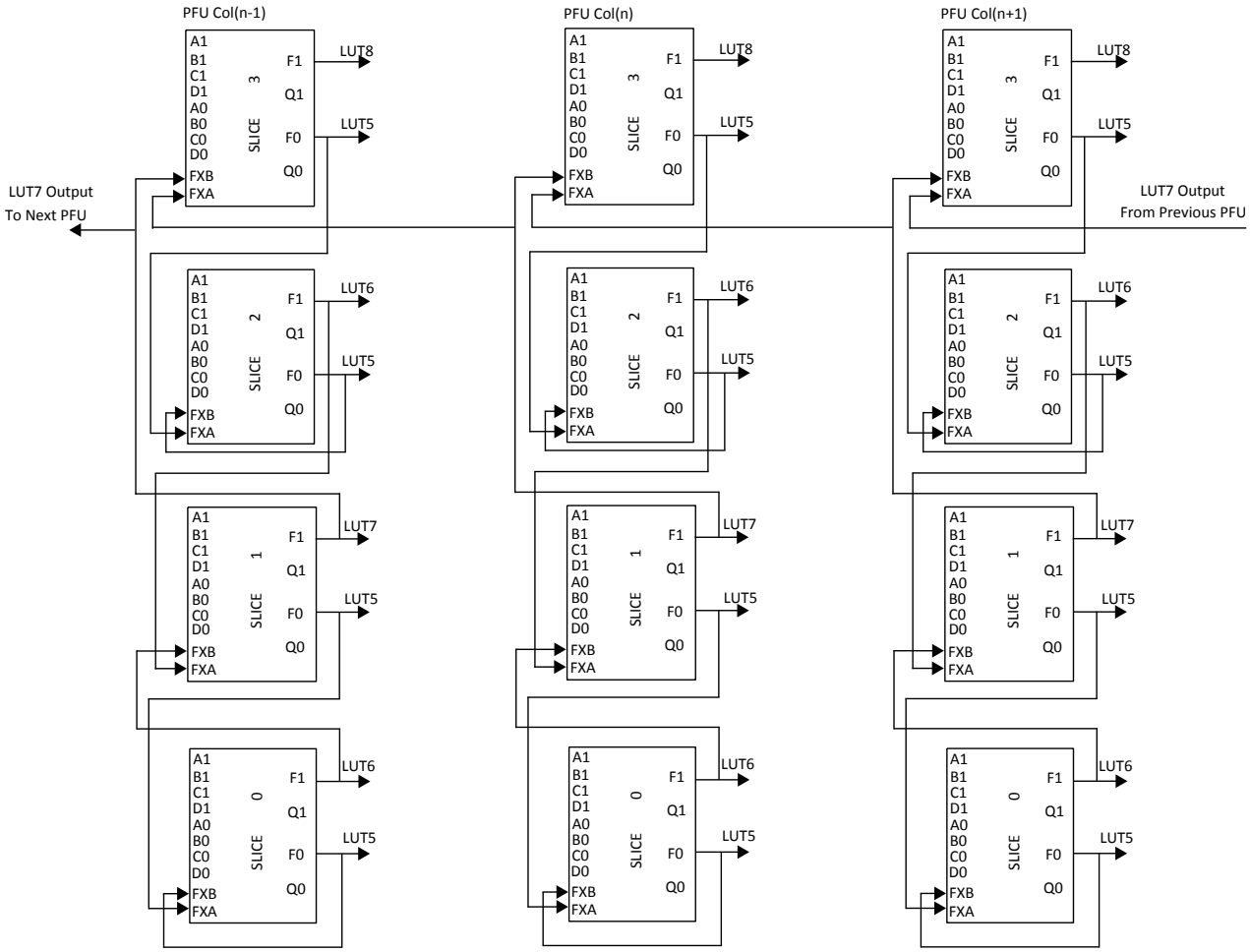


Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output[1]

Notes:

1. See Figure 2.3 on page 15 for connection details.
2. Requires two adjacent PFUs.

Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.

2.7. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

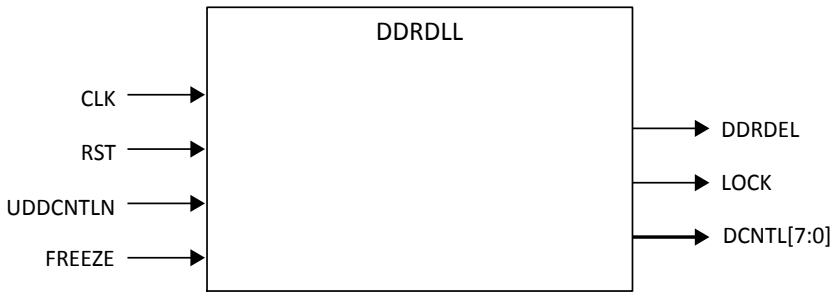


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

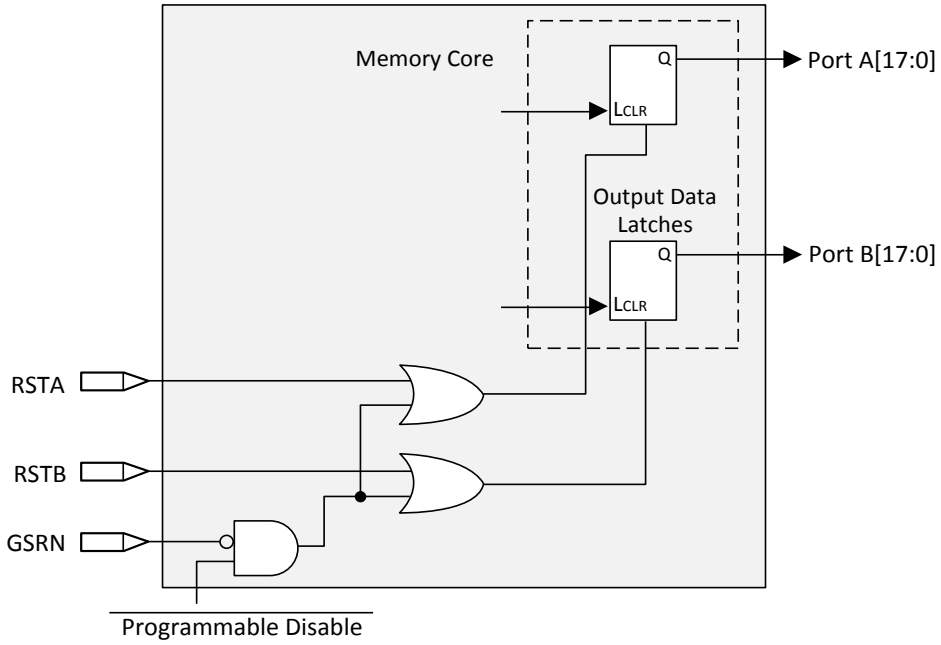


Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

2.9. sysDSP™ Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter			Min	Typ	Max	Unit
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC}, V_{CCAUX}, and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC}, and V_{CCAUX}	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIOs} do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC}, V_{CCAUX}, and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash.

For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA}, before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \le V_{IN} \le V_{IH}$ (Max)	—	—	±1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \le V_{IN} < V_{CCIO}$	—	—	±1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5$ V	—	18	—	mA

Notes:

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ±1 mA.

3.11. SERDES Power Supply Requirements[1,2,3]

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I_{CCA-SB}	V_{CCA} Power Supply Current (Per Channel)	4	9.5	mA
$I_{CCHRX-SB}$[4]	V_{CCHRX}, Input Buffer Current (Per Channel)	—	0.1	mA
$I_{CCHTX-SB}$	V_{CCHTX}, Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 3.125 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	43	54	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	40	50	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	34	43	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	28	38	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For $I_{CCHRX-SB}$, during Standby, input termination on Rx are disabled.
5. For $I_{CCHRX-OP}$, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3, 5]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.13. sysI/O Single-Ended DC Electrical Characteristics

Table 3.12. Single-Ended DC Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33	–0.3	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	16, 12, 8, 4	–16, –12, –8, –4
LVCMOS25	–0.3	0.7	1.7	3.465	0.4	V_{CCIO} – 0.4	12, 8, 4	–12, –8, –4
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	12, 8, 4	–12, –8, –4
LVCMOS15	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	8, 4	–8, –4
LVCMOS12	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	8, 4	–8, –4
LVTTL33	–0.3	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	16, 12, 8, 4	–16, –12, –8, –4
SSTL18_I (DDR2 Memory)	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.465	0.4	V_{CCIO} – 0.4	6.7	–6.7
SSTL18_II	–0.3	V_{REF} –	V_{REF} + 0.125	3.465	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL15 _I (DDR3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.31	V_{CCIO} – 0.31	7.5	–7.5
SSTL15_II (DDR3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.31	V_{CCIO} – 0.31	8.8	–8.8
SSTL135_I (DDR3L Memory)	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	3.465	0.27	V_{CCIO} – 0.27	7	–7
SSTL135_II (DDR3L Memory)	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	3.465	0.27	V_{CCIO} – 0.27	8	–8
MIPI D-PHY (LP)[3]	–0.3	0.55	0.88	3.465	—	—	—	—
HSUL12 (LPDDR2/3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.3	V_{CCIO} – 0.3	4	–4

Notes:

1. For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O (All I/Os used in the same V_{CCIO}).
2. Not all IO types are supported in all banks. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
3. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.14.6. **LVPECL33**

The ECP5/ECP5-5G devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.3 is one possible solution for point-to-point signals.

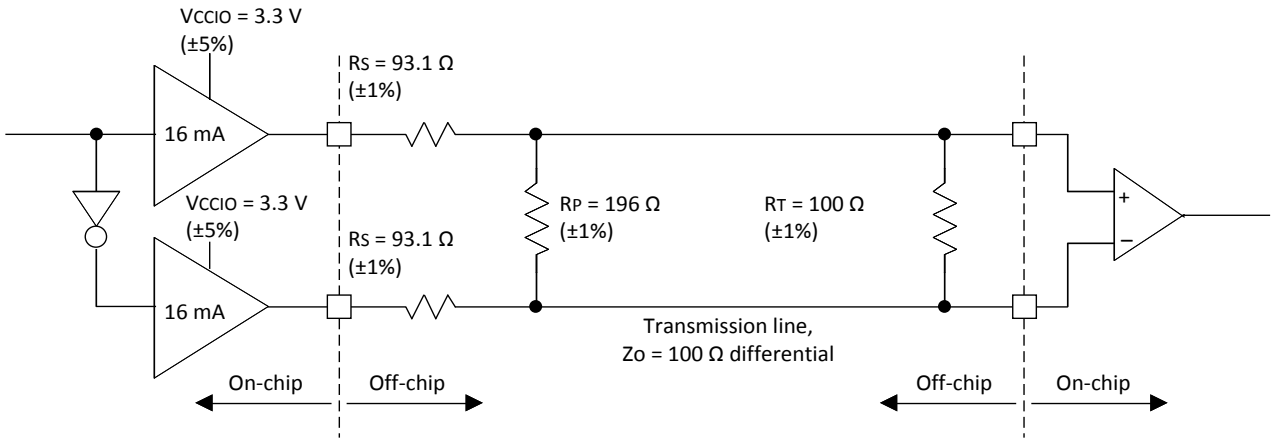


Figure 3.3. Differential LVPECL33

Over recommended operating conditions.

Table 3.16. LVPECL33 DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (±1%)	93	Ω
R_P	Driver Parallel Resistor (±1%)	196	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.15. Typical Building Block Function Performance

Table 3.19. Pin-to-Pin Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	5.06	ns
32-Bit Decoder	6.08	ns
64-Bit Decoder	5.06	ns
4:1 Mux	4.45	ns
8:1 Mux	4.63	ns
16:1 Mux	4.81	ns
32:1 Mux	4.85	ns

Notes:

1. I/Os are configured with LVCMOS25 with V_{CCIO}=2.5, 12 mA drive.
2. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
3. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

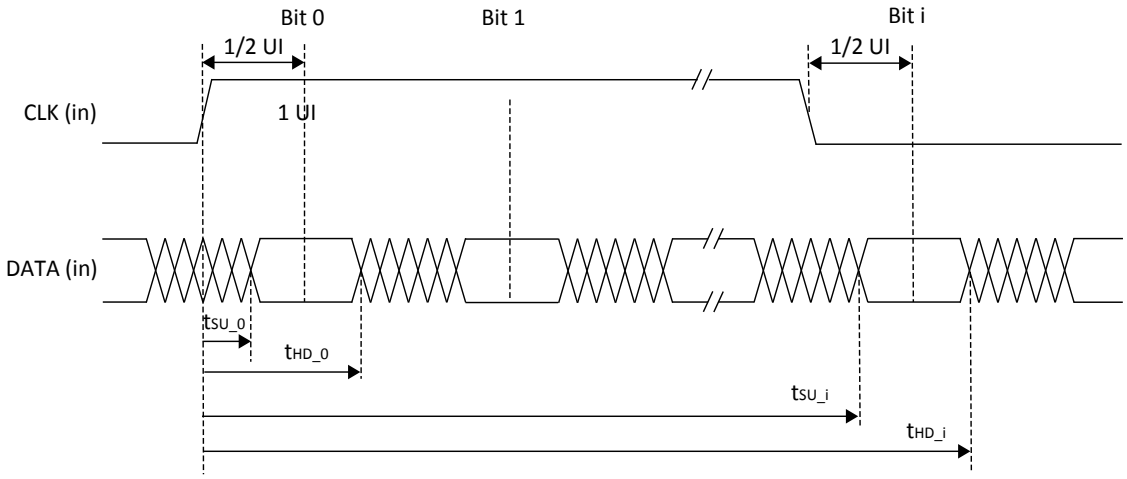


Figure 3.11. Receiver DDRX71_RX Waveforms

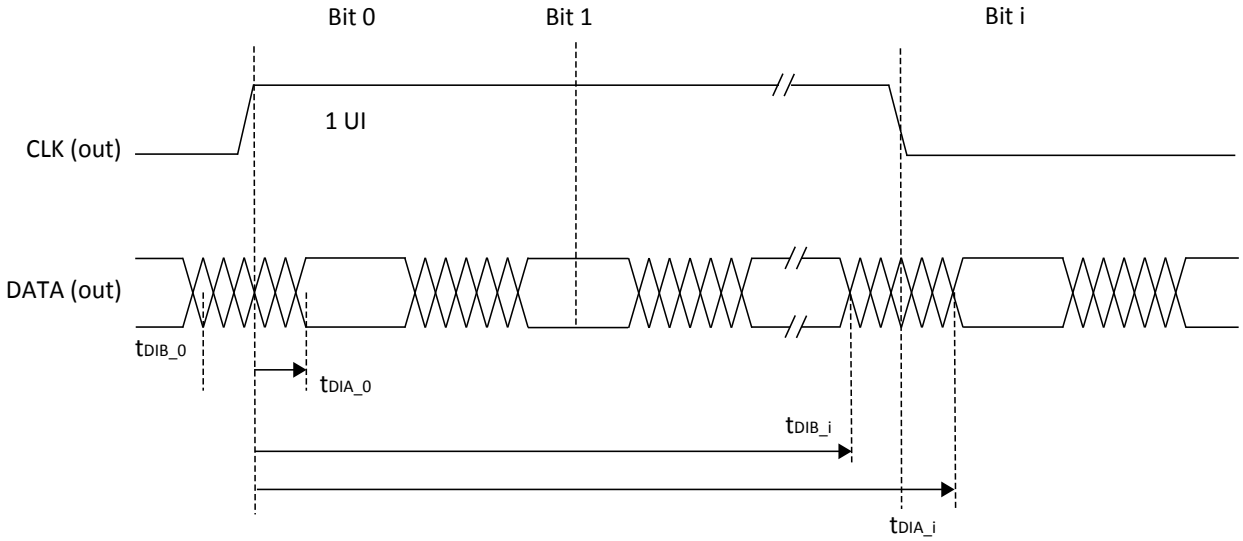


Figure 3.12. Transmitter DDRX71_TX Waveforms

3.20. SERDES High-Speed Data Transmitter

Table 3.24. Serial Output Timing and Levels

Symbol	Description	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Peak-Peak Differential voltage on selected amplitude[1, 2]	–25%	—	25%	mV, p-p
$V_{TX-CM-DC}$	Output common mode voltage	—	V_{CCHTX} / 2	—	mV, p-p
T_{TX-R}	Rise time (20% to 80%)	50	—	—	ps
T_{TX-F}	Fall time (80% to 20%)	50	—	—	ps
$T_{TX-CM-AC-P}$	RMS AC peak common-mode output voltage	—	—	20	mV
Z_{TX_SE}	Single ended output impedance for 50/75 Ω	–20%	50/75	20%	Ω
	Single ended output impedance for 6K Ω	–25%	6K	25%	Ω
RL_{TX_DIFF}	Differential return loss (with package included) [3]	—	—	–10	dB
RL_{TX_COM}	Common mode return loss (with package included) [3]	—	—	–6	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at V_{CCHTX}±5%.
2. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for settings of Tx amplitude.
3. Return los = −10 dB (differential), –6 dB (common mode) for 100 MHz ≤ f <= 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

Table 3.25. Channel Output Jitter

Description	Frequency	Min	Typ	Max	Unit
Deterministic	5 Gb/s	—	—	TBD	UI, p-p
Random	5 Gb/s	—	—	TBD	UI, p-p
Total	5 Gb/s	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	—	—	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	—	—	0.24	UI, p-p

Notes:

1. Values are measured with PRBS 2^7-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.
2. For ECP5-5G family devices only.

3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit						
UI	Unit Interval	—	203.43	203.45	203.47	ps
T_{DCD}	Duty Cycle Distortion	—	—	—	0.05	UI
J_{UBHPJ}	Uncorrelated Bounded High Probability Jitter	—	—	—	0.15	UI
J_{TOTAL}	Total Jitter	—	—	—	0.3	UI
$Z_{RX-DIFF-DC}$	DC differential Impedance	—	80	—	120	Ω
T_{SKEW}	Skew between differential signals	—	—	—	9	ps
$R_{LTX-DIFF}$	Tx Differential Return Loss (S22), including package and silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	—	—	dB
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	100	mA
$T_{RISE\_FALL-DIFF}$	Differential Rise and Fall Time	—		—	—	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—		ps
Receive						
UI	Unit Interval	—	203.43	203.45	203.47	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	—	—	1.2	V, p-p
$V_{RX-EYE\_Y1\_Y2}$	Receiver eye opening mask, Y1 and Y2	—	62.5	—	375	mV, diff
V_{RX-EYE_X1}	Receiver eye opening mask, X1	—	—	—	0.3	UI
T_{RX-TJ}	Receiver total jitter tolerance (not including sinusoidal)	—	—	—	0.6	UI
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
$Z_{RX-DIFF-DC}$	Receiver DC differential impedance	—	80	100	120	Ω

Note: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.39. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDO}	Serial data rate	—	270	—	2975	Mb/s
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	270 Mb/s[6]	—	—	0.2	UI
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	1485 Mb/s	—	—	0.2	UI
$T_{JALIGNMENT}$[1, 2]	Serial output jitter, alignment	2970 Mb/s	—	—	0.3	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mb/s[6]	—	—	0.2	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mb/s	—	—	1	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mb/s	—	—	2	UI

Notes:
1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice SERDES device configured to 50 Ω output impedance connecting to the external cable driver with differential signaling.
4. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mb/s.
5. All LFE5UM/LFE5UM5G devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.
6. 270 Mb/s is supported with Rate Divider only.

Table 3.40. Receive

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDI}	Serial input data rate	—	270	—	2970	Mb/s

Table 3.41. Reference Clock

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F_{VCLK}	Video output clock frequency	—	54	—	148.5	MHz
DC_V	Duty cycle, video clock	—	45	50	55	%

Note: SD-SDI (270 Mb/s) is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) *(Continued)*		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin
SERDES Function		
VCCAx	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCAx = 1.1 V for ECP5, VCCAx = 1.2 V for ECP5-5G.
VCCAUXAx	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUXAx = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	No
LFE5U-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	No
LFE5UM-25F-6MG285C	–6	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-7MG285C	–7	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-6BG381C	–6	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-7BG381C	–7	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-45F-6MG285C	–6	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-7MG285C	–7	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-6BG381C	–6	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-7BG381C	–7	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-6BG554C	–6	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-7BG554C	–7	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-85F-6MG285C	–6	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-7MG285C	–7	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-6BG381C	–6	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-7BG381C	–7	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-6BG554C	–6	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-7BG554C	–7	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-6BG756C	–6	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-7BG756C	–7	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes
LFE5UM5G-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM5G-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM5G-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM5G-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM5G-45F-8BG554C	–8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM5G-85F-8MG285C	–8	Lead free csfBGA	285	Commercial	84	Yes

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