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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

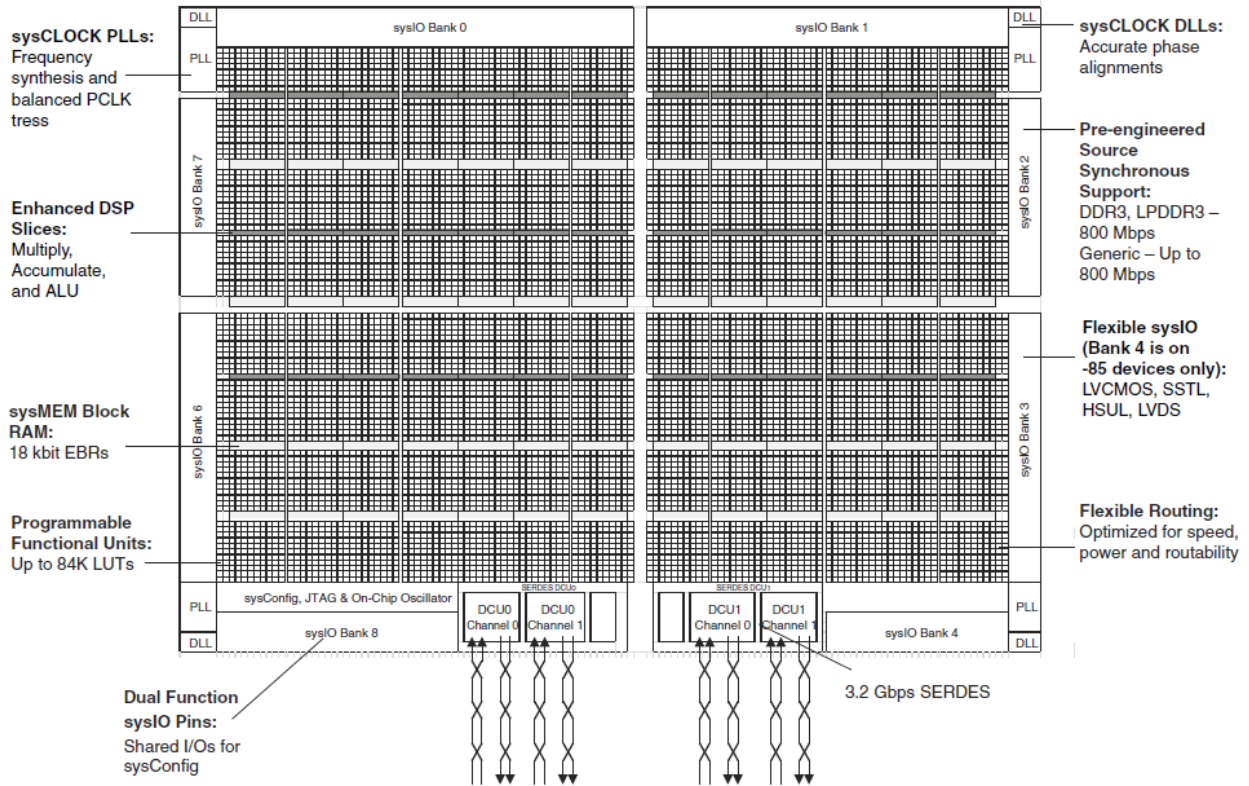
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	365
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	756-FBGA
Supplier Device Package	756-CABGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5u-85f-8bg756i

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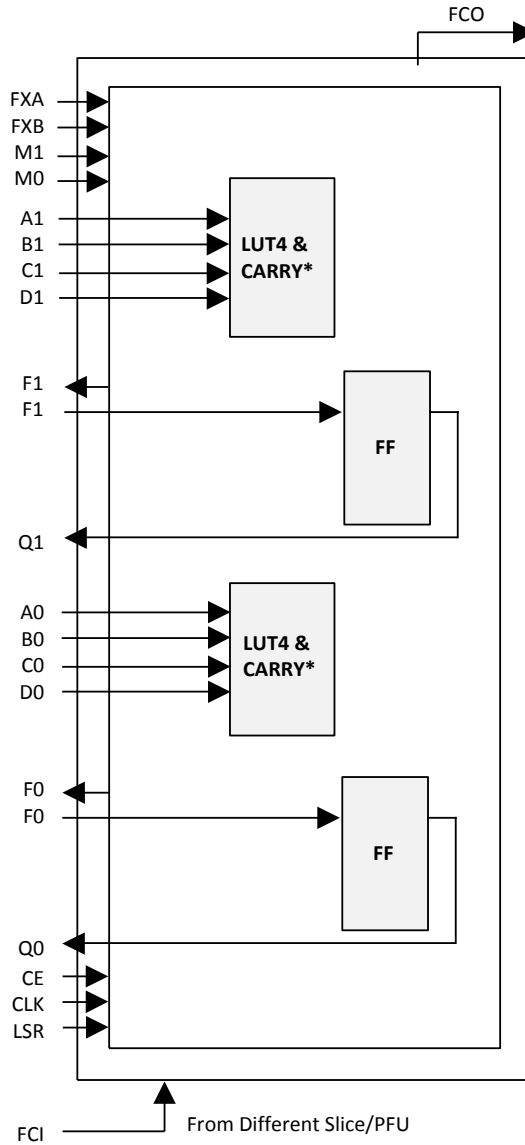
Note: There is no Bank 4 in -25 and -45 devices.
There are no PLL and DLL on the top corners in -25 devices.

Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

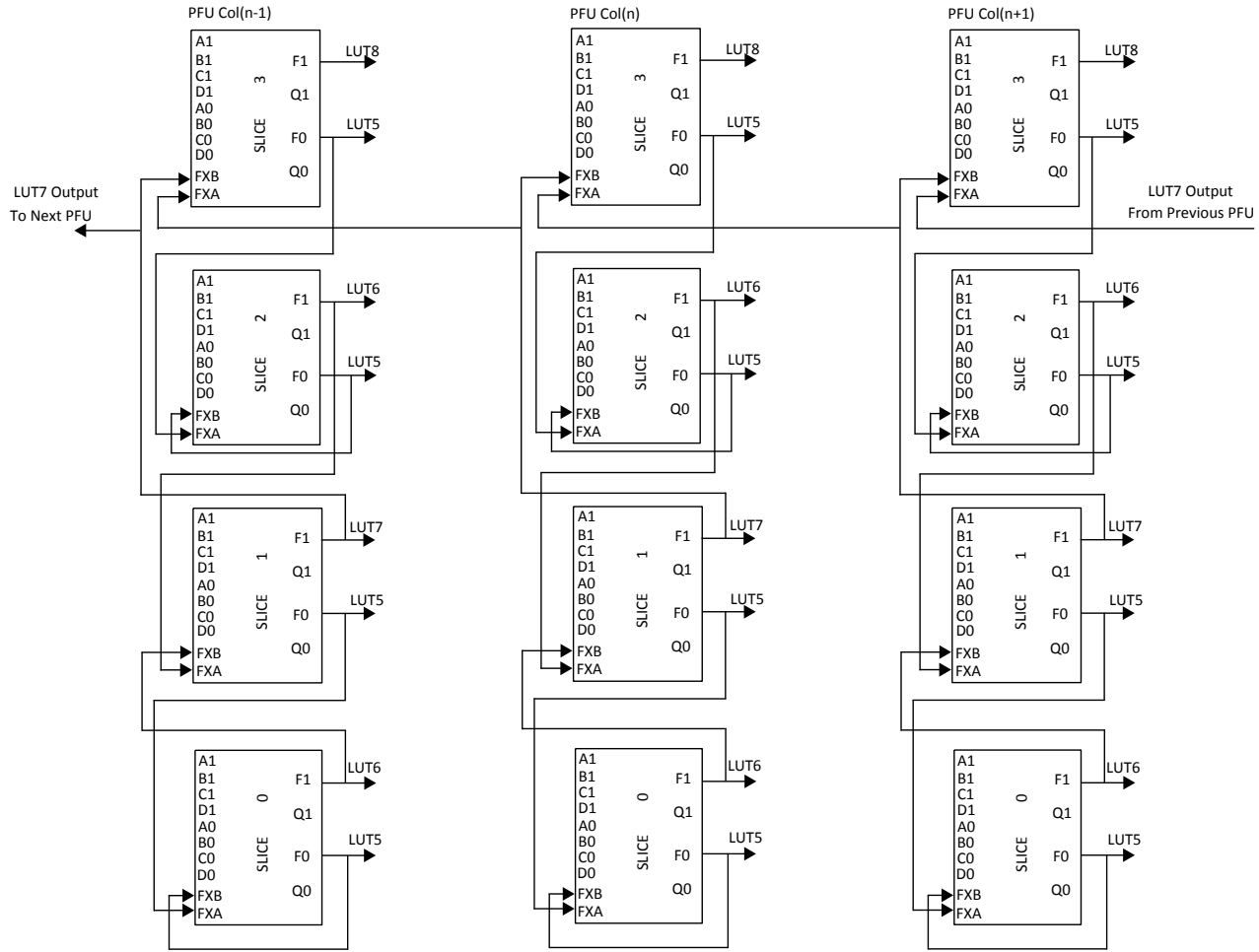


Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output ¹

Notes:

1. See Figure 2.3 on page 15 for connection details.
2. Requires two adjacent PFUs.

Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELOADREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL you can refer to the [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in [Figure 2.6](#) on page 20 for LFE5UM/LFE5UM5G-85 device.

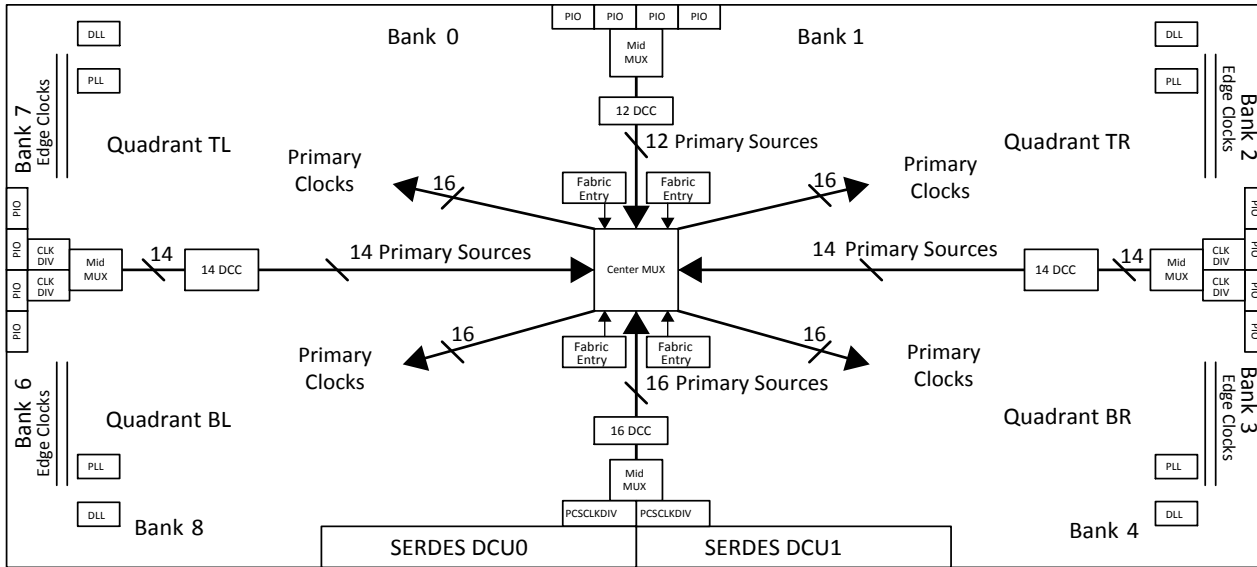


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXes that drive the quadrant clock network. For more information about the DCC, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

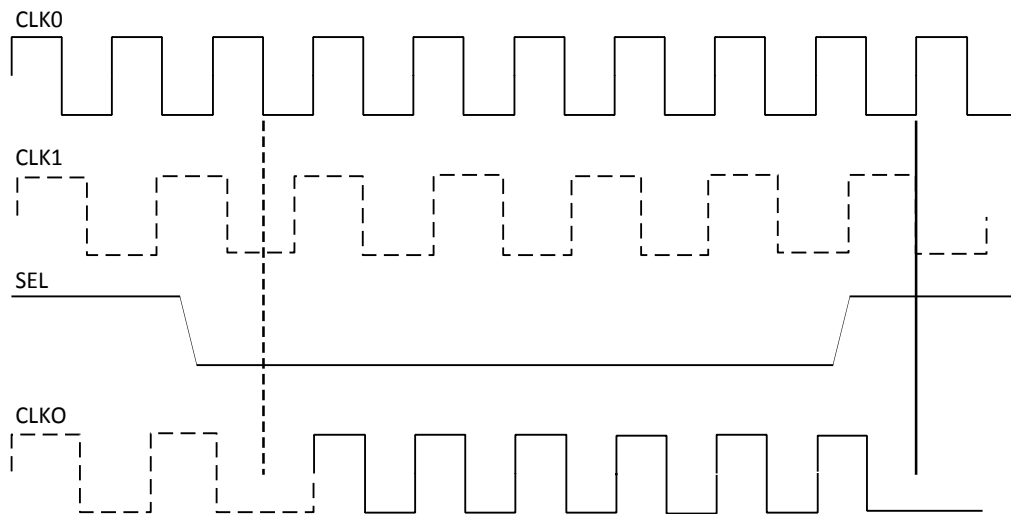


Figure 2.7. DCS Waveforms

2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

In [Figure 2.15](#), note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

[Table 2.7](#) shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note:** One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) – Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to [Minimizing System Interruption During Configuration Using TransFR Technology \(TN1087\)](#) for details.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#).

2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to [LatticeECP3, ECP5 and ECP5-5G Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide \(TN1184\)](#).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. [Table 2.16](#) lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#) and [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter		Min	Typ	Max	Unit	
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC} , V_{CCAUX} , and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC} , and V_{CCAUX})	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIO8} s do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC} , V_{CCAUX} , and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash. For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA} , before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \leq V_{IN} \leq V_{IH}$ (Max)	—	—	± 1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \leq V_{IN} < V_{CCIO}$	—	—	± 1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5$ V	—	18	—	mA

Notes:

1. V_{CC} , V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .
3. LVCMOS and LVTTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ± 1 mA.

3.12. **sysI/O Recommended Operating Conditions**
Table 3.11. sysI/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVC MOS33 ¹	3.135	3.3	3.465	—	—	—
LVC MOS33D ³ Output	3.135	3.3	3.465	—	—	—
LVC MOS25 ¹	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 ¹	1.14	1.2	1.26	—	—	—
LVTTL33 ¹	3.135	3.3	3.465	—	—	—
SSTL15_I, _II ²	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II ²	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12 ²	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input ^{3, 5}	1.425	1.5	1.575	—	—	—
LVDS25 ^{1, 3} Output	2.375	2.5	2.625	—	—	—
subLVDS ³ (Input only)	—	—	—	—	—	—
SLVS ³ (Input only)	—	—	—	—	—	—
LVDS25E ³ Output	2.375	2.5	2.625	—	—	—
MLVDS ³ Output	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1, 3} Output	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1, 3} Output	2.375	2.5	2.625	—	—	—
HSULD12D ^{2, 3}	1.14	1.2	1.26	—	—	—
SSTL135D_I, II ^{2, 3}	1.28	1.35	1.42	—	—	—
SSTL15D_I, II ^{2, 3}	1.43	1.5	1.57	—	—	—
SSTL18D_I ^{1, 2, 3} , II ^{1, 2, 3}	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVC MOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVC MOS12.

3.14. sysI/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.13. LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	± 100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	± 10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100 \Omega$	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100 \Omega$	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100 \Omega$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100 \Omega$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0 V$ Driver outputs shorted to each other	—	—	12	mA

Note: On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5 V$ or $3.3 V$.

3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with $3.3 V_{CCIO}$. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

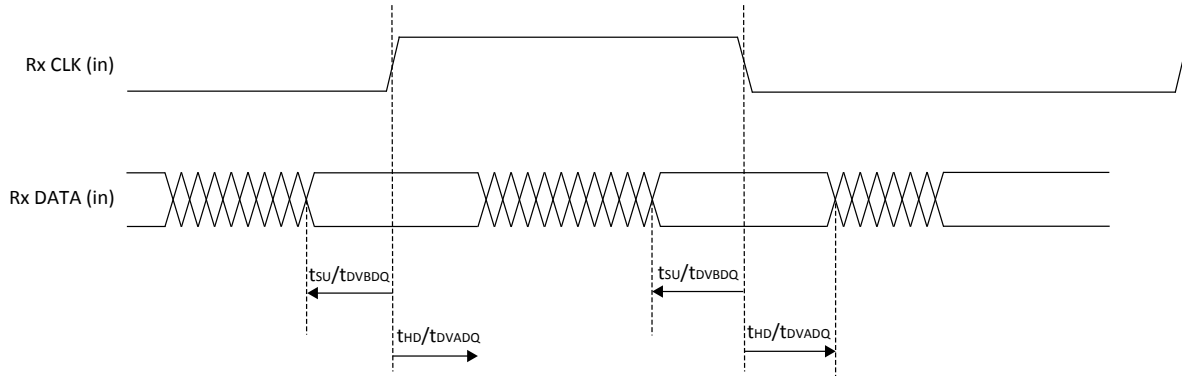


Figure 3.6. Receiver RX.CLK.Centered Waveforms

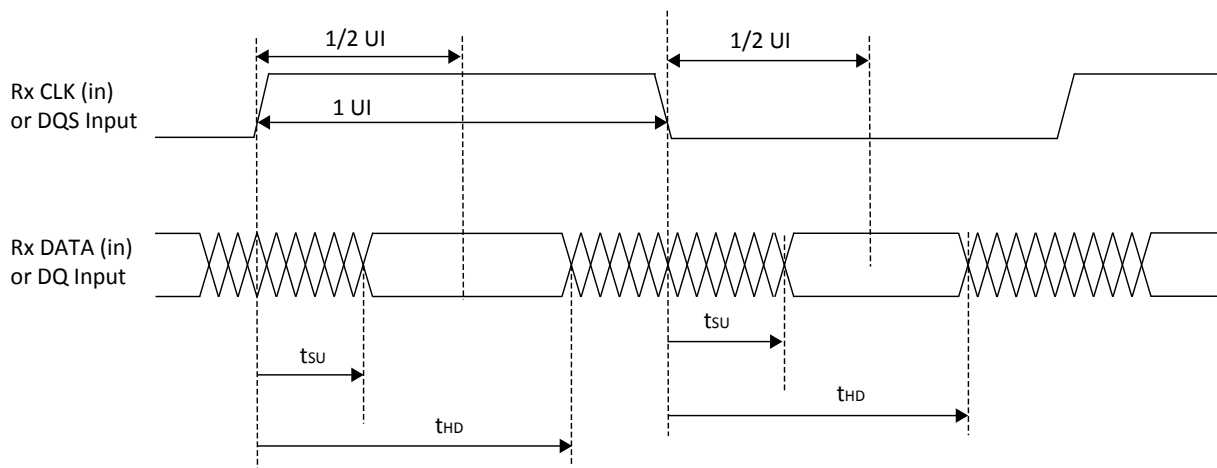


Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

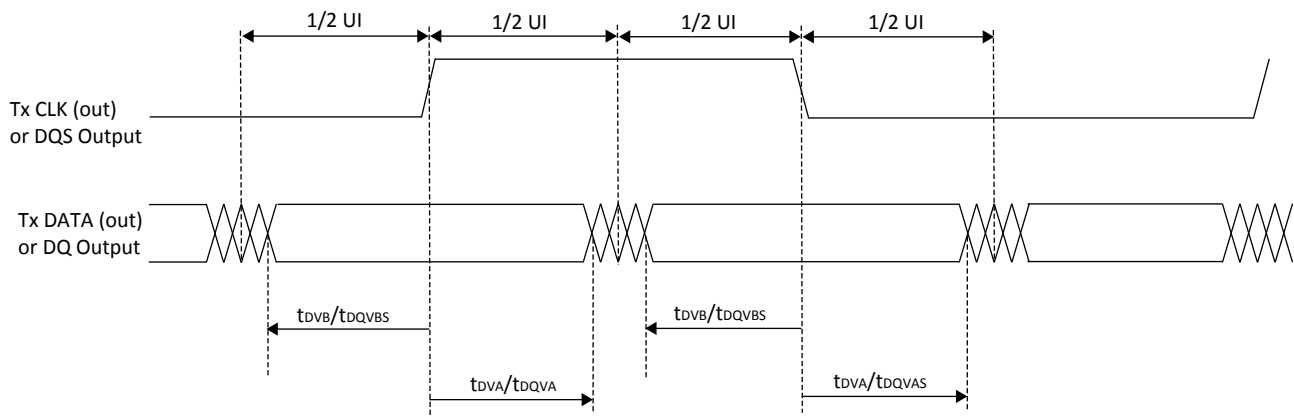


Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

3.20. SERDES High-Speed Data Transmitter

Table 3.24. Serial Output Timing and Levels

Symbol	Description	Min	Typ	Max	Unit
V _{TX-DIFF-PP}	Peak-Peak Differential voltage on selected amplitude ^{1, 2}	-25%	—	25%	mV, p-p
V _{TX-CM-DC}	Output common mode voltage	—	V _{CCHTX} / 2	—	mV, p-p
T _{TX-R}	Rise time (20% to 80%)	50	—	—	ps
T _{TX-F}	Fall time (80% to 20%)	50	—	—	ps
T _{TX-CM-AC-P}	RMS AC peak common-mode output voltage	—	—	20	mV
Z _{TX-SE}	Single ended output impedance for 50/75 Ω	-20%	50/75	20%	Ω
	Single ended output impedance for 6K Ω	-25%	6K	25%	Ω
RL _{TX-DIFF}	Differential return loss (with package included) ³	—	—	-10	dB
RL _{TX-COM}	Common mode return loss (with package included) ³	—	—	-6	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at V_{CCHTX}±5%.
2. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for settings of Tx amplitude.
3. Return los = -10 dB (differential), -6 dB (common mode) for 100 MHz ≤ f ≤ 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

Table 3.25. Channel Output Jitter

Description	Frequency	Min	Typ	Max	Unit
Deterministic	5 Gb/s	—	—	TBD	UI, p-p
Random	5 Gb/s	—	—	TBD	UI, p-p
Total	5 Gb/s	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	—	—	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	—	—	0.24	UI, p-p

Notes:

1. Values are measured with PRBS 2⁷-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.
2. For ECP5-5G family devices only.

Signal Name	I/O	Description
PLL, DLL and Clock Functions (Continued)		
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
[T/R]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. This is a dedicated input pin.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.
Configuration Pads (Used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes (Master SPI, Master Serial). This is a dedicated pin.
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPI _m mode data output. This is a shared I/O pin. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DOUT/CSON	O	Serial data output. Chip select output. SPI/SPI _m mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DO/MOSI/IOO	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-85F-6BG756I	-6	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-7BG756I	-7	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	No
LFE5UM-25F-6MG285I	-6	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-7MG285I	-7	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-6BG381I	-6	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-7BG381I	-7	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-45F-6MG285I	-6	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-7MG285I	-7	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-6BG381I	-6	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-7BG381I	-7	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-6BG554I	-6	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-7BG554I	-7	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-85F-6MG285I	-6	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-7MG285I	-7	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-6BG381I	-6	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-7BG381I	-7	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-6BG554I	-6	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-7BG554I	-7	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-6BG756I	-6	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-7BG756I	-7	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	Yes
LFE5UM5G-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM5G-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM5G-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM5G-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM5G-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM5G-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM5G-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM5G-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM5G-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	Yes

Supplemental Information

For Further Information

A variety of technical notes for the ECP5/ECP5-5G family are available.

- [High-Speed PCB Design Considerations \(TN1033\)](#)
- [Transmission of High-Speed Serial Signals Over Common Cable Media \(TN1066\)](#)
- [PCB Layout Recommendations for BGA Packages \(TN1074\)](#)
- [Minimizing System Interruption During Configuration Using TransFR Technology \(TN1087\)](#)
- [Electrical Recommendations for Lattice SERDES \(FPGA-TN-02077\)](#)
- [LatticeECP3, ECP-5 and ECP5-5G Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide \(TN1184\)](#)
- [Using TraceID \(TN1207\)](#)
- [Sub-LVDS Signaling Using Lattice Devices \(TN1210\)](#)
- [Advanced Security Encryption Key Programming Guide for ECP5, ECP5-5G, LatticeECP3, and LatticeECP2/MS Devices \(TN1215\)](#)
- [LatticeECP3, LatticeECP2/M, ECP5 and ECP5-5G Dual Boot and Multiple Boot Feature \(TN1216\)](#)
- [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#)
- [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#)
- [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#)
- [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#)
- [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#)
- [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#)
- [Power Consumption and Management for ECP5 and ECP5-5G Devices \(TN1266\)](#)
- [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#)
- [ECP5 and ECP5-5G Hardware Checklist \(FPGA-TN-02038\)](#)
- [Solder Reflow Guide for Surface Mount Devices \(FPGA-TN-02041\)](#)
- [ECP5 and ECP5-5G PCI Express Soft IP Ease of Use Guidelines \(FPGA-TN-02045\)](#)
- [Programming External SPI Flash through JTAG for ECP5/ECP5-5G \(FPGA-TN-02050\)](#)
- [Adding Scalable Power and Thermal Management to ECP5 Using L-ASC10 \(AN6095\)](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL): www.jedec.org
- PCI: www.pcisig.com

Revision History

Date	Version	Section	Change Summary
March 2018	1.9	All	Updated formatting and page referencing.
		General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide . Added caBGA256 package in LFE5U-45.
		Architecture	Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support . Updated footnote #1.
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions .
			Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics .
			Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) .
			Updated Table 3.11. sys/O Recommended Operating Conditions .
			Updated Table 3.12. Single-Ended DC Characteristics .
			Updated Table 3.13. LVDS .
			Updated Table 3.14. LVDS25E DC Conditions .
			Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed .
			Updated Table 3.28. Receiver Total Jitter Tolerance Specification .
			Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics .
			Updated header name of section 3.29 Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics .
		Pinout Information	Updated table in section 4.3.2 LFE5U .
Ordering Information	Added table rows in 5.2.1 Commercial .		
	Added table rows in 5.2.2 Industrial .		
Supplemental Information	Updated For Further Information section.		
November 2017	1.8	General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide . Added caBGA256 package in LFE5U-12 and LFE5U-25.