# E. Lattice Semiconductor Corporation - LFE5UM-25F-6BG381C Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-25f-6bg381c

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# Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay-Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLL	Phase-Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SERDES	Serializer/Deserializer
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
ТАР	Test Access Port
TDM	Time Division Multiplexing

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- Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O<sup>™</sup> Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 18/15 I, II
  - HSUL12
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

- subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
  - Shared bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR<sup>™</sup> I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
  - Soft Error Detect Embedded hard macro
  - Soft Error Correction Without stopping user operation
  - Soft Error Injection Emulate SEU event to debug system error handling
- System Level Support
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - On-chip oscillator for initialization and general use
  - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U- 12	LFE5U- 25	LFE5U- 45	LFE5U- 85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels /	IO Count)						
256 caBGA (14 x 14 mm <sup>2</sup> , 0.8 mm)	-	—	-	0/197	0/197	0/197	-
285 csfBGA (10 x 10 mm <sup>2</sup> , 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm², 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm <sup>2</sup> , 0.8 mm)	_	4/245	4/259	_	_	0/245	0/259
756 caBGA (27 x 27 mm², 0.8 mm)	_	_	4/365	_	_	_	0/365

#### Table 1.1. ECP5 and ECP5-5G Family Selection Guide

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# 2. Architecture

# 2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM<sup>™</sup> Embedded Block RAM (EBR) and rows of sysDSP<sup>™</sup> Digital Signal Processing slices, as shown in Figure 2.1 on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG<sup>™</sup> ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.





Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)

# 2.2. **PFU Blocks**

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.



Table 2.4 provides a	description of	the signals	in the PLL blocks.
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Signal	Туре	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

#### Table 2.4. PLL Blocks Signal Descriptions

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

# 2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.



## 2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).



Figure 2.7. DCS Waveforms

# 2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

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# 2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.



Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

# 2.9. sysDSP<sup>™</sup> Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

# 2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.



- 5\*5 and larger size 2D blocks Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2<sup>™</sup> and LatticeECP3<sup>™</sup> sysDSP block, such that, legacy applications can be targeted to the ECP5/ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.



Figure 2.14. Simplified sysDSP Slice Block Diagram











# 2.11. **PIO**

The PIO contains three blocks: an input register block, output register block, and tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

# 2.11.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers to shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers samples the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The top side of the device supports IDDRX1 gearing function. For more information on gearing function, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

Figure 2.17 shows the input register block for the PIOs on the top edge.



Figure 2.17. Input Register Block for PIO on Top Side of the Device

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



\*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

#### Figure 2.18. Input Register Block for PIO on Left and Right Side of the Device



Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	-	2	2
756 caBGA	-	-	2

#### Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

# 2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).



Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

# 2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

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# 3.18. External Switching Characteristics

Over recommended commercial operating conditions.

## Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Devementer	the Description		-8		-7		-6		11
Parameter	Description	Device	Min	Max	Min	Max	Min	Max	Unit
Clocks									
Primary Clock									
f <sub>MAX_PRI</sub>	Frequency for Primary Clock Tree	_	—	370	—	303	_	257	MHz
t <sub>w_pri</sub>	Clock Pulse Width for Primary Clock	-	0.8	—	0.9	_	1.0	-	ns
t <sub>skew_pri</sub>	Primary Clock Skew within a Device	-	_	420	_	462	-	505	ps
Edge Clock									
f <sub>MAX_EDGE</sub>	Frequency for Edge Clock Tree		_	400	—	350		312	MHz
tw_edge	Clock Pulse Width for Edge Clock	_	1.175	—	1.344	—	1.50	-	ns
t <sub>skew_edge</sub>	Edge Clock Skew within a Bank	_	—	160	—	180	-	200	ps
Generic SDR Input									
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ithout PL	L					
t <sub>co</sub>	Clock to Output - PIO Output Register	All Devices	_	5.4	_	6.1	-	6.8	ns
t <sub>su</sub>	Clock to Data Setup - PIO Input Register	All Devices	0	_	0	_	0	_	ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	All Devices	2.7	_	3	_	3.3	Ι	ns
t <sub>su_del</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	_	1.33	_	1.46	-	ns
t <sub>h_del</sub>	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	_	0	_	0	-	ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	All Devices	_	400	_	350	_	312	MHz
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ith PLL						
t <sub>copll</sub>	Clock to Output - PIO Output Register	All Devices	_	3.5	_	3.8	_	4.1	ns
t <sub>supll</sub>	Clock to Data Setup - PIO Input Register	All Devices	0.7	-	0.78	_	0.85	_	ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	All Devices	0.8	_	0.89	_	0.98	_	ns
t <sub>su_delpll</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	_	1.78	_	1.95	_	ns

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# 3.20. SERDES High-Speed Data Transmitter

#### Table 3.24. Serial Output Timing and Levels

Symbol	Description	Min	Тур	Max	Unit
V <sub>TX-DIFF-PP</sub>	Peak-Peak Differential voltage on selected amplitude <sup>1, 2</sup>	-25%	—	25%	mV, p-p
V <sub>TX-CM-DC</sub>	Output common mode voltage	—	V <sub>CCHTX</sub> / 2	—	mV, p-p
T <sub>TX-R</sub>	Rise time (20% to 80%)	50	—	—	ps
T <sub>TX-F</sub>	Fall time (80% to 20%)	50	—	—	ps
T <sub>TX-CM-AC-P</sub>	RMS AC peak common-mode output voltage	—	—	20	mV
-	Single ended output impedance for 50/75 $\boldsymbol{\Omega}$	-20%	50/75	20%	Ω
ZTX_SE	Single ended output impedance for 6K $\boldsymbol{\Omega}$	-25%	6K	25%	Ω
RL <sub>TX_DIFF</sub>	Differential return loss (with package included) <sup>3</sup>	—	—	-10	dB
RL <sub>TX_COM</sub>	Common mode return loss (with package included) $^3$	_	_	-6	dB

#### Notes:

1. Measured with 50  $\Omega$  Tx Driver impedance at V\_{CCHTx} \pm 5\%.

2. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for settings of Tx amplitude.

3. Return los = -10 dB (differential), -6 dB (common mode) for 100 MHz  $\leq$  f <= 1.6 GHz with 50  $\Omega$  output impedance configuration. This includes degradation due to package effects.

#### Table 3.25. Channel Output Jitter

Description	Frequency	Min	Тур	Max	Unit
Deterministic	5 Gb/s	—	—	TBD	UI, p-p
Random	5 Gb/s	—	—	TBD	UI, p-p
Total	5 Gb/s	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	_	_	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	_	_	0.24	UI, p-p

Notes:

1. Values are measured with PRBS 2<sup>7</sup>-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

2. For ECP5-5G family devices only.



#### Table 3.36. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z <sub>RX_DIFF</sub>	Differential termination resistance	_	80	100	120	Ω
J <sub>RX_DJ</sub> <sup>2, 3, 4</sup>	Deterministic jitter tolerance (peak-to-peak)	_	_	_	0.37	UI
J <sub>RX_RJ</sub> <sup>2, 3, 4</sup>	Random jitter tolerance (peak-to-peak)	_	—	—	0.18	UI
J <sub>RX_SJ</sub> <sup>2, 3, 4</sup>	Sinusoidal jitter tolerance (peak-to-peak)	_	—	—	0.10	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3, 4</sup>	Total jitter tolerance (peak-to-peak)	_	—	—	0.65	UI
T <sub>RX_EYE</sub>	Receiver eye opening	—	0.35	—	-	UI

Notes:

- 1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
- 2. Jitter values are measured with each high-speed input AC coupled into a 50  $\Omega$  impedance.
- 3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
- 4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

# 3.29. Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics

## 3.29.1. AC and DC Characteristics

#### Table 3.37. Transmit

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
T <sub>RF</sub>	Differential rise/fall time	20% to 80%	-	80	—	ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance	-	80	100	120	Ω
J <sub>TX_DDJ</sub> <sup>2, 3</sup>	Output data deterministic jitter	-	-	_	0.10	UI
J <sub>TX_TJ</sub> <sup>1, 2, 3</sup>	Total output data jitter	-	1	—	0.24	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

2. Jitter values are measured with each CML output AC coupled into a 50  $\Omega$  impedance (100  $\Omega$  differential impedance).

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

#### Table 3.38. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z <sub>RX_DIFF</sub>	Differential termination resistance	-	80	100	120	Ω
J <sub>RX_DJ</sub> <sup>1, 2, 3, 4</sup>	Deterministic jitter tolerance (peak-to-peak)	-	—	—	0.34	UI
J <sub>RX_RJ</sub> <sup>1, 2, 3, 4</sup>	Random jitter tolerance (peak-to-peak)	-	—	—	0.26	UI
J <sub>RX_SJ</sub> <sup>1, 2, 3, 4</sup>	Sinusoidal jitter tolerance (peak-to-peak)	-	—	—	0.11	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3, 4</sup>	Total jitter tolerance (peak-to-peak)	—	—	—	0.71	UI
T <sub>RX_EYE</sub>	Receiver eye opening	—	0.29	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.

- 2. Jitter values are measured with each high-speed input AC coupled into a 50  $\Omega$  impedance.
- 3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
- 4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

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## Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit		
Slave Parallel						
f <sub>CCLK</sub>	CCLK input clock frequency	—	—	50	MHz	
t <sub>BSCH</sub>	CCLK input clock pulsewidth HIGH	—	6	—	ns	
t <sub>BSCL</sub>	CCLK input clock pulsewidth LOW	—	6	—	ns	
t <sub>CORD</sub>	CCLK to DOUT for Read Data	—	—	12	ns	
t <sub>sucbdi</sub>	Data Setup Time to CCLK	—	1.5	—	ns	
t <sub>HCBDI</sub>	Data Hold Time to CCLK	—	1.5	—	ns	
t <sub>sucs</sub>	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns	
t <sub>HCS</sub>	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns	
t <sub>suwd</sub>	WRITEN Setup Time to CCLK	—	45	—	ns	
t <sub>HCWD</sub>	WRITEN Hold Time to CCLK	—	2	—	ns	
t <sub>DCB</sub>	CCLK to BUSY Delay Time	—	—	12	ns	



Figure 3.15. sysCONFIG Parallel Port Read Cycle

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\*The CFG pins are normally static (hardwired).











# 5.2. Ordering Part Numbers

## 5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	-6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	-7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	-8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	-6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	-7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	-8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	-6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	-7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	-8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	-6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	-7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	-8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	-6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	-7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	-8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	No

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Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-85F-6BG756I	-6	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-7BG756I –7		Lead free caBGA 756		Industrial	84	No
LFE5U-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	No
LFE5UM-25F-6MG285I	-6	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-7MG285I	-7	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-6BG381I	-6	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-7BG381I	-7	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-45F-6MG285I	-6	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-7MG285I	-7	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-6BG381I	-6	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-7BG381I	-7	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-6BG554I	-6	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-7BG554I	-7	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-85F-6MG285I	-6	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-7MG285I	-7	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-6BG381I	-6	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-7BG381I	-7	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-6BG554I	-6	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-7BG554I	-7	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-6BG756I	-6	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-7BG756I	-7	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	Yes
LFE5UM5G-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM5G-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM5G-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM5G-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM5G-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM5G-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM5G-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM5G-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM5G-85F-8BG756I	-8	Lead free caBGA	756	Industrial	84	Yes



# **Revision History**

Date	Version	Section	Change Summary
March 2018	1.9	All	Updated formatting and page referencing.
		General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-45.
		Architecture	Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support. Updated footnote #1.
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions.
			Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics.
			Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby).
			Updated Table 3.11. sysl/O Recommended Operating Conditions.
			Updated Table 3.12. Single-Ended DC Characteristics.
			Updated Table 3.13. LVDS.
			Updated Table 3.14. LVDS25E DC Conditions.
			Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed.
			Updated Table 3.28. Receiver Total Jitter Tolerance Specification.
			Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics.
			Updated header name of section 3.29 Gigabit Ethernet/CGMII(1, 25Gbps)/CBRI LVE 12 Electrical and Timing
			Characteristics
		Pinout Information	Updated table in section 4.3.2 LFE5U.
		Ordering Information	Added table rows in 5.2.1 Commercial.
			Added table rows in 5.2.2 Industrial.
		Supplemental Information	Updated For Further Information section.
November 2017	1.8	General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-12 and LFE5U-25.



#### (Continued)

Date	Version	Section	Change Summary
April 2017	1.7	All	Changed document number from DS1044 to FPGA-DS-02012.
		General Description	Updated Features section. Changed "1.1 V core power supply" to "1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G".
		Architecture	Updated Overview section. Change "The ECP5/ECP5-5G devices use 1.1 V as their core voltage" to "The ECP5 devices use 1.1V, ECP5UM5G devices use 1.2V as their core voltage"
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions Added ECP5-5G on VCC to be 1.2V +/- 5% Added ECP5-5G on VCCA to be 1.2V +/- 3% Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) Changed "Core Power Supply Current" for ICC on LFE5UM5G devices Changed "SERDES Power Supply Current (Per Dual)" for ICCA on LFE5UM5G devices Updated Table 3.20. Register-to-Register Performance. Remove "(DDR/SDR)" from DSP Function Changed DSP functions to 225 MHz
		Pinout Information	Update Section 4.1 Signal Description. Revised Vcc Description to "Power supply pins for core logic. Dedicated pins. VCC = 1.1 V (ECP5), 1.2 V (ECP5UM5G)"
February 2016	1.6	All	Changed document status from Preliminary to Final.
		General Description	Updated Features section. Changed "24K to 84K LUTs" to "12K to 84K LUTs". Added LFE5U-12 column to Table 1.1. ECP5 and ECP5-5G Family Selection Guide.
		DC and Switching Characteristics	Updated Power up Sequence section. Identified typical ICC current for specific devices in Table 3.8. ECP5/ECP5-5G Supply Current (Standby). Updated values in Table 3.9. ECP5. Updated values in Table 3.10. ECP5-5G. Added values to -8 Timing column of Table 3.19. Pin-to-Pin Performance. Added values to -8 Timing column of Table 3.20. Register-to-Register Performance. Changed LFE5-45 to All Devices in Table 3.22. ECP5/ECP5-5G External Switching Characteristics. Added table notes to Table 3.31. PCIe (5 Gb/s). Added table note to Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics.
		Pinout Information	Added LFE5U-12 column to the table in LFE5U section.
		Ordering Information	Updated LFE5U in ECP5/ECP5-5G Part Number Description section: added 12 F = 12K LUTs to Logic Capacity. Added LFE5U-12F information to Ordering Part Numbers section.