



Welcome to [E-XFL.COM](https://www.e-xfl.com)

## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-25f-8mg285c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-25f-8mg285c</a>

# 1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

## 1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 84K LUTs
  - 197 to 365 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 3.744 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs

## 2. Architecture

### 2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in [Figure 2.1](#) on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG™ ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.

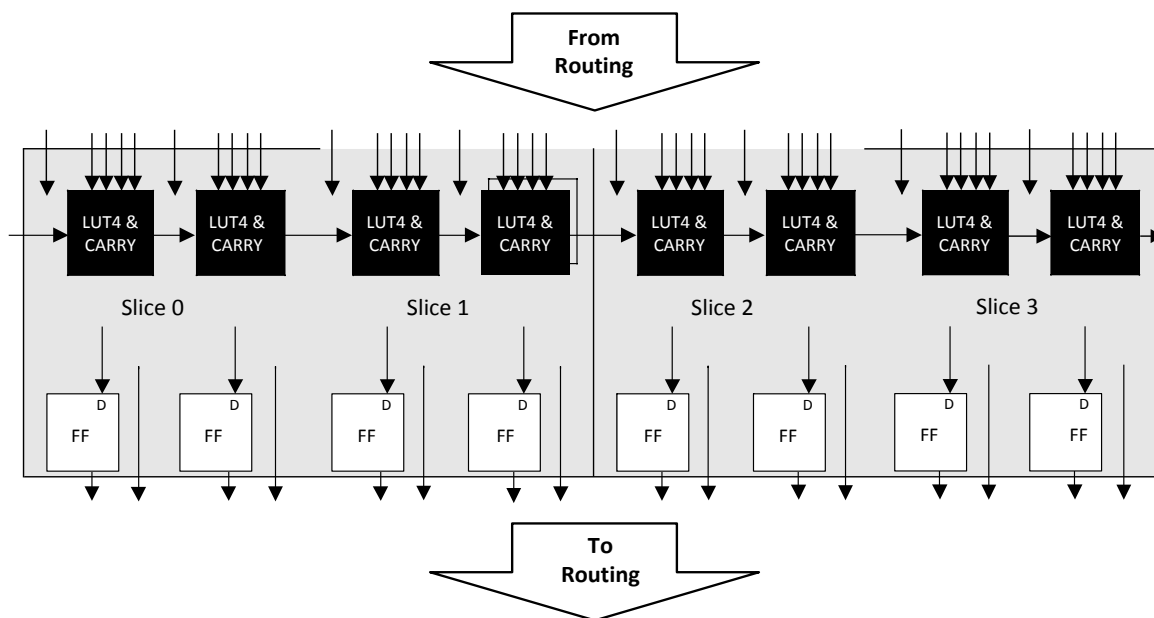


Figure 2.2. PFU Diagram

### 2.2.1. Slice

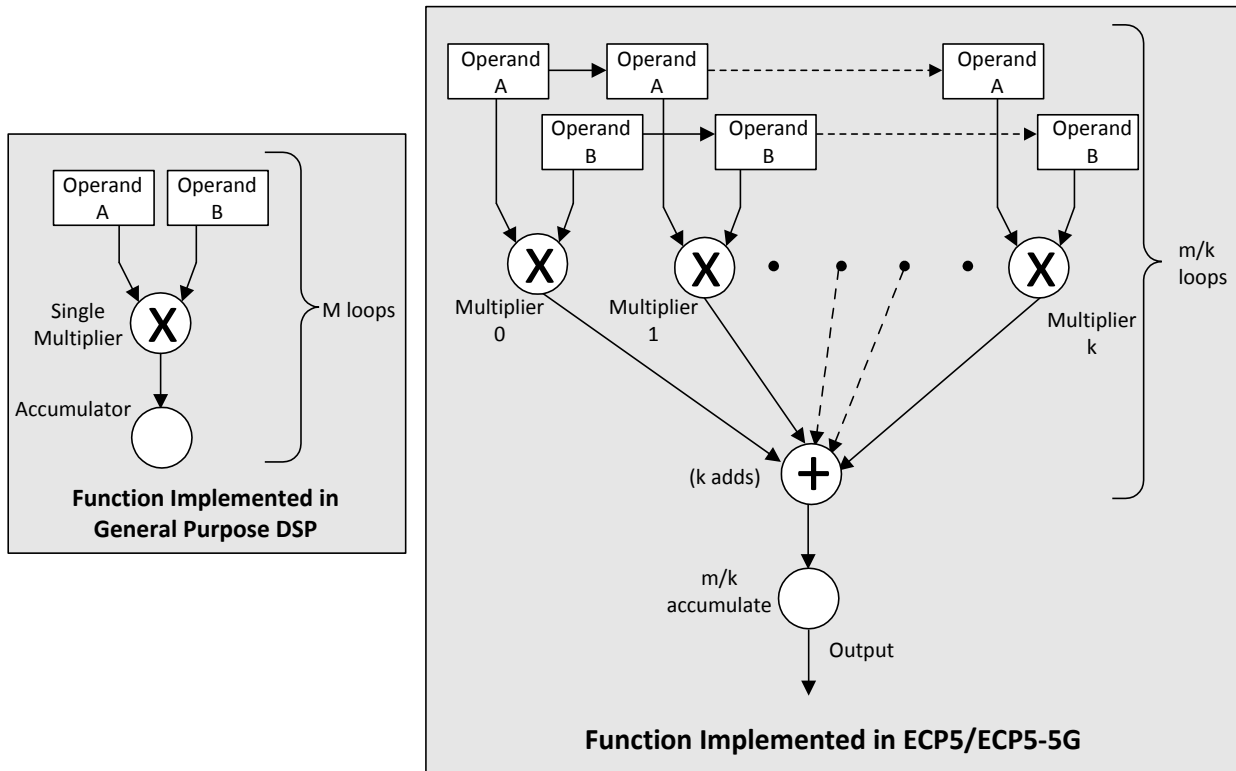
Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals, 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are five outputs, four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/ PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7 and LUT8. Table 2.2 and Figure 2.3 list the signals associated with all the slices. Figure 2.4 on page 16 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7 and LUT8.



**Figure 2.13. Comparison of General DSP and ECP5/ECP5-5G Approaches**

### 2.9.2. sysDSP Slice Architecture Features

The ECP5/ECP5-5G sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The ECP5/ECP5-5G sysDSP Slice supports many functions that include the following:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
  - Two dimensional (2D) symmetry mode – supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture
- Fully cascable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)
- Multiply (36x36 by cascading across two sysDSP slices)
- Multiply Accumulate (supports one 18x36 multiplier result accumulation or two 18x18 multiplier result accumulation)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
  - 3\*3 and 3\*5 – Internal DSP Slice support

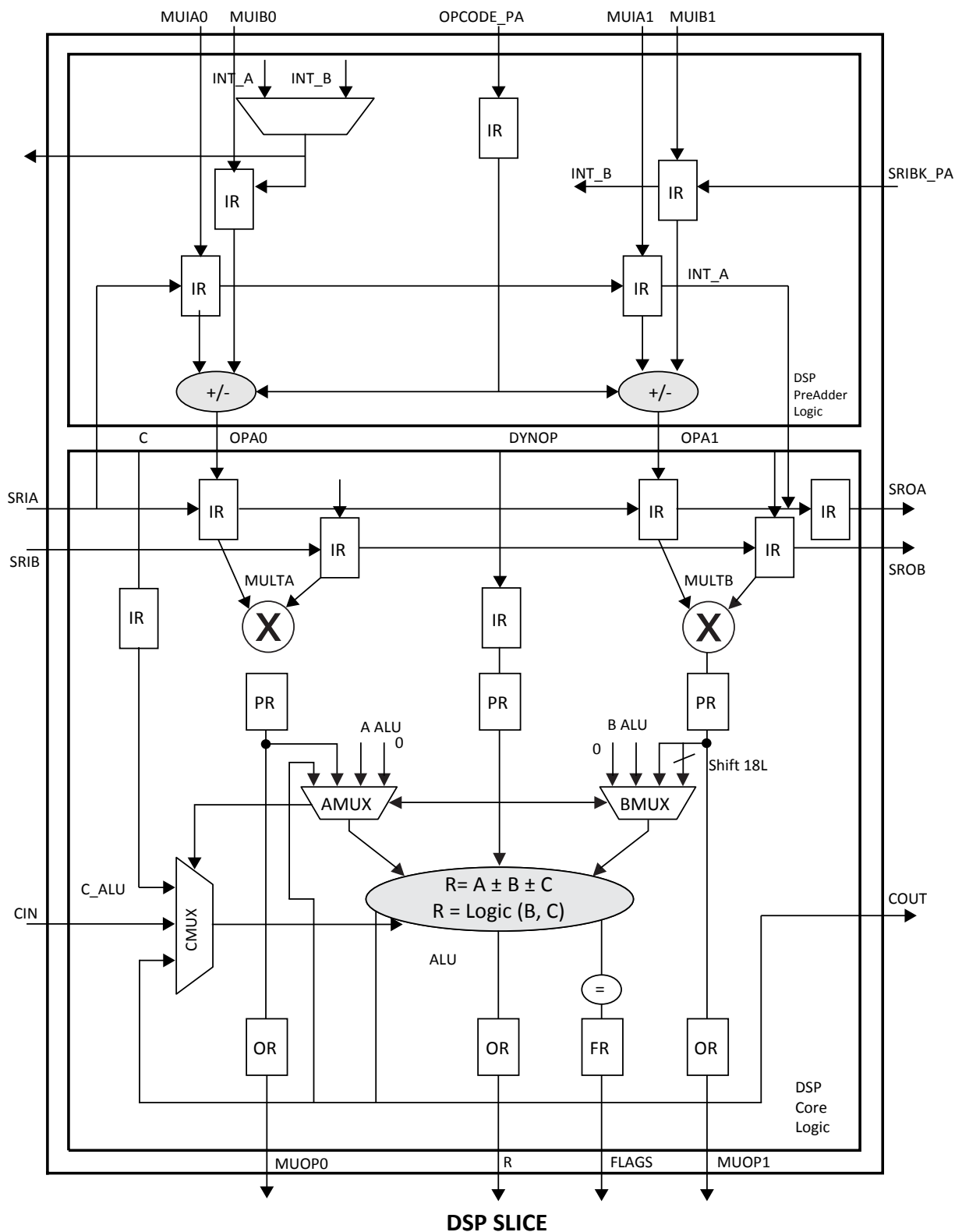


Figure 2.15. Detailed sysDSP Slice Diagram

### 2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in [DDR Memory Support](#) section on page 35.

**Table 2.8. Input Block Port Description**

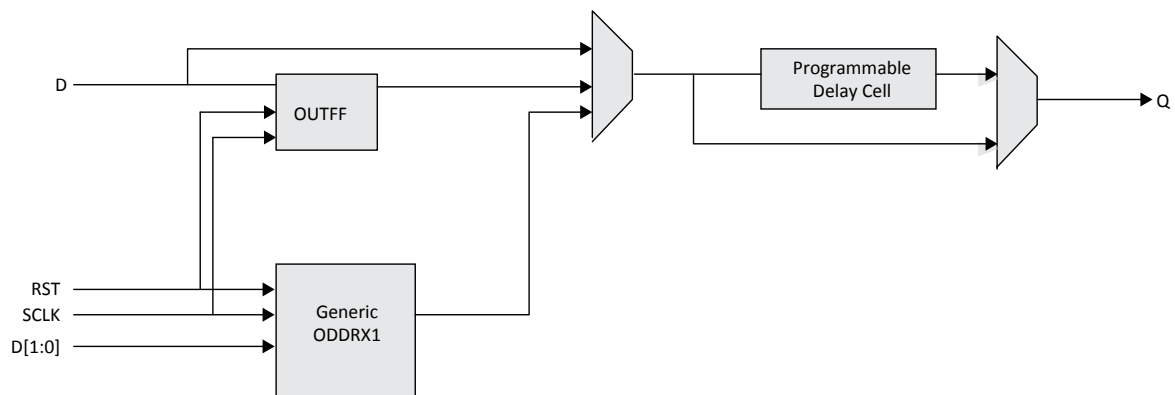
Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

### 2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in [Figure 2.19](#). The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).



**Figure 2.19. Output Register Block on Top Side**

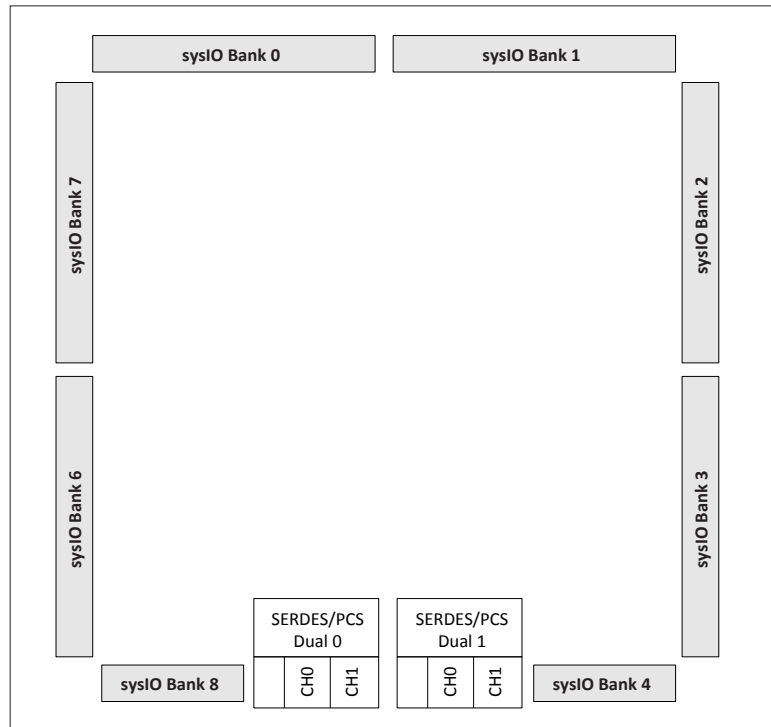


Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 <sup>2</sup>	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 <sup>2</sup>	x1	8b10b
SD-SDI (259M, 344M) <sup>1</sup>	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5	x1	NRZI/Scrambled
	1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	—	—
JESD204A/B	3125	x1	8b/10b

**Notes:**

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.



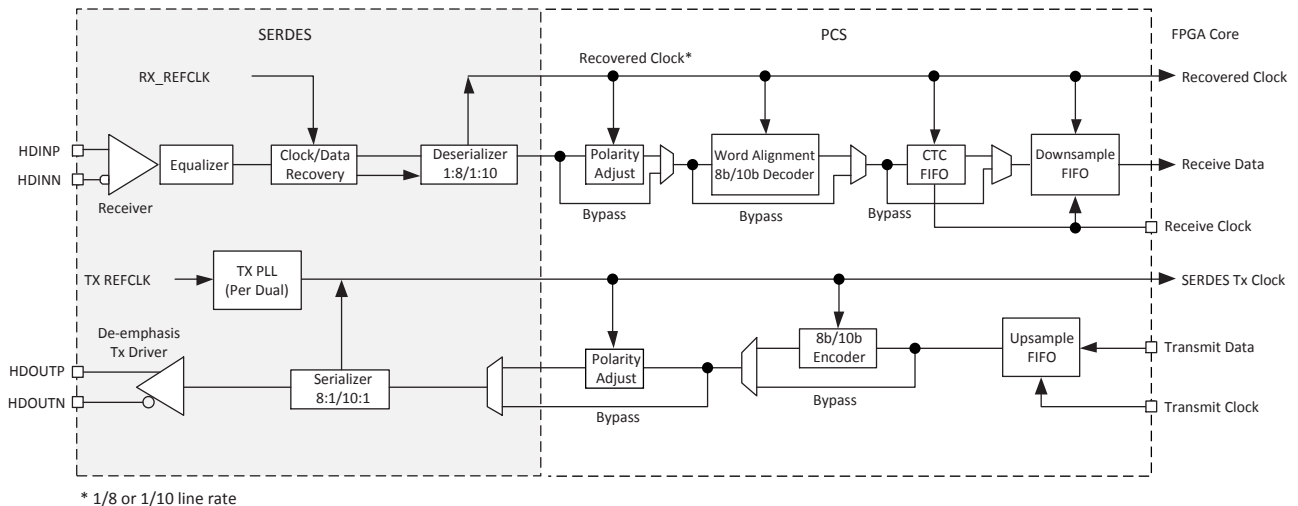
**Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices**

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

### 2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).



**Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block**

### 2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for more information.

## 3. DC and Switching Characteristics

### 3.1. Absolute Maximum Ratings

**Table 3.1. Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	−0.5	1.32	V
V <sub>CCA</sub>	Supply Voltage	−0.5	1.32	V
V <sub>CCAUX</sub> , V <sub>CCAUXA</sub>	Supply Voltage	−0.5	2.75	V
V <sub>CCIO</sub>	Supply Voltage	−0.5	3.63	V
—	Input or I/O Transient Voltage Applied	−0.5	3.63	V
V <sub>CCHRX</sub> , V <sub>CCHTX</sub>	SERDES RX/TX Buffer Supply Voltages	−0.5	1.32	V
—	Voltage Applied on SERDES Pins	−0.5	1.80	V
T <sub>A</sub>	Storage Temperature (Ambient)	−65	150	°C
T <sub>J</sub>	Junction Temperature	—	+125	°C

**Notes:**

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

### 3.2. Recommended Operating Conditions

**Table 3.2. Recommended Operating Conditions**

Symbol	Parameter		Min	Max	Unit
V <sub>CC</sub> <sup>2</sup>	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
V <sub>CCAUX</sub> <sup>2,4</sup>	Auxiliary Supply Voltage	—	2.375	2.625	V
V <sub>CCIO</sub> <sup>2,3</sup>	I/O Driver Supply Voltage	—	1.14	3.465	V
V <sub>REF</sub> <sup>1</sup>	Input Reference Voltage	—	0.5	1.0	V
t <sub>JCOM</sub>	Junction Temperature, Commercial Operation	—	0	85	°C
t <sub>JIND</sub>	Junction Temperature, Industrial Operation	—	−40	100	°C
<b>SERDES External Power Supply<sup>5</sup></b>					
V <sub>CCA</sub>	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V <sub>CCAUXA</sub>	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
V <sub>CCHRX</sub> <sup>6</sup>	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V <sub>CCHTX</sub>	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

**Notes:**

1. For correct operation, all supplies except V<sub>REF</sub> must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in [Table 3.4](#) on page 48.
4. V<sub>CCAUX</sub> ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
5. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for information on board considerations for SERDES power supplies.
6. V<sub>CCHRX</sub> is used for Rx termination. It can be biased to V<sub>cm</sub> if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

### 3.10. Supply Current (Standby)

Over recommended operating conditions.

**Table 3.8. ECP5/ECP5-5G Supply Current (Standby)**

Symbol	Parameter	Device	Typical	Unit
I <sub>CC</sub>	Core Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F	77	mA
		LFE5UM5G-25F	77	mA
		LFE5U-45F/ LFE5UM-45F	116	mA
		LFE5UM5G-45F	116	mA
		LFE5U-85F/ LFE5UM-85F	212	mA
		LFE5UM5G-85F	212	mA
I <sub>CCAUX</sub>	Auxiliary Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	16	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	17	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	26	mA
I <sub>CCIO</sub>	Bank Power Supply Current (Per Bank)	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	0.5	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	0.5	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	0.5	mA
I <sub>CCA</sub>	SERDES Power Supply Current (Per Dual)	LFE5UM-25F	11	mA
		LFE5UM5G-25F	12	mA
		LFE5UM-45F	9.5	mA
		LFE5UM5G-45F	11	mA
		LFE5UM-85F	9.5	mA
		LFE5UM5G-85F	11	mA

**Notes:**

- For further information on supply current, see the list of technical documentation in [Supplemental Information](#) section on page 102.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V<sub>CCIO</sub> or GND.
- Frequency 0 Hz.
- Pattern represents a “blank” configuration data file.
- T<sub>J</sub> = 85 °C, power supplies at nominal voltage.
- To determine the ECP5/ECP5-5G peak start-up current, use the Power Calculator tool in the Lattice Diamond Design Software.

**Table 3.10. ECP5-5G**

Symbol	Description	Typ	Max	Unit
<b>Standby (Power Down)</b>				
I <sub>CCA-SB</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	4	9.5	mA
I <sub>CCHRX-SB</sub> <sup>4</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	—	0.1	mA
I <sub>CCHTX-SB</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	—	0.9	mA
<b>Operating (Data Rate = 5 Gb/s)</b>				
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	58	67	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
<b>Operating (Data Rate = 3.2 Gb/s)</b>				
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	48	57	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
<b>Operating (Data Rate = 2.5 Gb/s)</b>				
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	44	53	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
<b>Operating (Data Rate = 1.25 Gb/s)</b>				
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	36	46	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA
<b>Operating (Data Rate = 270 Mb/s)</b>				
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	30	40	mA
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	8	10	mA

**Notes:**

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For I<sub>CCHRX-SB</sub>, during Standby, input termination on Rx are disabled.
5. For I<sub>CCHRX-OP</sub>, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

### 3.12. sysI/O Recommended Operating Conditions

**Table 3.11. sysI/O Recommended Operating Conditions**

Standard	V <sub>CCIO</sub>			V <sub>REF</sub> (V)		
	Min	Typ	Max	Min	Typ	Max
LVC MOS33 <sup>1</sup>	3.135	3.3	3.465	—	—	—
LVC MOS33D <sup>3</sup> Output	3.135	3.3	3.465	—	—	—
LVC MOS25 <sup>1</sup>	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 <sup>1</sup>	1.14	1.2	1.26	—	—	—
LVTTL33 <sup>1</sup>	3.135	3.3	3.465	—	—	—
SSTL15_I, _II <sup>2</sup>	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II <sup>2</sup>	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II <sup>2</sup>	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12 <sup>2</sup>	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input <sup>3, 5</sup>	1.425	1.5	1.575	—	—	—
LVDS25 <sup>1, 3</sup> Output	2.375	2.5	2.625	—	—	—
subLVDS <sup>3</sup> (Input only)	—	—	—	—	—	—
SLVS <sup>3</sup> (Input only)	—	—	—	—	—	—
LVDS25E <sup>3</sup> Output	2.375	2.5	2.625	—	—	—
MLVDS <sup>3</sup> Output	2.375	2.5	2.625	—	—	—
LVPECL33 <sup>1, 3</sup> Output	3.135	3.3	3.465	—	—	—
BLVDS25 <sup>1, 3</sup> Output	2.375	2.5	2.625	—	—	—
HSULD12D <sup>2, 3</sup>	1.14	1.2	1.26	—	—	—
SSTL135D_I, II <sup>2, 3</sup>	1.28	1.35	1.42	—	—	—
SSTL15D_I, II <sup>2, 3</sup>	1.43	1.5	1.57	—	—	—
SSTL18D_I <sup>1, 2, 3</sup> , II <sup>1, 2, 3</sup>	1.71	1.8	1.89	—	—	—

**Notes:**

1. For input voltage compatibility, refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#).
2. V<sub>REF</sub> is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V<sub>CCAUX</sub> power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V<sub>IH</sub> and V<sub>IL</sub>. It can also be implemented as LVC MOS12 with VCCIO at 1.2V, which would meet V<sub>IH</sub>/V<sub>IL</sub> spec on LVC MOS12.

### 3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

**Table 3.23. sysCLOCK PLL Timing**

Parameter	Descriptions	Conditions	Min	Max	Units
$f_{IN}$	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
$f_{OUT}$	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
$f_{VCO}$	PLL VCO Frequency	—	400	800	MHz
$f_{PFD}^3$	Phase Detector Input Frequency	—	10	400	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle	—	45	55	%
$t_{PH4}$	Output Phase Accuracy	—	–5	5	%
$t_{OPJIT}^1$	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
$t_{SPO}$	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
$t_W$	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
$t_{LOCK}^2$	PLL Lock-in Time	—	—	15	ms
$t_{UNLOCK}$	PLL Unlock Time	—	—	50	ns
$t_{IPJIT}$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{HI}$	Input Clock High Time	90% to 90%	0.5	—	ns
$t_{LO}$	Input Clock Low Time	10% to 10%	0.5	—	ns
$t_{RST}$	RST/ Pulse Width	—	1	—	ms
$t_{RSTREC}$	RST Recovery Time	—	1	—	ns
$t_{LOAD\_REG}$	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain “0” or	—	4	—	VCO cycles

**Notes:**

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PFD} > 10$  MHz. For  $f_{PFD} < 10$  MHz, the jitter numbers may not be met in certain conditions.

### 3.20. SERDES High-Speed Data Transmitter

**Table 3.24. Serial Output Timing and Levels**

Symbol	Description	Min	Typ	Max	Unit
V <sub>TX-DIFF-PP</sub>	Peak-Peak Differential voltage on selected amplitude <sup>1, 2</sup>	-25%	—	25%	mV, p-p
V <sub>TX-CM-DC</sub>	Output common mode voltage	—	V <sub>CCHTX</sub> / 2	—	mV, p-p
T <sub>TX-R</sub>	Rise time (20% to 80%)	50	—	—	ps
T <sub>TX-F</sub>	Fall time (80% to 20%)	50	—	—	ps
T <sub>TX-CM-AC-P</sub>	RMS AC peak common-mode output voltage	—	—	20	mV
Z <sub>TX-SE</sub>	Single ended output impedance for 50/75 Ω	-20%	50/75	20%	Ω
	Single ended output impedance for 6K Ω	-25%	6K	25%	Ω
RL <sub>TX-DIFF</sub>	Differential return loss (with package included) <sup>3</sup>	—	—	-10	dB
RL <sub>TX-COM</sub>	Common mode return loss (with package included) <sup>3</sup>	—	—	-6	dB

**Notes:**

1. Measured with 50 Ω Tx Driver impedance at V<sub>CCHTX</sub>±5%.
2. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for settings of Tx amplitude.
3. Return los = -10 dB (differential), -6 dB (common mode) for 100 MHz ≤ f ≤ 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

**Table 3.25. Channel Output Jitter**

Description	Frequency	Min	Typ	Max	Unit
Deterministic	5 Gb/s	—	—	TBD	UI, p-p
Random	5 Gb/s	—	—	TBD	UI, p-p
Total	5 Gb/s	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	—	—	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	—	—	0.24	UI, p-p

**Notes:**

1. Values are measured with PRBS 2<sup>7</sup>-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.
2. For ECP5-5G family devices only.

### 3.31. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

**Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications**

Symbol	Parameter		Min	Max	Unit
<b>POR, Configuration Initialization, and Wakeup</b>					
$t_{ICFG}$	Time from the Application of $V_{CC}$ , $V_{CCAUX}$ or $V_{CCIO8}$ (whichever is the last) to the rising edge of INITN	—	—	33	ms
$t_{VMC}$	Time from $t_{ICFG}$ to the valid Master CCLK	—	—	5	us
$t_{CZ}$	CCLK from Active to High-Z	—	—	300	ns
<b>Master CCLK</b>					
$f_{MCLK}$	Frequency	All selected frequencies	–20	20	%
$t_{MCLK-DC}$	Duty Cycle	All selected frequencies	40	60	%
<b>All Configuration Modes</b>					
$t_{PRGM}$	PROGRAMN LOW pulse accepted	—	110	—	ns
$t_{PRGMRJ}$	PROGRAMN LOW pulse rejected	—	—	50	ns
$t_{INITL}$	INITN LOW time	—	—	55	ns
$t_{DPPINT}$	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
$t_{IODISS}$	PROGRAMN LOW to I/O Disabled	—	—	150	ns
<b>Slave SPI</b>					
$f_{CCLK}$	CCLK input clock frequency	—	—	60	MHz
$t_{CCLKH}$	CCLK input clock pulsewidth HIGH	—	6	—	ns
$t_{CCLKL}$	CCLK input clock pulsewidth LOW	—	6	—	ns
$t_{STSU}$	CCLK setup time	—	1	—	ns
$t_{STH}$	CCLK hold time	—	1	—	ns
$t_{STCO}$	CCLK falling edge to valid output	—	—	10	ns
$t_{STOZ}$	CCLK falling edge to valid disable	—	—	10	ns
$t_{STOV}$	CCLK falling edge to valid enable	—	—	10	ns
$t_{SCS}$	Chip Select HIGH time	—	25	—	ns
$t_{SCSS}$	Chip Select setup time	—	3	—	ns
$t_{SCSH}$	Chip Select hold time	—	3	—	ns
<b>Master SPI</b>					
$f_{CCLK}$	Max selected CCLK output frequency	—	—	62	MHz
$t_{CCLKH}$	CCLK output clock pulse width HIGH	—	3.5	—	ns
$t_{CCLKL}$	CCLK output clock pulse width LOW	—	3.5	—	ns
$t_{STSU}$	CCLK setup time	—	5	—	ns
$t_{STH}$	CCLK hold time	—	1	—	ns
$t_{CSSPI}$	INITN HIGH to Chip Select LOW	—	100	200	ns
$t_{CFGX}$	INITN HIGH to first CCLK edge	—	—	150	ns
<b>Slave Serial</b>					
$f_{CCLK}$	CCLK input clock frequency	—	—	66	MHz
$t_{SSCH}$	CCLK input clock pulse width HIGH	—	5	—	ns
$t_{SSCL}$	CCLK input clock pulse width LOW	—	5	—	ns
$t_{SUSCDI}$	CCLK setup time	—	0.5	—	ns
$t_{HS CDI}$	CCLK hold time	—	1.5	—	ns



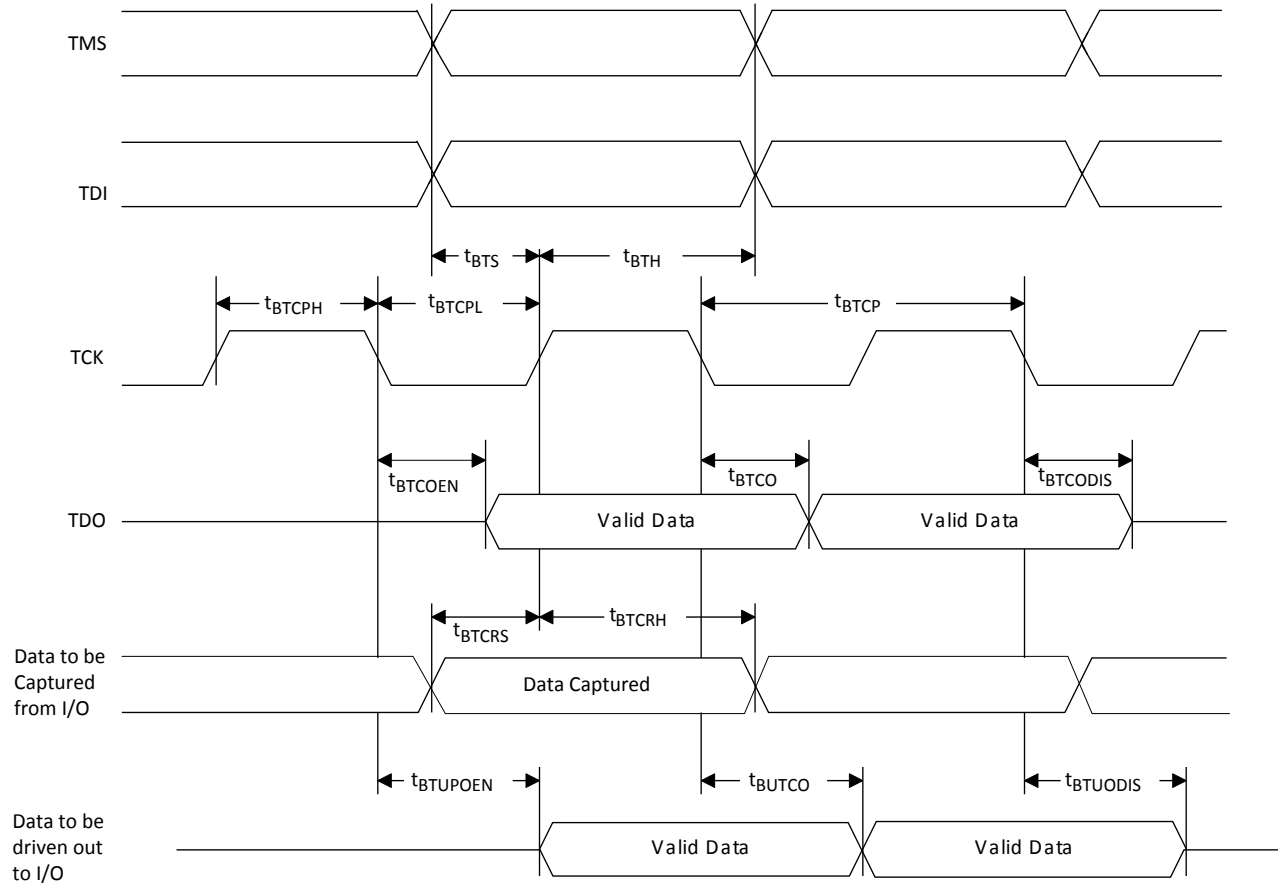
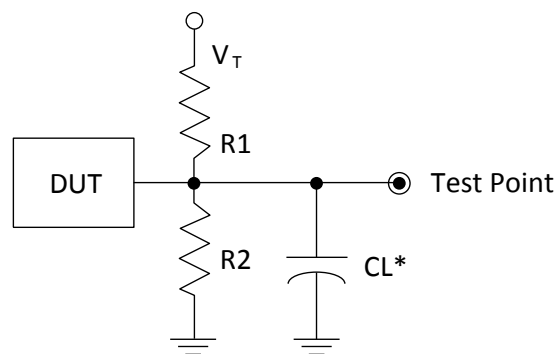


Figure 3.23. JTAG Port Timing Waveforms

### 3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.



\*CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTTL and LVCMOS Standards

**Table 3.44. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>	Timing Ref.	V <sub>T</sub>
LVTTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V <sub>CCIO</sub> /2	V <sub>CCIO</sub>
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V <sub>OH</sub> – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V <sub>OL</sub> + 0.10	V <sub>CCIO</sub>

**Note:** Output test conditions for all other interfaces are determined by the respective standards.

## LFE5UM5G - XX - X XXXXX X

Device Family  
LFE5UM5G (ECP5-5G FPGA  
with SERDES)

Logic Capacity  
25F = 25K LUTs  
45F = 45K LUTs  
85F = 85K LUTs

Speed  
8 = Fastest

Grade  
C = Commercial  
I = Industrial

Package  
MG285 = 285-ball csfBGA  
BG381 = 381-ball caBGA  
BG554 = 554-ball caBGA  
BG756 = 756-ball caBGA

## 5.2. Ordering Part Numbers

### 5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	-6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	-7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	-8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	-6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	-7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	-8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	-6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	-7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	-8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	-6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	-7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	-8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	-6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	-7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	-8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	No

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes

## 5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	–6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	–7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	–8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	–6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	–7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	–8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	–6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	–7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	–8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	–6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	–7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	–8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	–6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	–7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	–8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	No

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclk).
			Modified section heading to XXAU/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.