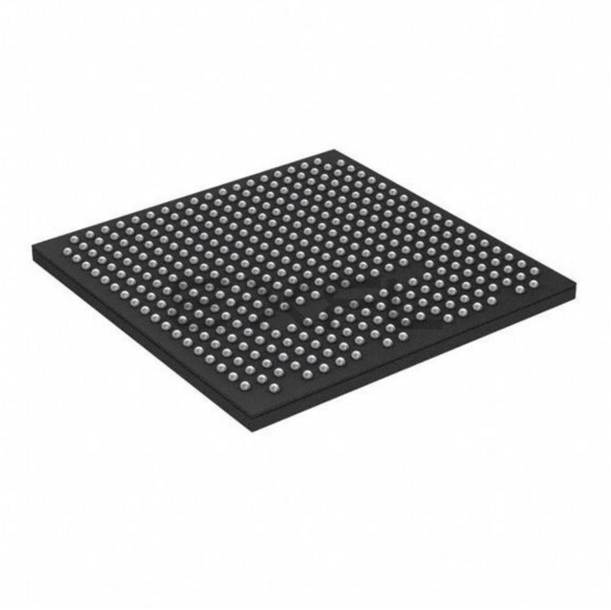
Lattice Semiconductor Corporation - LFE5UM-45F-6BG381I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	203
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-6bg381i

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Contents

  - Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 18/15 I, II
  - HSUL12
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
  - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
  - Shared bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
  - Soft Error Detect – Embedded hard macro
  - Soft Error Correction – Without stopping user operation
  - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - On-chip oscillator for initialization and general use
  - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	**LFE5UM-25 LFE5UM5G-25**	**LFE5UM-45 LFE5UM5G-45**	**LFE5UM-85 LFE5UM5G-85**	**LFE5U-12**	**LFE5U-25**	**LFE5U-45**	**LFE5U-85**
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels / IO Count)							
256 caBGA (14 x 14 mm², 0.8 mm)	—	—	—	0/197	0/197	0/197	—
285 csfBGA (10 x 10 mm², 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm², 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm², 0.8 mm)	—	4/245	4/259	—	—	0/245	0/259
756 caBGA (27 x 27 mm², 0.8 mm)	—	—	4/365	—	—	—	0/365

2.7. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

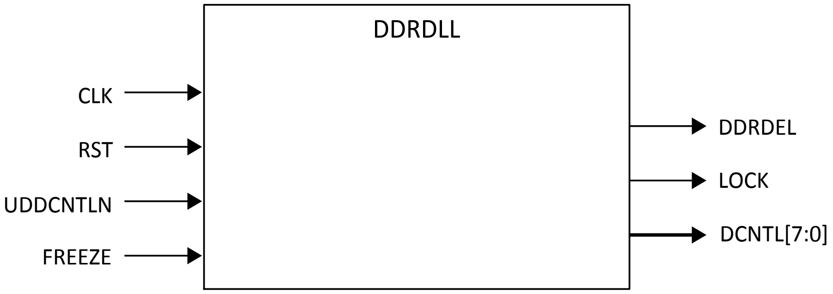


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

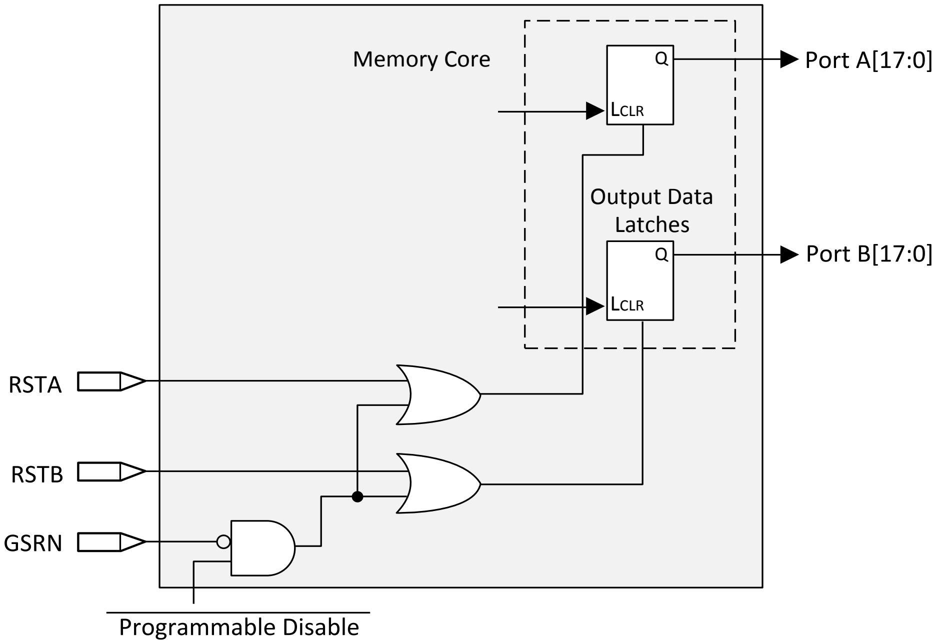


Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

2.9. sysDSP™ Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

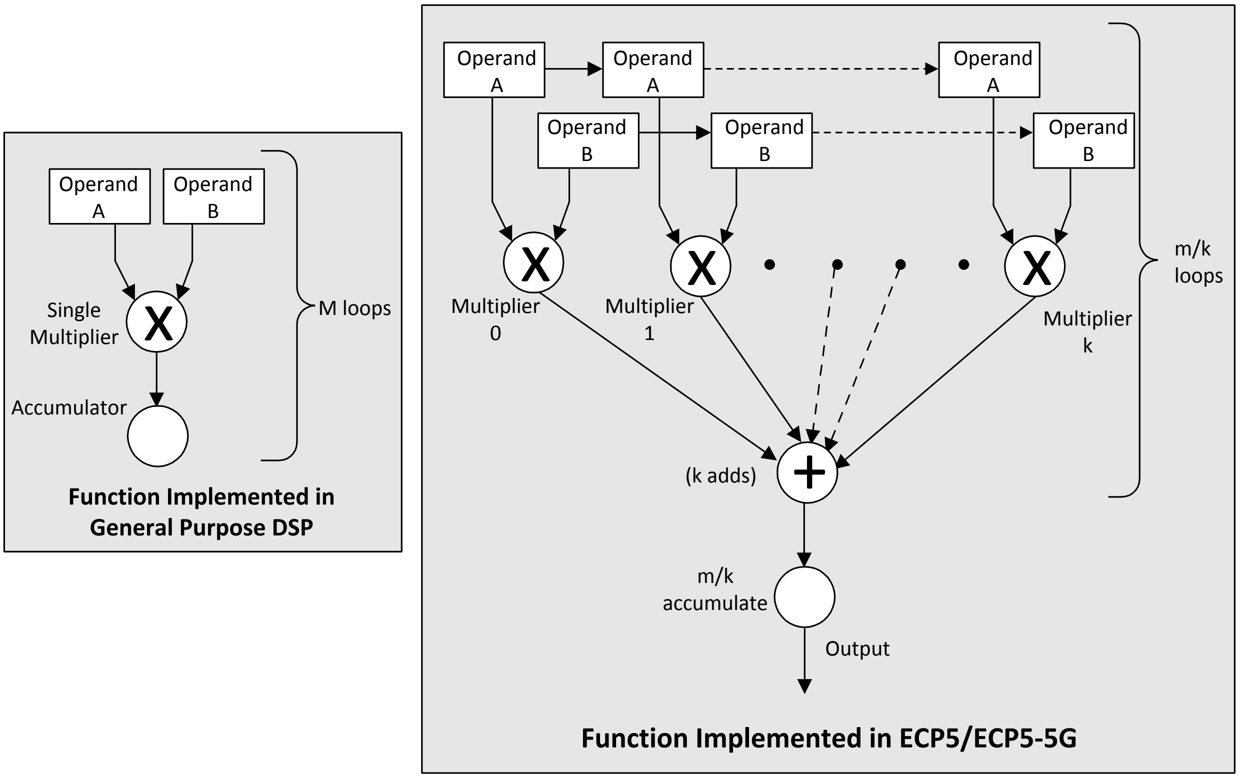


Figure 2.13. Comparison of General DSP and ECP5/ECP5-5G Approaches

2.9.2. sysDSP Slice Architecture Features

The ECP5/ECP5-5G sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The ECP5/ECP5-5G sysDSP Slice supports many functions that include the following:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
  - Two dimensional (2D) symmetry mode – supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture
- Fully cascadable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)
- Multiply (36x36 by cascading across two sysDSP slices)
- Multiply Accumulate (supports one 18x36 multiplier result accumulation or two 18x18 multiplier result accumulation)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
  - 3*3 and 3*5 – Internal DSP Slice support

In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note**: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

2.10. **Programmable I/O Cells**

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

3.11. SERDES Power Supply Requirements[1,2,3]

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
$I_{CCA\text{-}SB}$	V_{CCA} Power Supply Current (Per Channel)	4	9.5	mA
$I_{CCHRX\text{-}SB}$[4]	V_{CCHRX}, Input Buffer Current (Per Channel)	—	0.1	mA
$I_{CCHTX\text{-}SB}$	V_{CCHTX}, Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 3.125 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	43	54	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	40	50	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	34	43	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	28	38	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For $I_{CCHRX\text{-}SB}$, during Standby, input termination on Rx are disabled.
5. For $I_{CCHRX\text{-}OP}$, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

Table 3.10. ECP5-5G

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
$I_{CCA\text{-}SB}$	V_{CCA} Power Supply Current (Per Channel)	4	9.5	mA
$I_{CCHRX\text{-}SB}$[4]	V_{CCHRX}, Input Buffer Current (Per Channel)	—	0.1	mA
$I_{CCHTX\text{-}SB}$	V_{CCHTX}, Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 5 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	58	67	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 3.2 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	48	57	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	44	53	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	36	46	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
$I_{CCA\text{-}OP}$	V_{CCA} Power Supply Current (Per Channel)	30	40	mA
$I_{CCHRX\text{-}OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX\text{-}OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For $I_{CCHRX\text{-}SB}$, during Standby, input termination on Rx are disabled.
5. For $I_{CCHRX\text{-}OP}$, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3, 5]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.14. sysI/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.13. LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	±100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	±10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver outputs shorted to each other	—	—	12	mA

Note: On the left and right sides of the device, this specification is valid only for V_{CCIO} = 2.5 V or 3.3 V.

3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

Table 3.18. Input to SLVS

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.

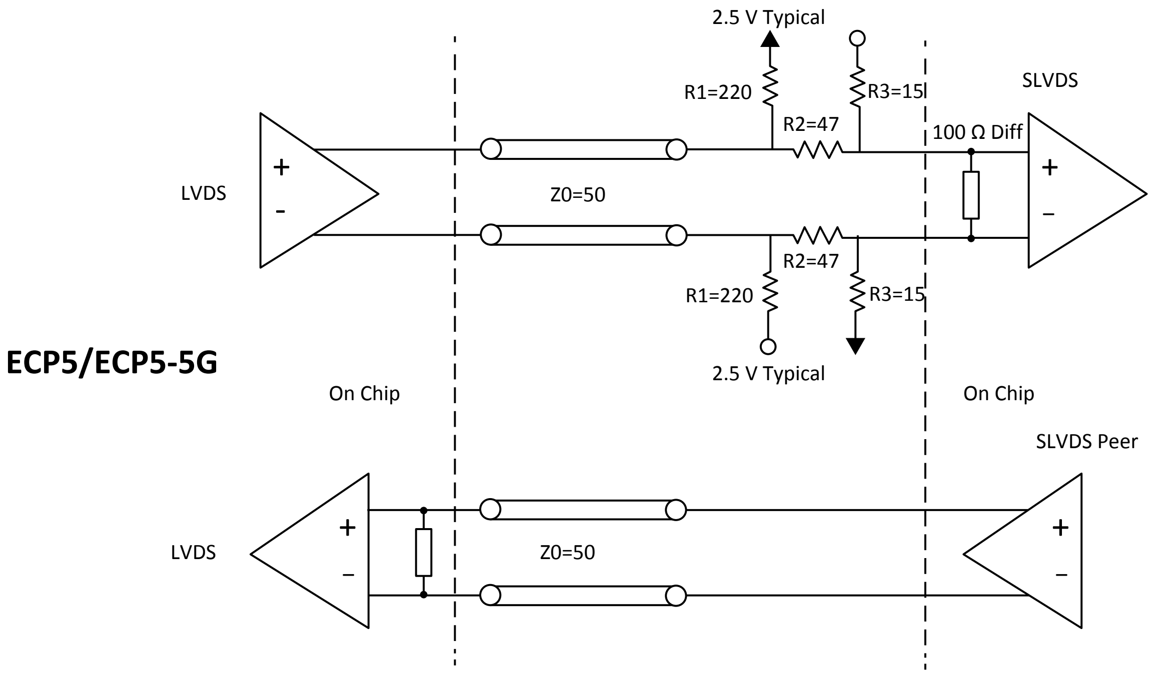


Figure 3.5. SLVS Interface

Table 3.20. Register-to-Register Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	441	MHz
32-Bit Decoder	441	MHz
64-Bit Decoder	332	MHz
4:1 Mux	441	MHz
8:1 Mux	441	MHz
16:1 Mux	441	MHz
32:1 Mux	441	MHz
8-Bit Adder	441	MHz
16-Bit Adder	441	MHz
64-Bit Adder	441	MHz
16-Bit Counter	384	MHz
32-Bit Counter	317	MHz
64-Bit Counter	263	MHz
64-Bit Accumulator	288	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	214	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	441	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	441	MHz
DSP Functions		
9 x 9 Multiplier (All Registers)	225	MHz
18 x 18 Multiplier (All Registers)	225	MHz
36 x 36 Multiplier (All Registers)	225	MHz
18 x 18 Multiply-Add/Sub (All Registers)	225	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	225	MHz

Notes:

1. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

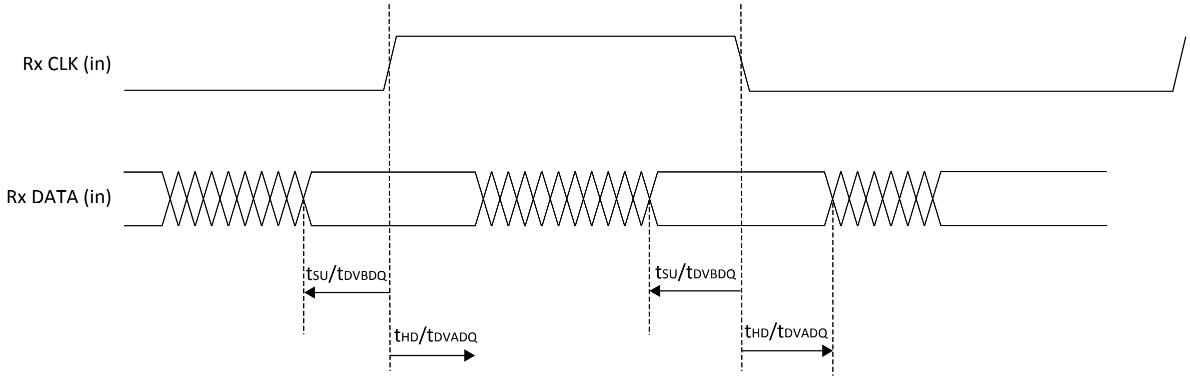


Figure 3.6. Receiver RX.CLK.Centered Waveforms

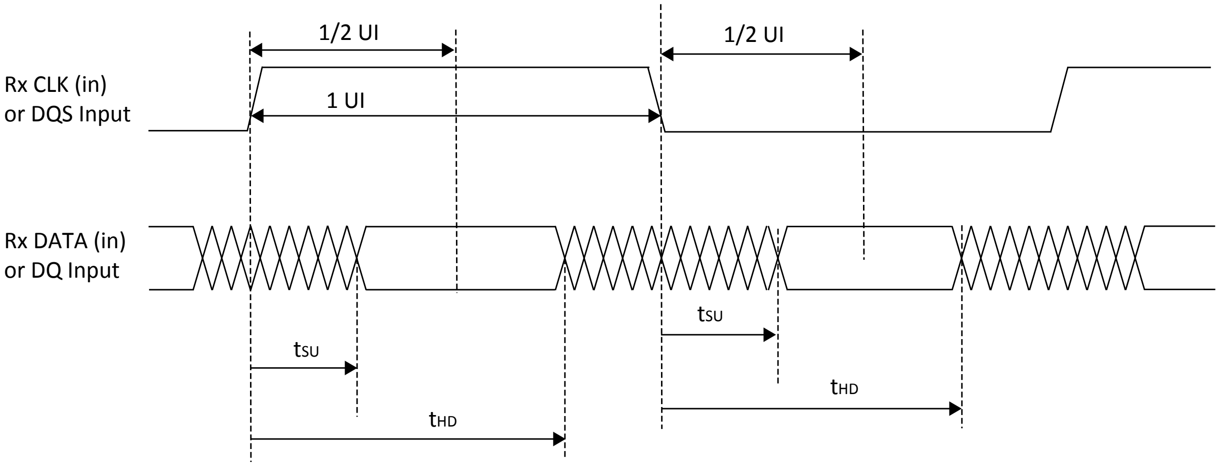


Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

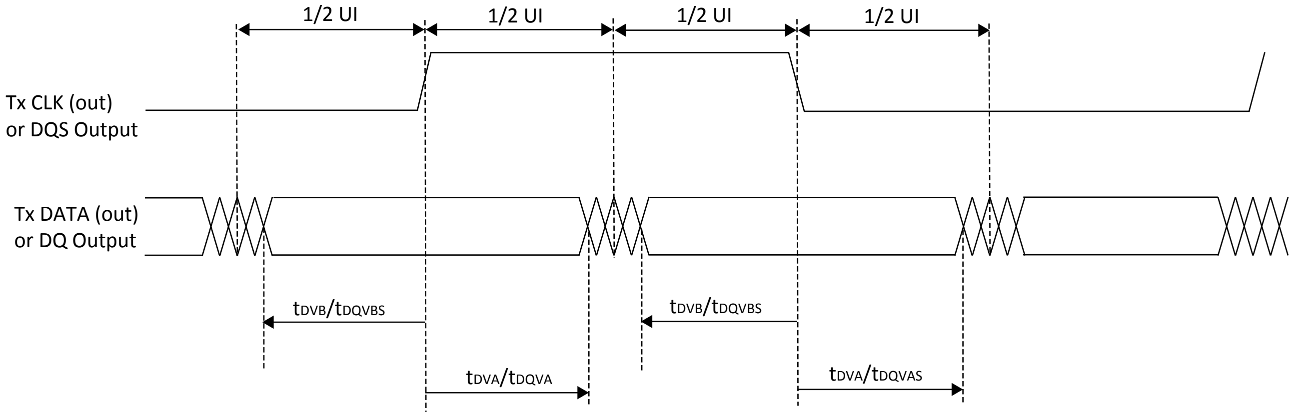


Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

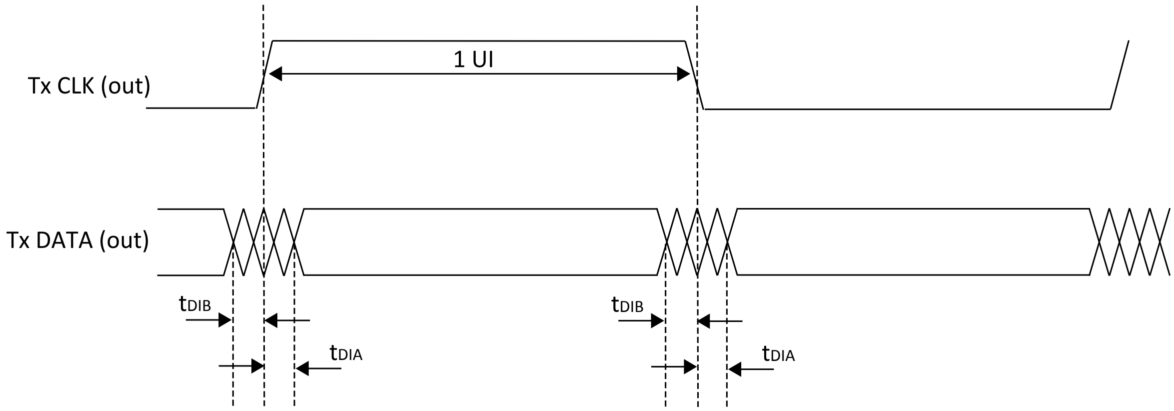
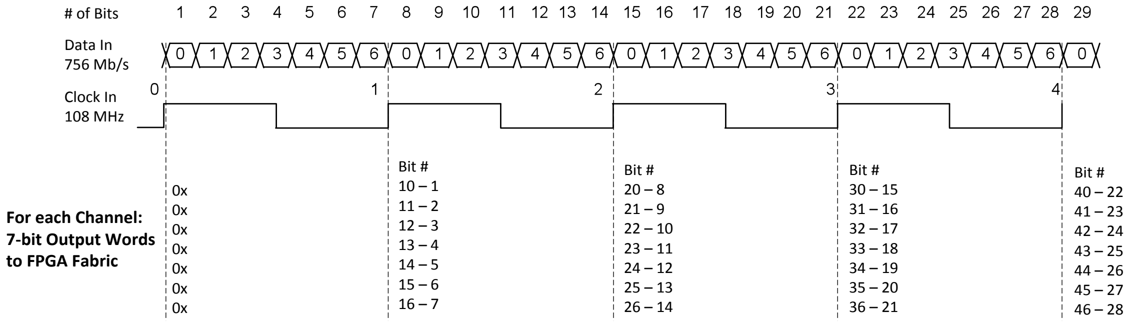


Figure 3.9. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter – Shown for one LVDS Channel

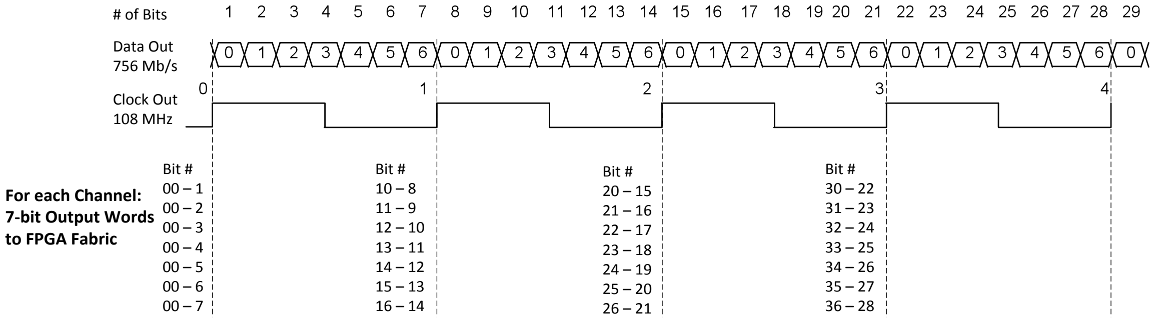


Figure 3.10. DDRX71 Video Timing Waveforms

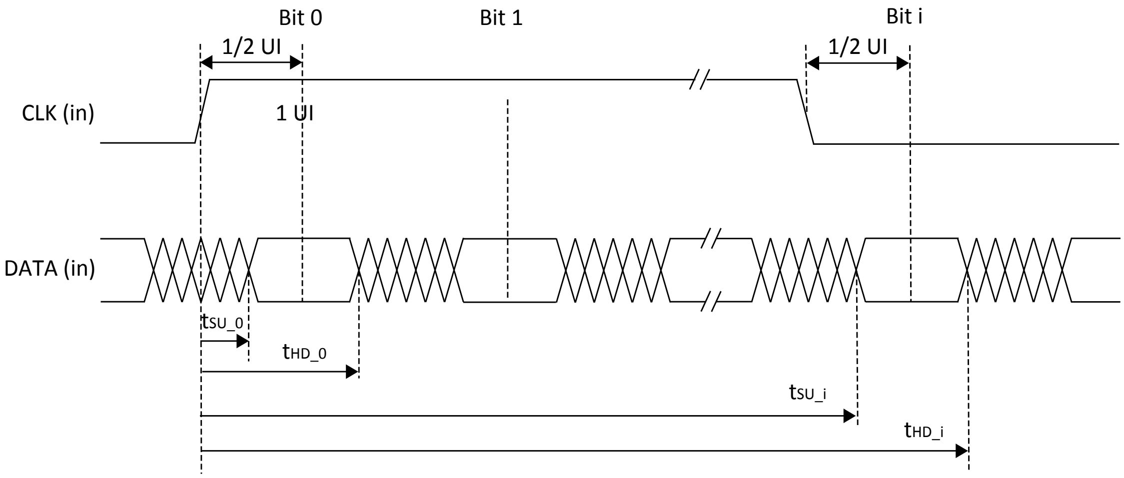


Figure 3.11. Receiver DDRX71_RX Waveforms

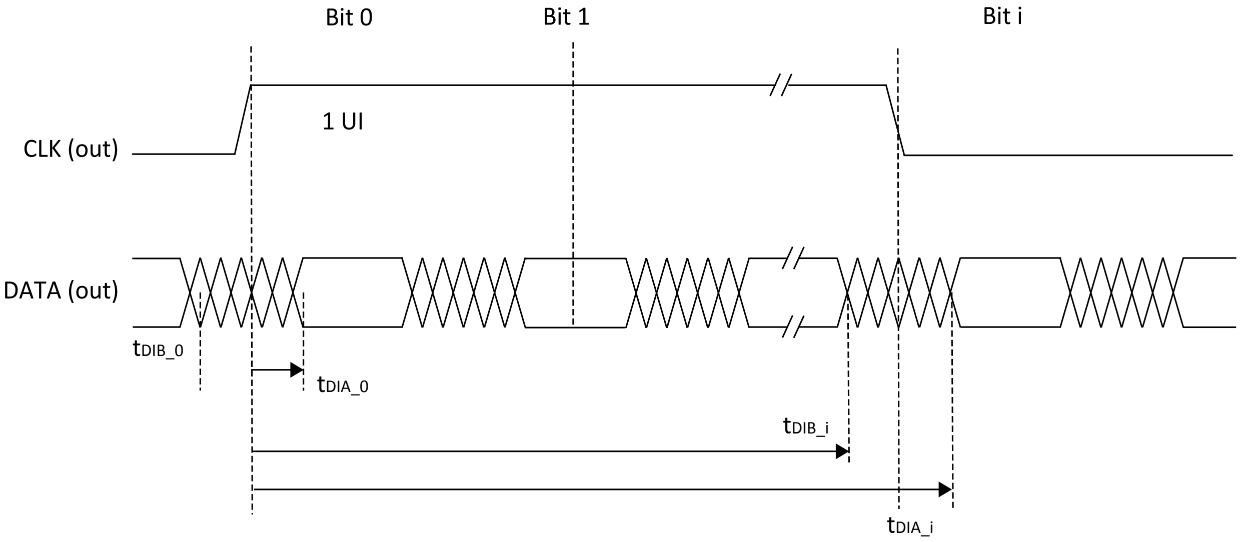


Figure 3.12. Transmitter DDRX71_TX Waveforms

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity	150	—	1760	mV, p-p
$V_{RX\text{-}IN}$	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX\text{-}CM\text{-}DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX\text{-}CM\text{-}ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX\text{-}RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
$RL_{RX\text{-}RL}$	Return loss (without package)	—	—	–10	dB

Notes:

1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Notes:

1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

Table 3.44. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	$V_{OL} + 0.10$	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4.3.2. LFE5U

Pin Information Summary		LFE5U-12			LFE5U-25			LFE5U-45				LFE5U-85			
Pin Type		**256 caBGA**	**285 csfBGA**	**381 caBGA**	**256 caBGA**	**285 csfBGA**	**381 caBGA**	**256 caBGA**	**285 csfBGA**	**381 caBGA**	**554 caBGA**	**285 csfBG**	**381 caBGA**	**554 caBGA**	**756 caBG**
General Purpose Inputs/Outputs per Bank	Bank 0	24	6	24	24	6	24	24	6	27	32	6	27	32	56
	Bank 1	32	6	32	32	6	32	32	6	33	40	6	33	40	48
	Bank 2	32	21	32	32	21	32	32	21	32	32	21	34	32	48
	Bank 3	32	28	32	32	28	32	32	28	33	48	28	33	48	64
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	14	24
	Bank 6	32	26	32	32	26	32	32	26	33	48	26	33	48	64
	Bank 7	32	18	32	32	18	32	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13	13	13	13	13	13
Total Single-Ended User		197	118	197	197	118	197	197	118	203	245	118	205	259	365
VCC		6	13	20	6	13	20	6	13	20	24	13	20	24	36
VCCAUX (Core)		2	3	4	2	3	4	2	3	4	9	3	4	9	8
VCCIO	Bank 0	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 1	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 2	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 3	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	2	2
	Bank 6	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 7	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 8	1	2	2	1	2	2	1	2	2	2	2	2	2	2
TAP		4	4	4	4	4	4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated		7	7	7	7	7	7	7	7	7	7	7	7	7	7
GND		27	123	99	27	123	99	27	123	99	198	123	99	198	267
NC		0	1	26	0	1	26	0	1	26	33	1	26	33	29
Reserved		0	4	6	0	4	6	0	4	6	12	4	6	12	12
Total Balls		256	285	381	256	285	381	256	285	381	554	285	381	554	756
High Speed Differential Input / Output Pairs		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8
		Bank	16/8	14/7	16/8	16/8	14/7	16/8	16/8	14/7	16/8	24/12	14/7	16/8	24/1
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	16/8	13/6	16/8	16/8	13/6	16/8	16/8	13/6	16/8	24/12	13/6	16/8	24/1
		Bank	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
Total High Speed		64/32	45/27	64/32	64/32	45/27	64/32	64/32	45/27	64/32	80/40	45/27	65/33	80/40	112/
DQS Groups (> 11 pins in group)		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	2	1	2	2	1	2	2	1	2	2	1	2	2
		Bank	2	2	2	2	2	2	2	2	2	3	2	2	3
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	2	2	2	2	2	2	2	2	2	3	2	2	3
		Bank	2	1	2	2	1	2	2	1	2	2	1	2	2
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
Total DQS Groups		8	6	8	8	6	8	8	6	8	10	6	8	10	14

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes

5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	–6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	–7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	–8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	–6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	–7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	–8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	–6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	–7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	–8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	–6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	–7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	–8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	–6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	–7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	–8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	No

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	No
LFE5UM-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes
LFE5UM5G-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM5G-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM5G-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM5G-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM5G-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM5G-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM5G-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM5G-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM5G-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes