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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	245
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-6bg554i

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- Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
 - DDR registers in I/O cells
 - Dedicated read/write levelling functionality
 - Dedicated gearing logic
 - Source synchronous standards support
 - ADC/DAC, 7:1 LVDS, XGMII
 - High Speed ADC/DAC devices
 - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
 - On-chip termination
 - LVTTTL and LVCMOS 33/25/18/15/12
 - SSTL 18/15 I, II
 - HSUL12
 - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
 - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
 - Shared bank for configuration I/Os
 - SPI boot flash interface
 - Dual-boot images supported
 - Slave SPI
 - TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
 - Soft Error Detect – Embedded hard macro
 - Soft Error Correction – Without stopping user operation
 - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
 - IEEE 1149.1 and IEEE 1532 compliant
 - Reveal Logic Analyzer
 - On-chip oscillator for initialization and general use
 - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U- 12	LFE5U- 25	LFE5U- 45	LFE5U- 85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels / IO Count)							
256 caBGA (14 x 14 mm ² , 0.8 mm)	—	—	—	0/197	0/197	0/197	—
285 csfBGA (10 x 10 mm ² , 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm ² , 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm ² , 0.8 mm)	—	4/245	4/259	—	—	0/245	0/259
756 caBGA (27 x 27 mm ² , 0.8 mm)	—	—	4/365	—	—	—	0/365

2. Architecture

2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in [Figure 2.1](#) on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG™ ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.

A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. [Table 2.3](#) lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#).

2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

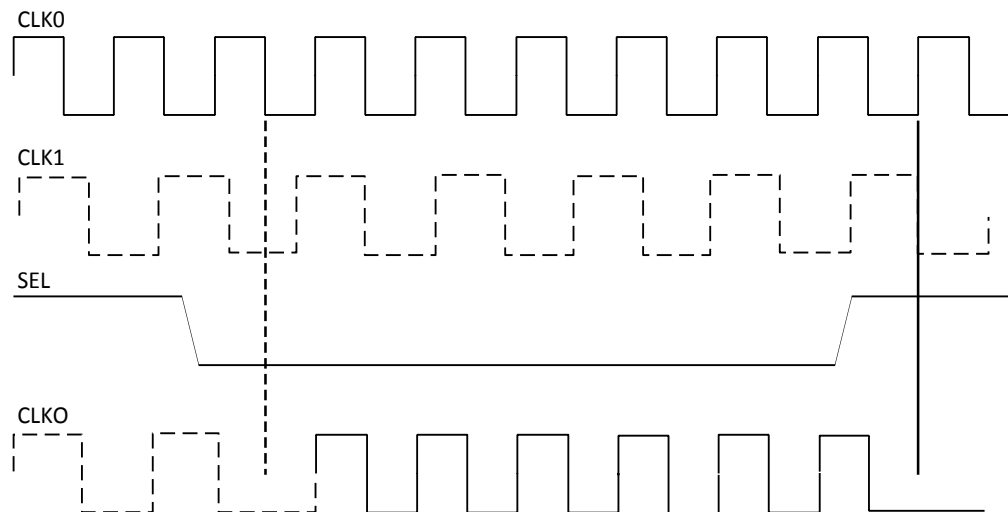


Figure 2.7. DCS Waveforms

2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90°)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

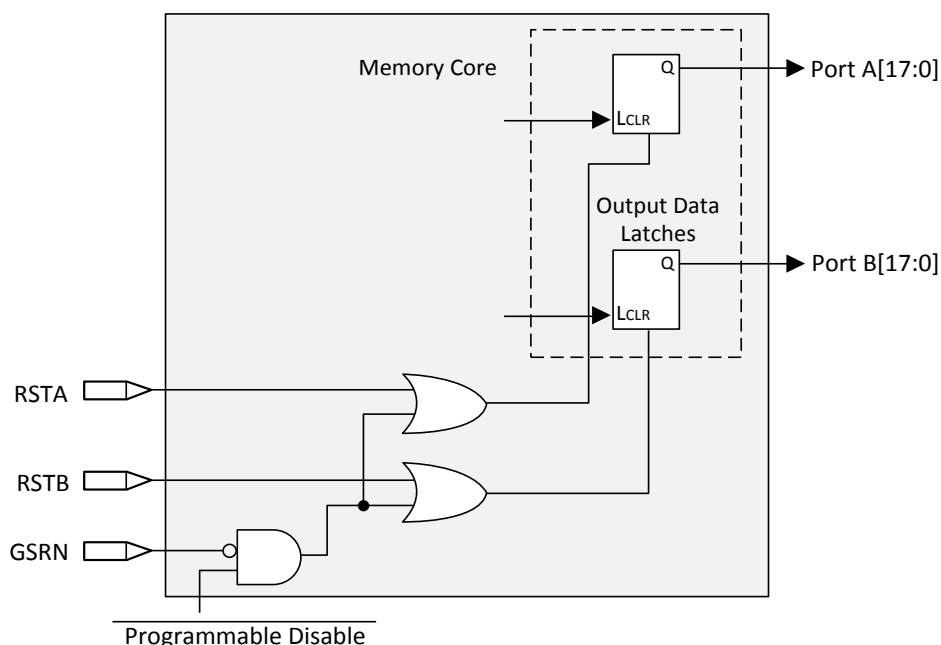


Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in [Supplemental Information](#) section on page 102.

2.9. sysDSP™ Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

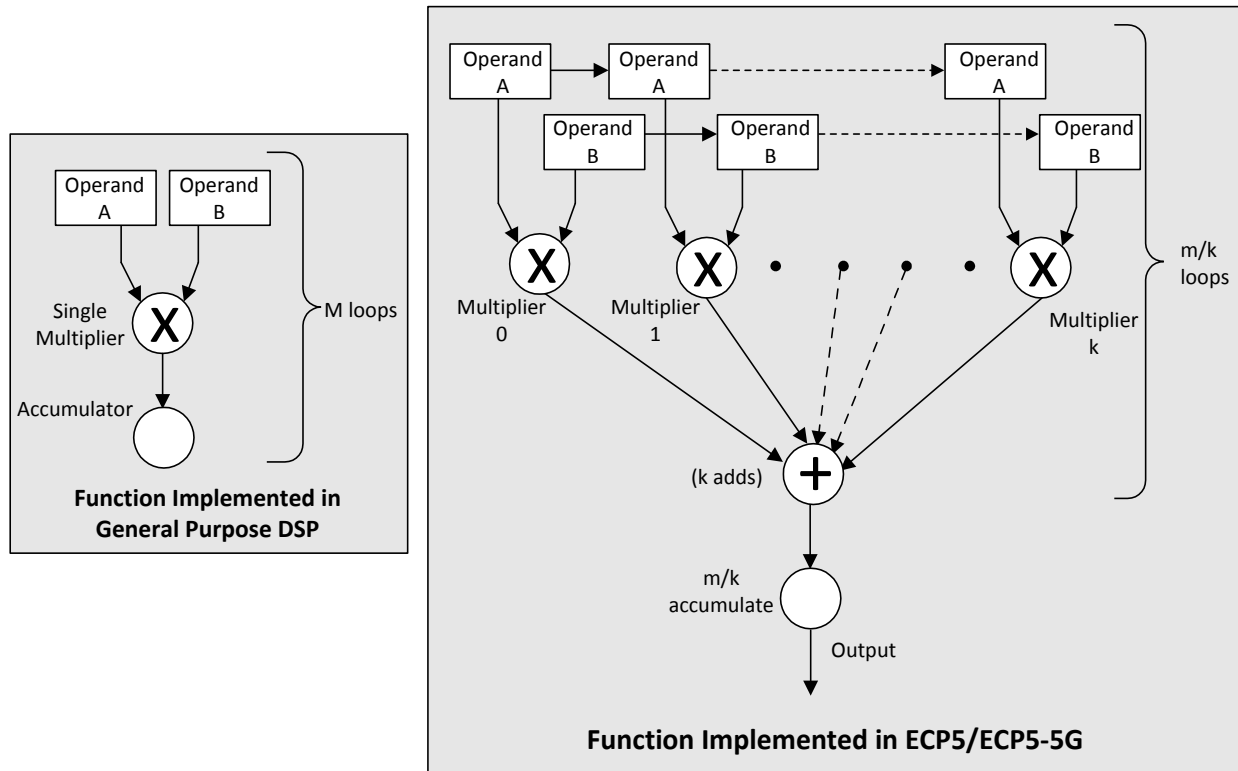


Figure 2.13. Comparison of General DSP and ECP5/ECP5-5G Approaches

2.9.2. sysDSP Slice Architecture Features

The ECP5/ECP5-5G sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The ECP5/ECP5-5G sysDSP Slice supports many functions that include the following:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
 - Odd mode – Filter with Odd number of taps
 - Even mode – Filter with Even number of taps
 - Two dimensional (2D) symmetry mode – supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture
- Fully cascable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)
- Multiply (36x36 by cascading across two sysDSP slices)
- Multiply Accumulate (supports one 18x36 multiplier result accumulation or two 18x18 multiplier result accumulation)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
 - Odd mode – Filter with Odd number of taps
 - Even mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
 - 3*3 and 3*5 – Internal DSP Slice support

2.11. PIO

The PIO contains three blocks: an input register block, output register block, and tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

2.11.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers to shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers samples the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The top side of the device supports IDDRX1 gearing function. For more information on gearing function, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

Figure 2.17 shows the input register block for the PIOs on the top edge.

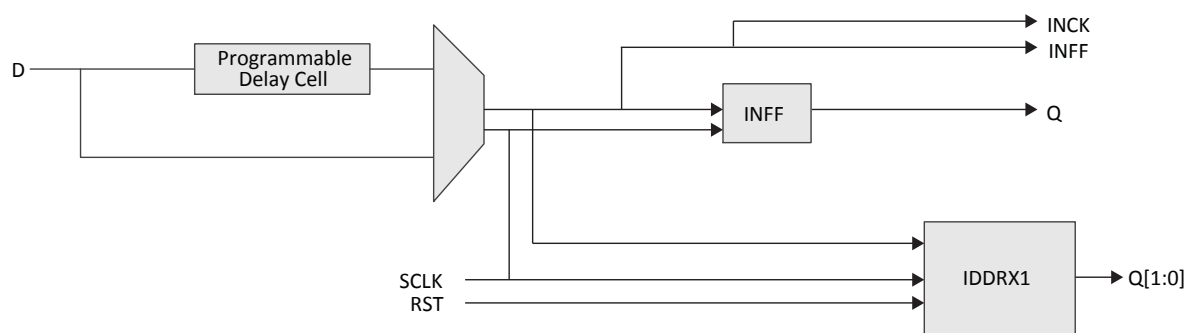
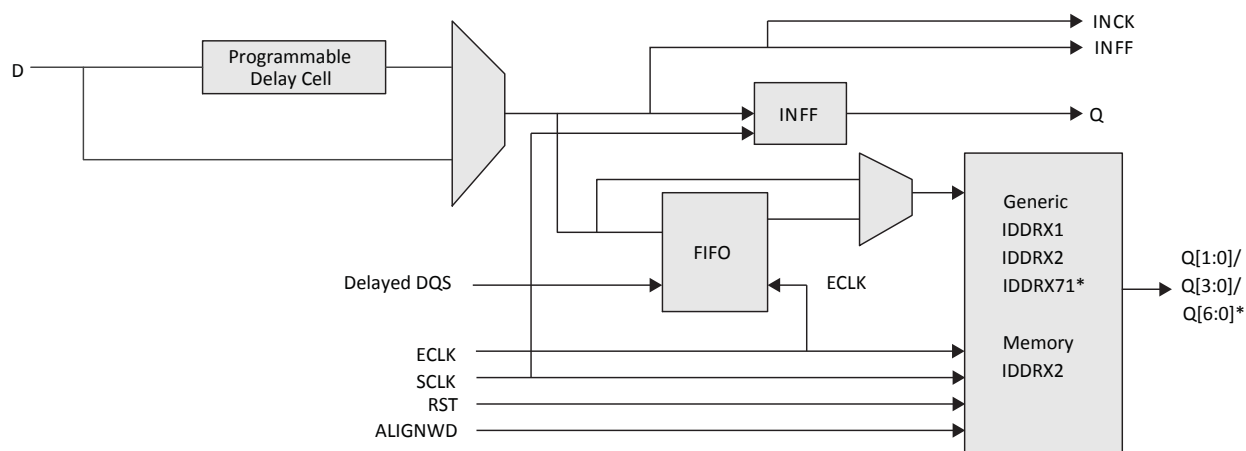


Figure 2.17. Input Register Block for PIO on Top Side of the Device

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

Figure 2.18. Input Register Block for PIO on Left and Right Side of the Device

2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in [DDR Memory Support](#) section on page 35.

Table 2.8. Input Block Port Description

Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in [Figure 2.19](#). The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

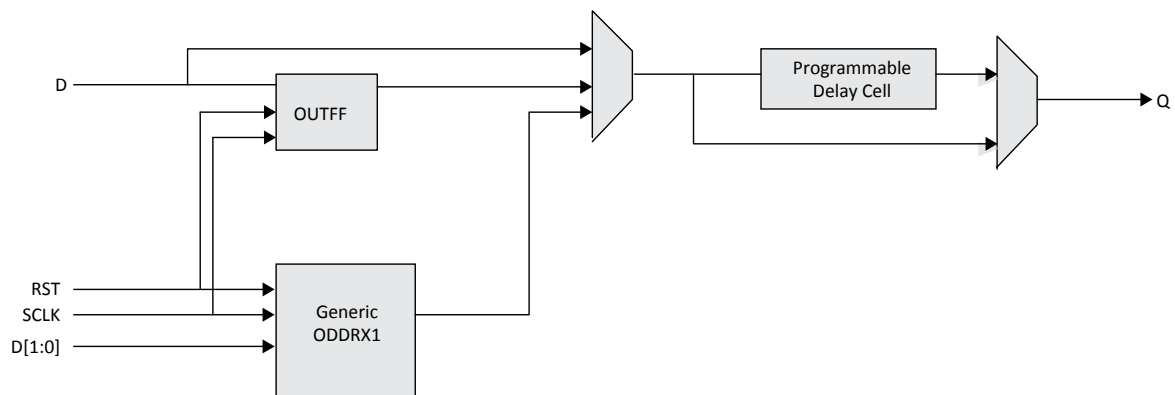


Figure 2.19. Output Register Block on Top Side

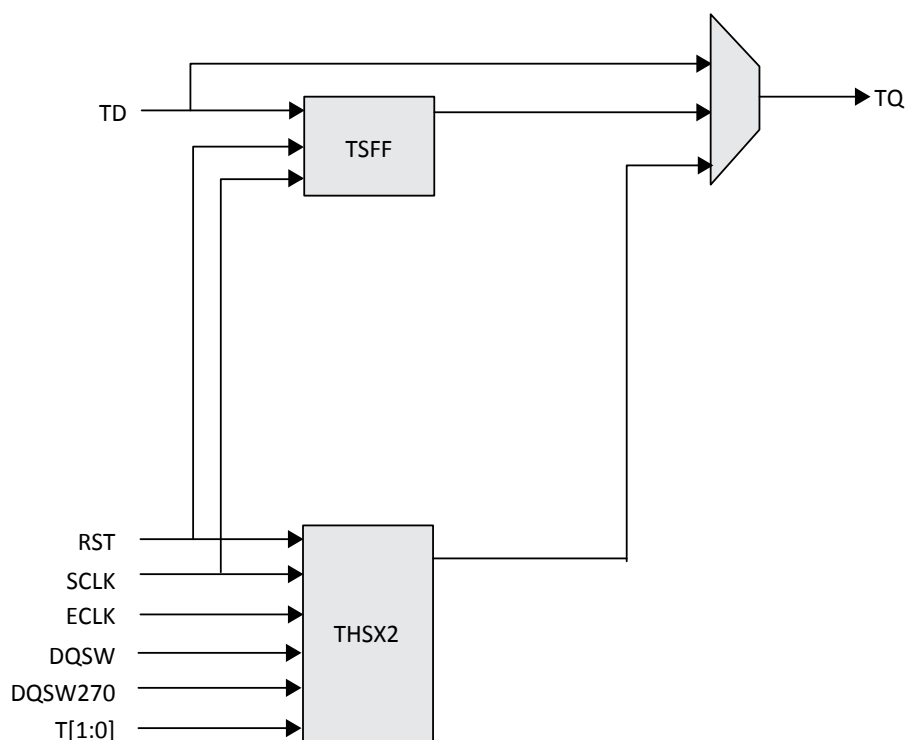


Figure 2.22. Tristate Register Block on Left and Right Sides

Table 2.10. Tristate Block Port Description

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR Register
RST	Input	Reset to the Tristate Block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.13. DDR Memory Support

2.13.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in [Figure 2.23](#) on page 36. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as "virtual" VCCIO, by driving these pins to HIGH, with the user connecting these pins to VCCIO power supply. These connections create "soft" connections to VCCIO thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter			Min	Typ	Max	Unit
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC} , V_{CCAUX} , and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC} , and V_{CCAUX})	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other V_{CCIOs} do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when V_{CC} , V_{CCAUX} , and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies (V_{CC} and/or V_{CCAUX}) is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the V_{IH} voltage requirement of the SPI Flash. For LFE5UM/LFE5UM5G devices, it is required to power up V_{CCA} , before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \leq V_{IN} \leq V_{IH} \text{ (Max)}$	—	—	± 1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \leq V_{IN} < V_{CCIO}$	—	—	± 1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5 \text{ V}$	—	18	—	mA

Notes:

1. V_{CC} , V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the I_{DK} current can exceed ± 1 mA.

3.10. Supply Current (Standby)

Over recommended operating conditions.

Table 3.8. ECP5/ECP5-5G Supply Current (Standby)

Symbol	Parameter	Device	Typical	Unit
I _{CC}	Core Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F	77	mA
		LFE5UM5G-25F	77	mA
		LFE5U-45F/ LFE5UM-45F	116	mA
		LFE5UM5G-45F	116	mA
		LFE5U-85F/ LFE5UM-85F	212	mA
		LFE5UM5G-85F	212	mA
I _{CCAUX}	Auxiliary Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	16	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	17	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	26	mA
I _{CCIO}	Bank Power Supply Current (Per Bank)	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	0.5	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	0.5	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	0.5	mA
I _{CCA}	SERDES Power Supply Current (Per Dual)	LFE5UM-25F	11	mA
		LFE5UM5G-25F	12	mA
		LFE5UM-45F	9.5	mA
		LFE5UM5G-45F	11	mA
		LFE5UM-85F	9.5	mA
		LFE5UM5G-85F	11	mA

Notes:

- For further information on supply current, see the list of technical documentation in [Supplemental Information](#) section on page 102.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 Hz.
- Pattern represents a “blank” configuration data file.
- T_J = 85 °C, power supplies at nominal voltage.
- To determine the ECP5/ECP5-5G peak start-up current, use the Power Calculator tool in the Lattice Diamond Design Software.

3.11. SERDES Power Supply Requirements^{1,2,3}

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I _{CCA-SB}	V _{CCA} Power Supply Current (Per Channel)	4	9.5	mA
I _{CCHRX-SB} ⁴	V _{CCHRX} , Input Buffer Current (Per Channel)	—	0.1	mA
I _{CCHTX-SB}	V _{CCHTX} , Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 3.125 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	43	54	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	40	50	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	34	43	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	28	38	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For I_{CCHRX-SB}, during Standby, input termination on Rx are disabled.
5. For I_{CCHRX-OP}, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVC MOS33 ¹	3.135	3.3	3.465	—	—	—
LVC MOS33D ³ Output	3.135	3.3	3.465	—	—	—
LVC MOS25 ¹	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 ¹	1.14	1.2	1.26	—	—	—
LVTTL33 ¹	3.135	3.3	3.465	—	—	—
SSTL15_I, _II ²	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II ²	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12 ²	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input ^{3, 5}	1.425	1.5	1.575	—	—	—
LVDS25 ^{1, 3} Output	2.375	2.5	2.625	—	—	—
subLVDS ³ (Input only)	—	—	—	—	—	—
SLVS ³ (Input only)	—	—	—	—	—	—
LVDS25E ³ Output	2.375	2.5	2.625	—	—	—
MLVDS ³ Output	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1, 3} Output	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1, 3} Output	2.375	2.5	2.625	—	—	—
HSULD12D ^{2, 3}	1.14	1.2	1.26	—	—	—
SSTL135D_I, II ^{2, 3}	1.28	1.35	1.42	—	—	—
SSTL15D_I, II ^{2, 3}	1.43	1.5	1.57	—	—	—
SSTL18D_I ^{1, 2, 3} , II ^{1, 2, 3}	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVC MOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

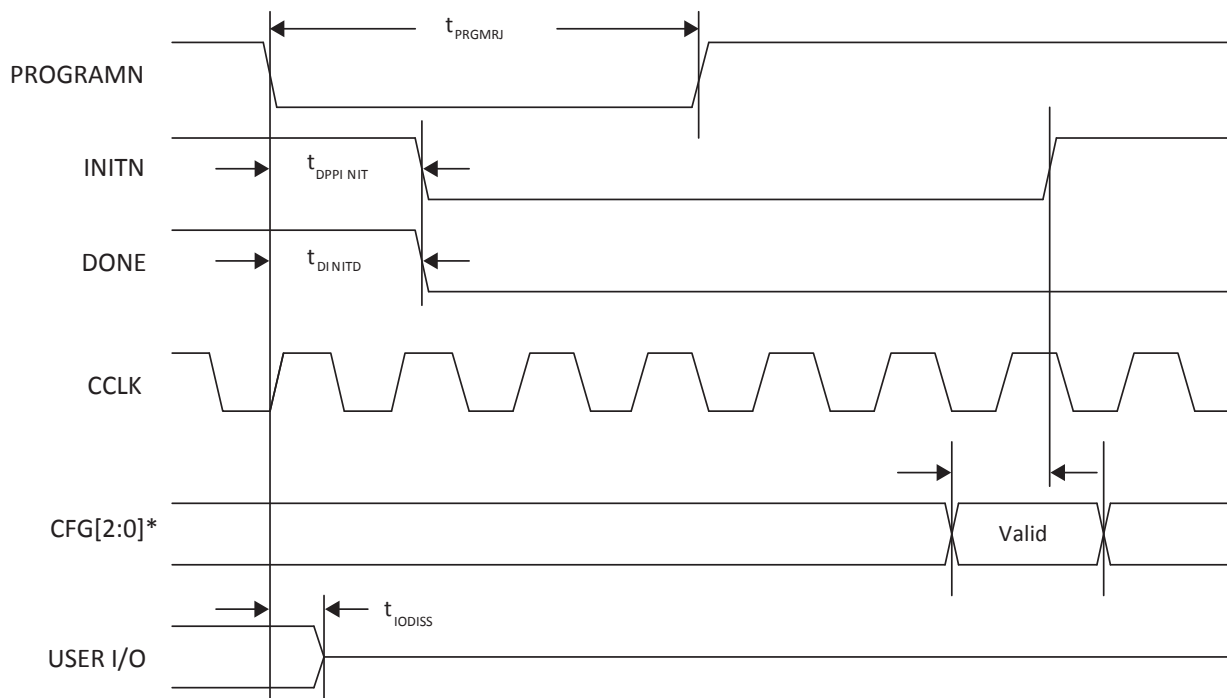
Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks									
Primary Clock									
f _{MAX_PRI}	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
t _{SKEW_PRI}	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
Edge Clock									
f _{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
t _{SKEW_EDGE}	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
Generic SDR Input									
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL									
t _{CO}	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
t _{SU}	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
t _H	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL									
t _{COPLL}	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
t _{SU_DEPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns

3.31. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications

Symbol	Parameter		Min	Max	Unit
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC} , V_{CCAUX} or V_{CCIO8} (whichever is the last) to the rising edge of INITN	—	—	33	ms
t_{VMC}	Time from t_{ICFG} to the valid Master CCLK	—	—	5	us
t_{CZ}	CCLK from Active to High-Z	—	—	300	ns
Master CCLK					
f_{MCLK}	Frequency	All selected frequencies	–20	20	%
$t_{MCLK-DC}$	Duty Cycle	All selected frequencies	40	60	%
All Configuration Modes					
t_{PRGM}	PROGRAMN LOW pulse accepted	—	110	—	ns
t_{PRGMRJ}	PROGRAMN LOW pulse rejected	—	—	50	ns
t_{INITL}	INITN LOW time	—	—	55	ns
t_{DPPINT}	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	150	ns
Slave SPI					
f_{CCLK}	CCLK input clock frequency	—	—	60	MHz
t_{CCLKH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{CCLKL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{STSU}	CCLK setup time	—	1	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{STCO}	CCLK falling edge to valid output	—	—	10	ns
t_{STOZ}	CCLK falling edge to valid disable	—	—	10	ns
t_{STOV}	CCLK falling edge to valid enable	—	—	10	ns
t_{SCS}	Chip Select HIGH time	—	25	—	ns
t_{SCSS}	Chip Select setup time	—	3	—	ns
t_{SCSH}	Chip Select hold time	—	3	—	ns
Master SPI					
f_{CCLK}	Max selected CCLK output frequency	—	—	62	MHz
t_{CCLKH}	CCLK output clock pulse width HIGH	—	3.5	—	ns
t_{CCLKL}	CCLK output clock pulse width LOW	—	3.5	—	ns
t_{STSU}	CCLK setup time	—	5	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{CSSPI}	INITN HIGH to Chip Select LOW	—	100	200	ns
t_{CFGX}	INITN HIGH to first CCLK edge	—	—	150	ns
Slave Serial					
f_{CCLK}	CCLK input clock frequency	—	—	66	MHz
t_{SSCH}	CCLK input clock pulse width HIGH	—	5	—	ns
t_{SSCL}	CCLK input clock pulse width LOW	—	5	—	ns
t_{SUSCDI}	CCLK setup time	—	0.5	—	ns
$t_{HS CDI}$	CCLK hold time	—	1.5	—	ns



*The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

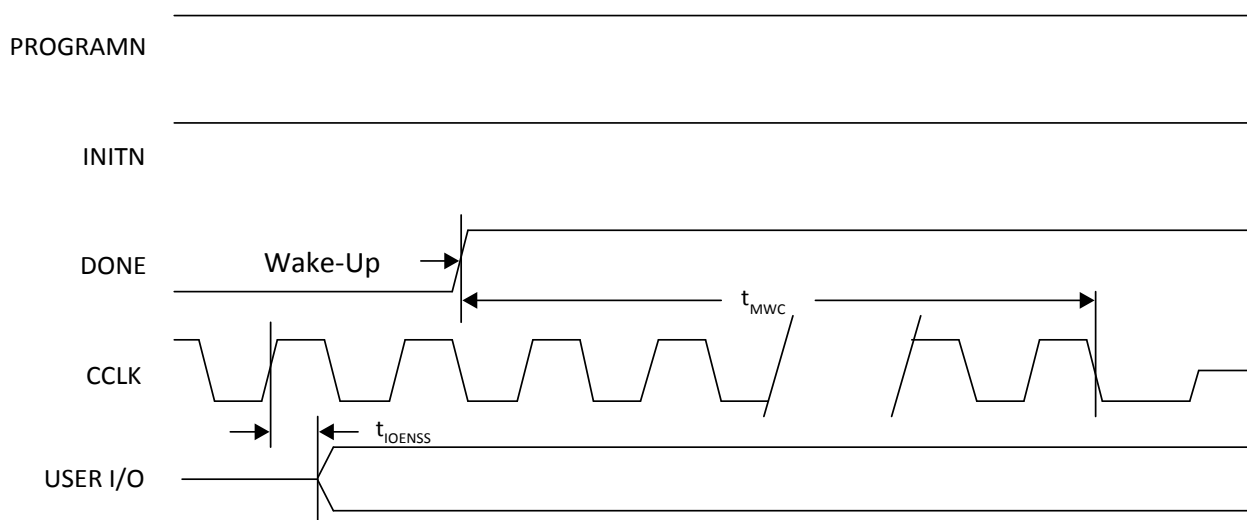


Figure 3.21. Wake-Up Timing

4.3.2. LFE5U

Pin Information Summary		LFE5U-12			LFE5U-25			LFE5U-45				LFE5U-85			
Pin Type		256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	554 caBGA	285 csfBGA	381 caBGA	554 caBGA	756 caBGA
General Purpose Inputs/Outputs per Bank	Bank 0	24	6	24	24	6	24	24	6	27	32	6	27	32	56
	Bank 1	32	6	32	32	6	32	32	6	33	40	6	33	40	48
	Bank 2	32	21	32	32	21	32	32	21	32	32	21	34	32	48
	Bank 3	32	28	32	32	28	32	32	28	33	48	28	33	48	64
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	14	24
	Bank 6	32	26	32	32	26	32	32	26	33	48	26	33	48	64
	Bank 7	32	18	32	32	18	32	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13	13	13	13	13	13
Total Single-Ended User		197	118	197	197	118	197	197	118	203	245	118	205	259	365
VCC		6	13	20	6	13	20	6	13	20	24	13	20	24	36
VCCAUX (Core)		2	3	4	2	3	4	2	3	4	9	3	4	9	8
VCCIO	Bank 0	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 1	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 2	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 3	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	2	2
	Bank 6	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 7	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 8	1	2	2	1	2	2	1	2	2	2	2	2	2	2
TAP		4	4	4	4	4	4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated		7	7	7	7	7	7	7	7	7	7	7	7	7	7
GND		27	123	99	27	123	99	27	123	99	198	123	99	198	267
NC		0	1	26	0	1	26	0	1	26	33	1	26	33	29
Reserved		0	4	6	0	4	6	0	4	6	12	4	6	12	12
Total Balls		256	285	381	256	285	381	256	285	381	554	285	381	554	756
High Speed Differential Input / Output Pairs	Bank 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 2	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	16/8	16/8	16/8	10/8	17/9	16/8
	Bank 3	16/8	14/7	16/8	16/8	14/7	16/8	16/8	14/7	16/8	24/12	14/7	16/8	24/1	
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 5	16/8	13/6	16/8	16/8	13/6	16/8	16/8	13/6	16/8	24/12	13/6	16/8	24/1	
	Bank 6	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8	
	Bank 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Total High Speed		64/32	45/27	64/32	64/32	45/27	64/32	64/32	45/27	64/32	80/40	45/27	65/33	80/40	112/
DQS Groups (> 11 pins in group)	Bank 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 2	2	1	2	2	1	2	2	1	2	2	2	1	2	2
	Bank 3	2	2	2	2	2	2	2	2	2	2	3	2	2	3
	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank 5	2	2	2	2	2	2	2	2	2	2	3	2	2	3
	Bank 6	2	1	2	2	1	2	2	1	2	2	2	1	2	2
	Bank 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Total DQS Groups		8	6	8	8	6	8	8	6	8	10	6	8	10	14

Revision History

Date	Version	Section	Change Summary
March 2018	1.9	All	Updated formatting and page referencing.
		General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide . Added caBGA256 package in LFE5U-45.
		Architecture	Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support . Updated footnote #1.
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions .
			Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics .
			Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) .
			Updated Table 3.11. sys/O Recommended Operating Conditions .
			Updated Table 3.12. Single-Ended DC Characteristics .
			Updated Table 3.13. LVDS .
			Updated Table 3.14. LVDS25E DC Conditions .
			Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed .
			Updated Table 3.28. Receiver Total Jitter Tolerance Specification .
			Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics .
			Updated header name of section 3.29 Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics .
		Pinout Information	Updated table in section 4.3.2 LFE5U .
		Ordering Information	Added table rows in 5.2.1 Commercial .
			Added table rows in 5.2.2 Industrial .
		Supplemental Information	Updated For Further Information section.
November 2017	1.8	General Description	Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide . Added caBGA256 package in LFE5U-12 and LFE5U-25.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclk).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.