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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

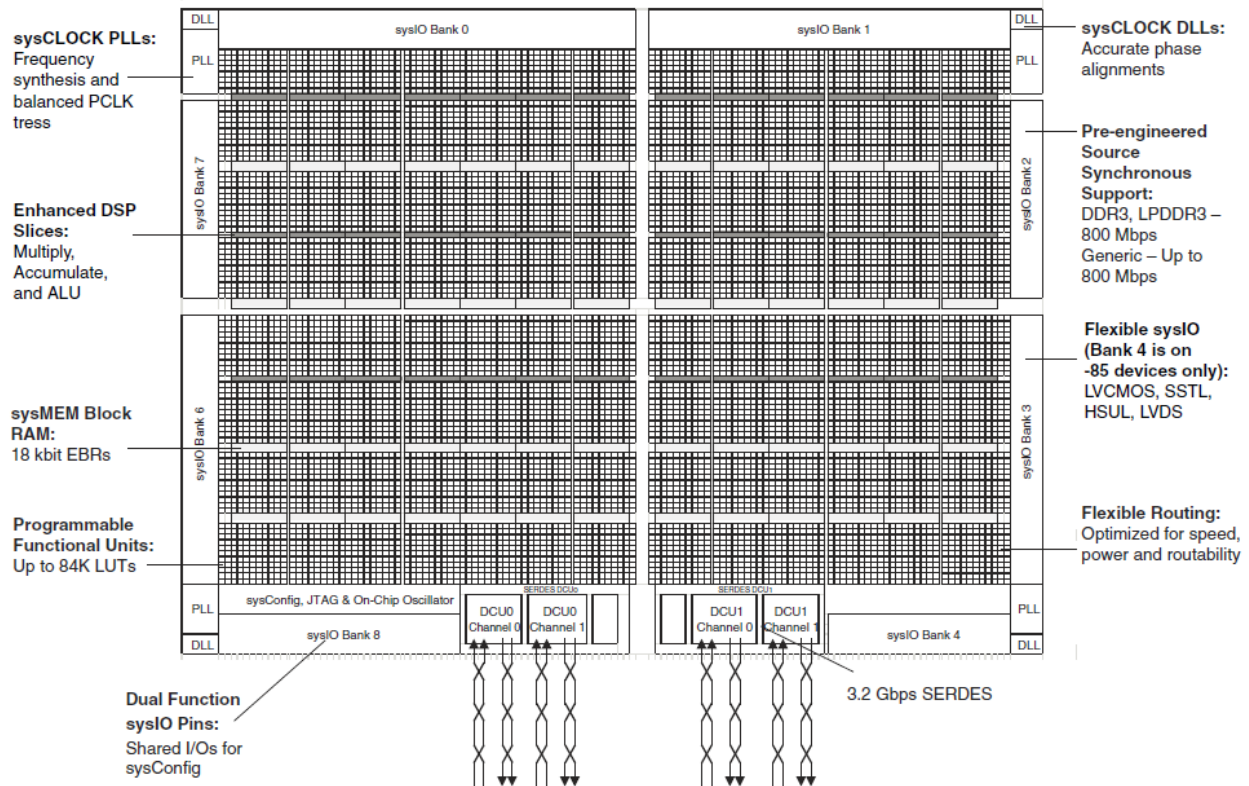
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-6mg285i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-6mg285i</a>

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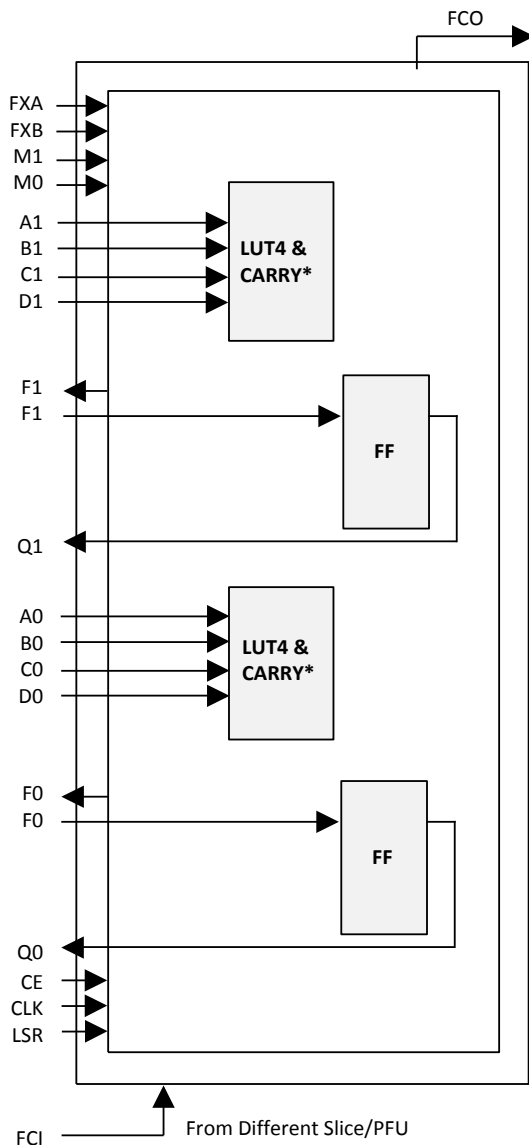
Note: There is no Bank 4 in -25 and -45 devices.  
There are no PLL and DLL on the top corners in -25 devices.

**Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)**

## 2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.



**Notes:** For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

WCK is CLK

WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2

WAD [A:D] is a 4-bit address from slice 2 LUT input

**Figure 2.3. Slice Diagram**

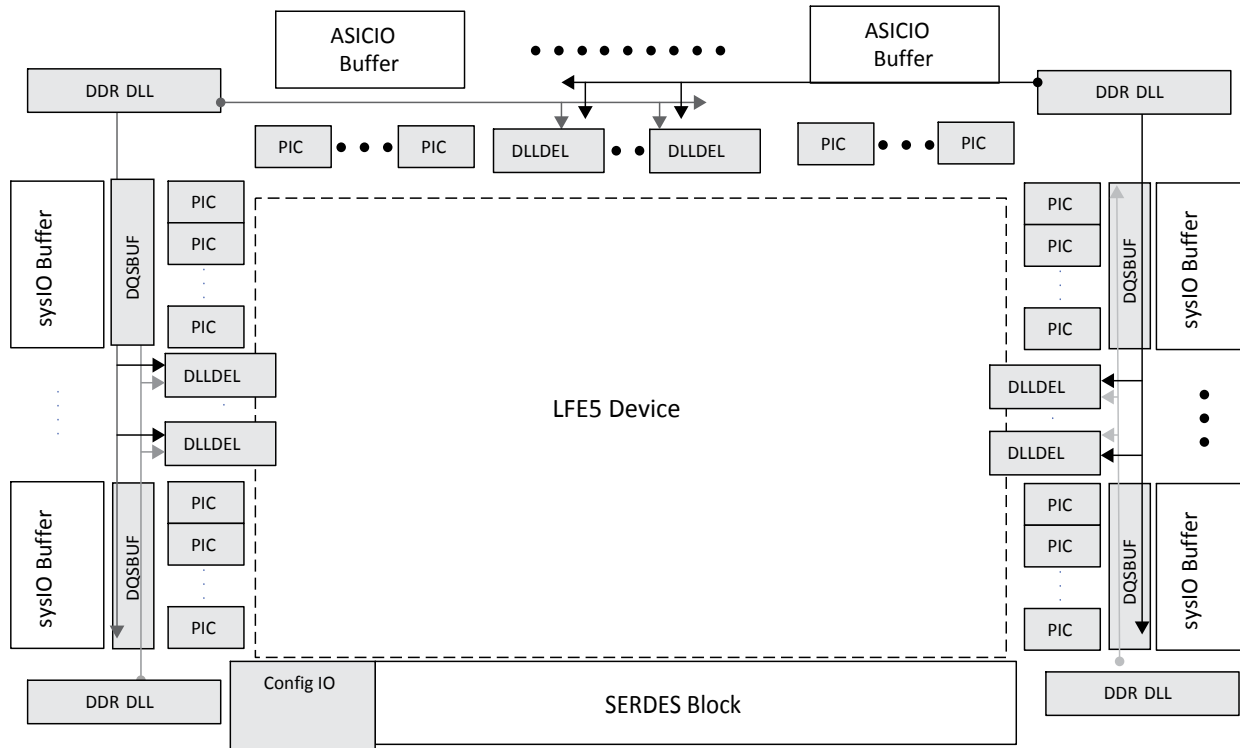


Figure 2.11. ECP5/ECP5-5G DLL Top Level View (For LFE-45 and LFE-85)

## 2.8. sysMEM Memory

ECP5/ECP5-5G devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

### 2.8.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.6 on page 25. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#).

- 5\*5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5/ ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.

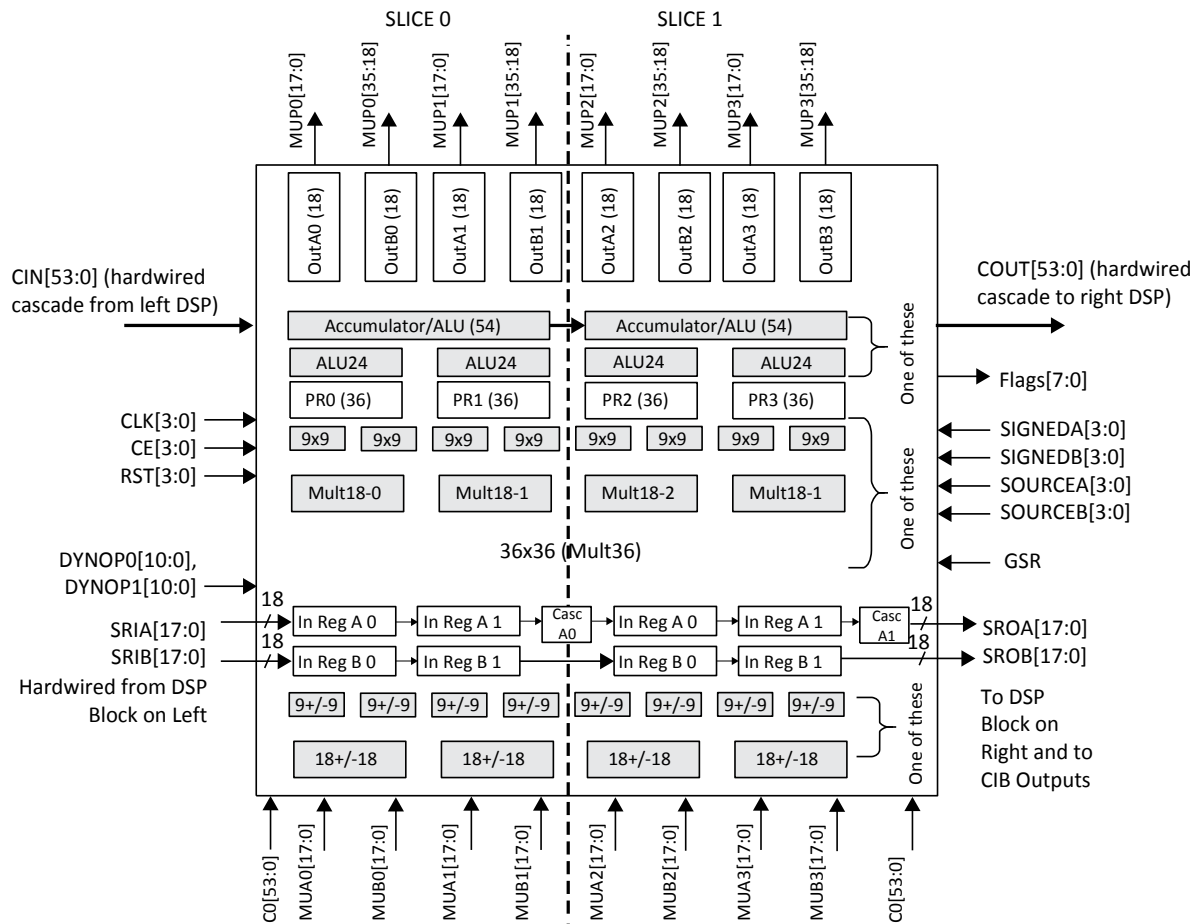


Figure 2.14. Simplified sysDSP Slice Block Diagram

## 2.11. PIO

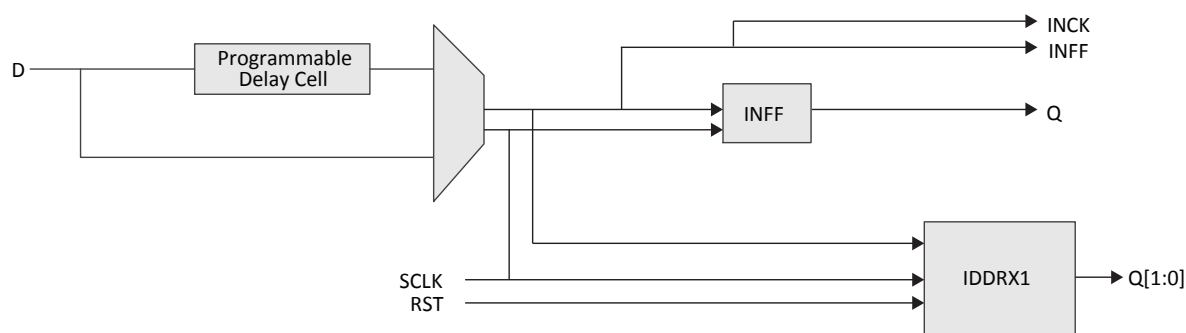
The PIO contains three blocks: an input register block, output register block, and tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

### 2.11.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

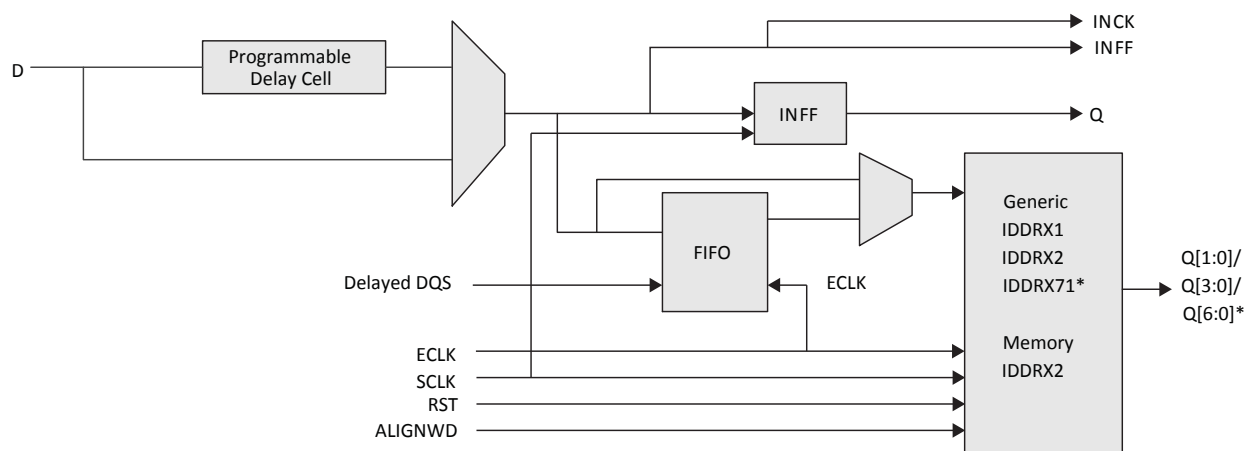
The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers to shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers samples the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The top side of the device supports IDDRX1 gearing function. For more information on gearing function, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

Figure 2.17 shows the input register block for the PIOs on the top edge.



**Figure 2.17. Input Register Block for PIO on Top Side of the Device**

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



\*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

**Figure 2.18. Input Register Block for PIO on Left and Right Side of the Device**

## 2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. [Figure 2.27](#) shows the position of the dual blocks for the LFE5-85. [Table 2.13](#) shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).



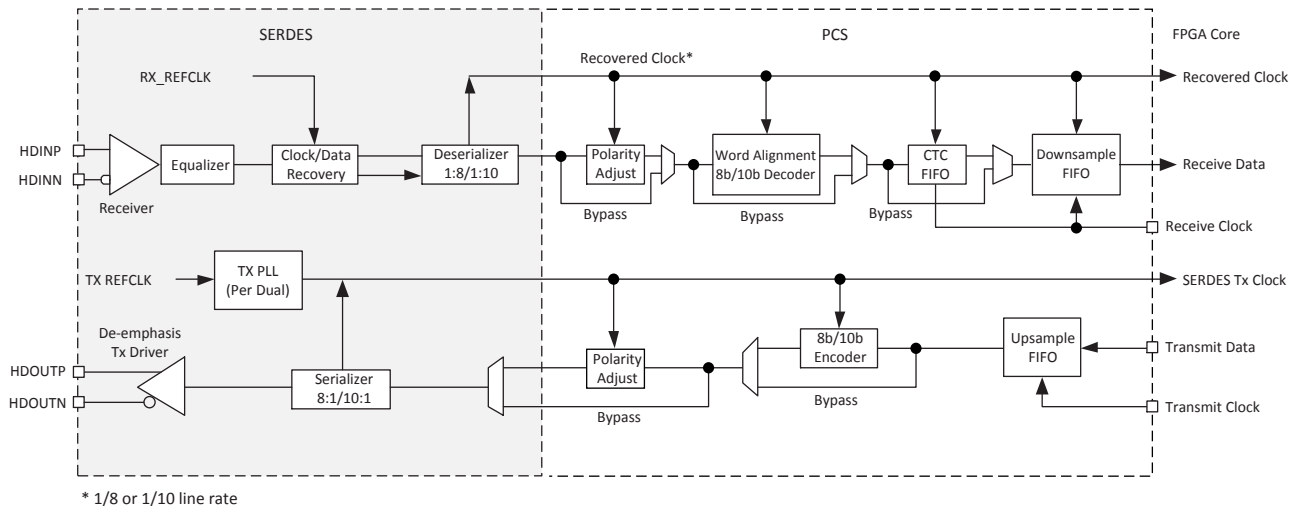
**Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices**

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

### 2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. [Figure 2.28](#) shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).


**Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block**

### 2.15.2. PCS

As shown in [Figure 2.28](#), the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for more information.

## 3. DC and Switching Characteristics

### 3.1. Absolute Maximum Ratings

**Table 3.1. Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	−0.5	1.32	V
V <sub>CCA</sub>	Supply Voltage	−0.5	1.32	V
V <sub>CCAUX</sub> , V <sub>CCAUXA</sub>	Supply Voltage	−0.5	2.75	V
V <sub>CCIO</sub>	Supply Voltage	−0.5	3.63	V
—	Input or I/O Transient Voltage Applied	−0.5	3.63	V
V <sub>CCHRX</sub> , V <sub>CCHTX</sub>	SERDES RX/TX Buffer Supply Voltages	−0.5	1.32	V
—	Voltage Applied on SERDES Pins	−0.5	1.80	V
T <sub>A</sub>	Storage Temperature (Ambient)	−65	150	°C
T <sub>J</sub>	Junction Temperature	—	+125	°C

**Notes:**

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

### 3.2. Recommended Operating Conditions

**Table 3.2. Recommended Operating Conditions**

Symbol	Parameter		Min	Max	Unit
V <sub>CC</sub> <sup>2</sup>	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
V <sub>CCAUX</sub> <sup>2,4</sup>	Auxiliary Supply Voltage	—	2.375	2.625	V
V <sub>CCIO</sub> <sup>2,3</sup>	I/O Driver Supply Voltage	—	1.14	3.465	V
V <sub>REF</sub> <sup>1</sup>	Input Reference Voltage	—	0.5	1.0	V
t <sub>JCOM</sub>	Junction Temperature, Commercial Operation	—	0	85	°C
t <sub>JIND</sub>	Junction Temperature, Industrial Operation	—	−40	100	°C
<b>SERDES External Power Supply<sup>5</sup></b>					
V <sub>CCA</sub>	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V <sub>CCAUXA</sub>	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
V <sub>CCHRX</sub> <sup>6</sup>	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V <sub>CCHTX</sub>	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

**Notes:**

1. For correct operation, all supplies except V<sub>REF</sub> must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in [Table 3.4](#) on page 48.
4. V<sub>CCAUX</sub> ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
5. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for information on board considerations for SERDES power supplies.
6. V<sub>CCHRX</sub> is used for Rx termination. It can be biased to V<sub>cm</sub> if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

### 3.3. Power Supply Ramp Rates

**Table 3.3. Power Supply Ramp Rates**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{RAMP}$	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

**Note:** Assumes monotonic ramp rates.

### 3.4. Power-On-Reset Voltage Levels

**Table 3.4. Power-On-Reset Voltage Levels**

Symbol	Parameter			Min	Typ	Max	Unit
$V_{PORUP}$	All Devices	Power-On-Reset ramp-up trip point (Monitoring $V_{CC}$ , $V_{CCAUX}$ , and $V_{CCIO8}$ )	$V_{CC}$	0.90	—	1.00	V
			$V_{CCAUX}$	2.00	—	2.20	V
			$V_{CCIO8}$	0.95	—	1.06	V
$V_{PORDN}$	All Devices	Power-On-Reset ramp-down trip point (Monitoring $V_{CC}$ , and $V_{CCAUX}$ )	$V_{CC}$	0.77	—	0.87	V
			$V_{CCAUX}$	1.80	—	2.00	V

**Notes:**

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only  $V_{CCIO8}$  has a Power-On-Reset ramp up trip point. All other  $V_{CCIOs}$  do not have Power-On-Reset ramp up detection.
- $V_{CCIO8}$  does not have a Power-On-Reset ramp down detection.  $V_{CCIO8}$  must remain within the Recommended Operating Conditions to ensure proper operation.

### 3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when  $V_{CC}$ ,  $V_{CCAUX}$ , and  $V_{CCIO8}$  are ramped above the  $V_{PORUP}$  voltage, as specified above.

$V_{CCIO8}$  controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp  $V_{CCIO8}$  above  $V_{IH}$  of the external SPI Flash, before at least one of the other two supplies ( $V_{CC}$  and/or  $V_{CCAUX}$ ) is ramped to  $V_{PORUP}$  voltage level. If the system cannot meet this power up sequence requirement, and requires the  $V_{CCIO8}$  to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until  $V_{CCIO8}$  reaches  $V_{IH}$  of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the  $V_{IH}$  voltage requirement of the SPI Flash. For LFE5UM/LFE5UM5G devices, it is required to power up  $V_{CCA}$ , before  $V_{CCAUXA}$  is powered up.

### 3.6. Hot Socketing Specifications

**Table 3.5. Hot Socketing Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \leq V_{IN} \leq V_{IH} \text{ (Max)}$	—	—	$\pm 1$	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \leq V_{IN} < V_{CCIO}$	—	—	$\pm 1$	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5 \text{ V}$	—	18	—	mA

**Notes:**

- $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$  should rise/fall monotonically.
- $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PW}$  or  $I_{BH}$ .
- LVC MOS and LV TTL only.
- Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the  $I_{DK}$  current can exceed  $\pm 1$  mA.

### 3.14.5. BLVDS25

The ECP5/ECP5-5G devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

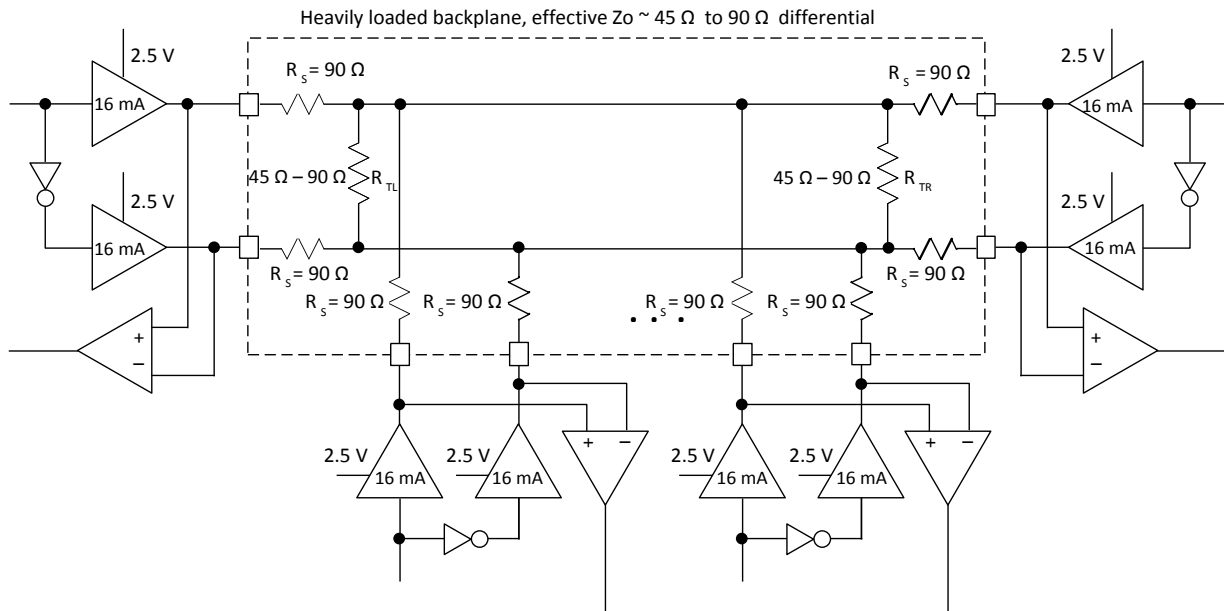


Figure 3.2. BLVDS25 Multi-point Output Example

Over recommended operating conditions.

Table 3.15. BLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		$Z_o = 45 \Omega$	$Z_o = 90 \Omega$	
$V_{CCIO}$	Output Driver Supply ( $\pm 5\%$ )	2.50	2.50	V
$Z_{OUT}$	Driver Impedance	10.00	10.00	$\Omega$
$R_S$	Driver Series Resistor ( $\pm 1\%$ )	90.00	90.00	$\Omega$
$R_{TL}$	Driver Parallel Resistor ( $\pm 1\%$ )	45.00	90.00	$\Omega$
$R_{TR}$	Receiver Termination ( $\pm 1\%$ )	45.00	90.00	$\Omega$
$V_{OH}$	Output High Voltage	1.38	1.48	V
$V_{OL}$	Output Low Voltage	1.12	1.02	V
$V_{OD}$	Output Differential Voltage	0.25	0.46	V
$V_{CM}$	Output Common Mode Voltage	1.25	1.25	V
$I_{DC}$	DC Output Current	11.24	10.20	mA

**Note:** For input buffer, see LVDS Table 3.13 on page 55.

### 3.14.8. SLVS

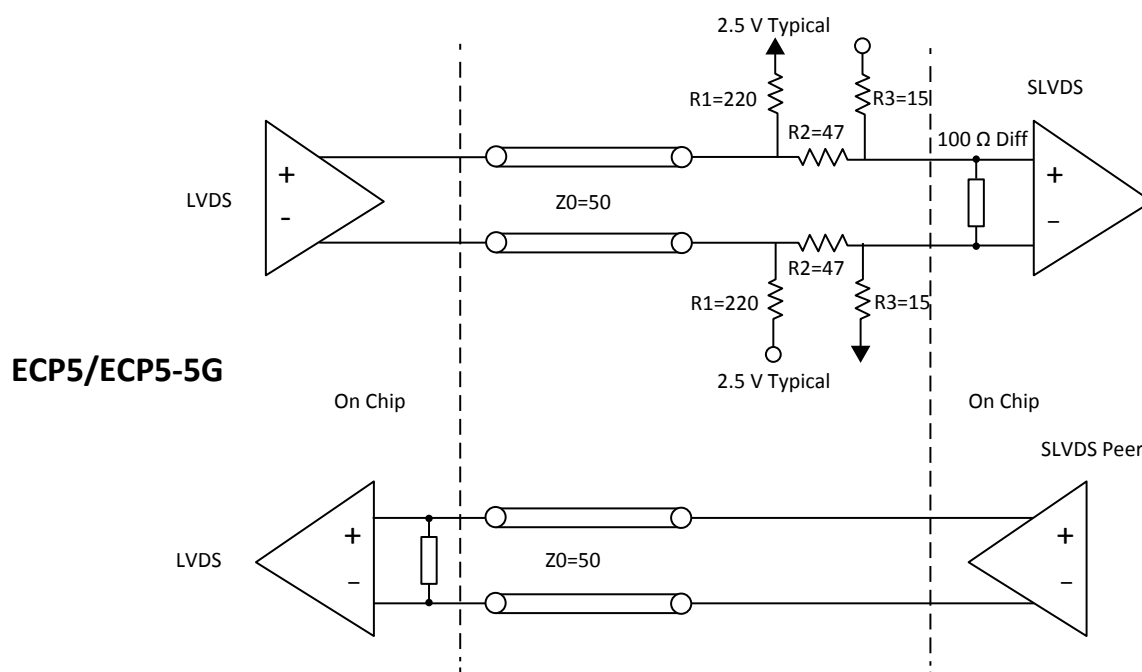
Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

**Table 3.18. Input to SLVS**

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.



**Figure 3.5. SLVS Interface**

### 3.18. External Switching Characteristics

Over recommended commercial operating conditions.

**Table 3.22. ECP5/ECP5-5G External Switching Characteristics**

Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks									
Primary Clock									
f <sub>MAX_PRI</sub>	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
t <sub>SKEW_PRI</sub>	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
Edge Clock									
f <sub>MAX_EDGE</sub>	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
t <sub>W_EDGE</sub>	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
t <sub>SKEW_EDGE</sub>	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
Generic SDR Input									
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL									
t <sub>CO</sub>	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
t <sub>SU</sub>	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
t <sub>SU_DEL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
t <sub>H_DEL</sub>	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL									
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
t <sub>SU_DEPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns

## 3.22. SERDES High-Speed Data Receiver

**Table 3.27. Serial Input Data Specifications**

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
$V_{RX-IN}$	Input levels	0	—	$V_{CCA} + 0.5^2$	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	$V_{CCA}$	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode) <sup>2</sup>	0.1	—	$V_{CCA} + 0.2$	V
$T_{RX-RELOCK}$	SCDR re-lock time <sup>1</sup>	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 $\Omega$ /High Z	–20%	50/75/5 K	+20%	$\Omega$
$RL_{RX-RL}$	Return loss (without package)	—	—	–10	dB

**Notes:**

1. This is the typical number of bit times to re-lock to a new phase or frequency within  $\pm 300$  ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

## 3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

**Table 3.28. Receiver Total Jitter Tolerance Specification**

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

**Notes:**

1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

## 3.24. SERDES External Reference Clock

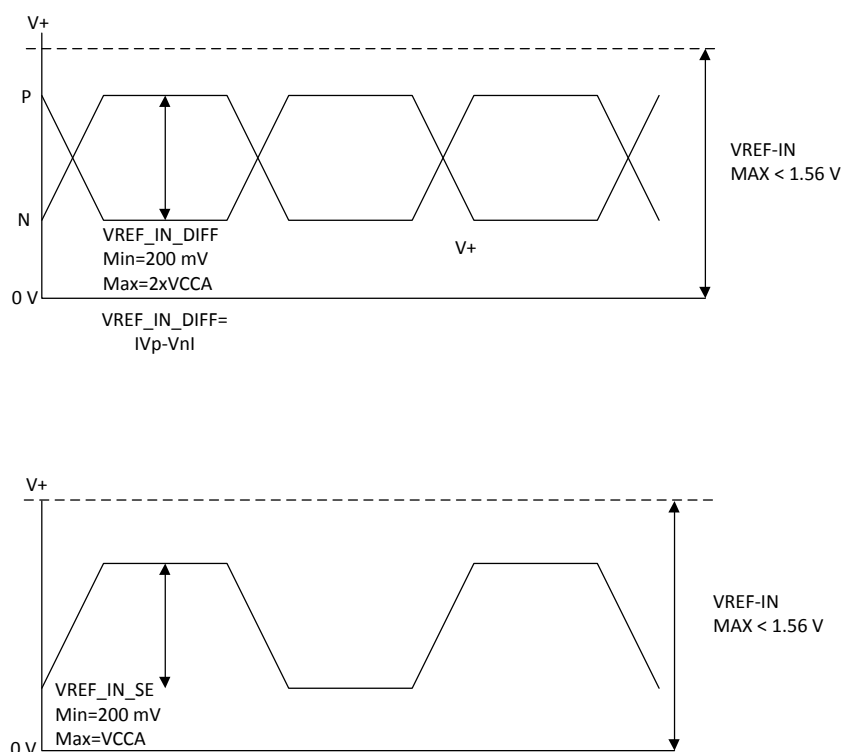
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3.29 specifies reference clock requirements, over the full range of operating conditions.

**Table 3.29. External Reference Clock Specification (refclkp/refclkn)**

Symbol	Description	Min	Typ	Max	Unit
$F_{REF}$	Frequency range	50	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance <sup>1</sup>	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock <sup>2,4</sup>	200	—	$V_{CCAUXA}$	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2 \cdot V_{CCAUXA}$	mV, p-p differential
$V_{REF-IN}$	Input levels	0	—	$V_{CCAUXA} + 0.4$	V
$D_{REF}$	Duty cycle <sup>3</sup>	40	—	60	%
$T_{REF-R}$	Rise time (20% to 80%)	200	500	1000	ps
$T_{REF-F}$	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–30%	100/HiZ	+30%	$\Omega$
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

**Notes:**

- Depending on the application, the PLL\_LOL\_SET and CDR\_LOL\_SET control registers may be adjusted for other tolerance values as described in [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).
- The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
- Measured at 50% amplitude.
- Single-ended clocking is achieved by applying a reference voltage  $V_{REF}$  on REFCLKN input, with the clock applied to REFCLKP input pin.  $V_{REF}$  should be set to mid-point of the REFCLKP voltage swing.



**Figure 3.14. SERDES External Reference Clock Waveforms**



### 3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

**Table 3.31. PCIe (5 Gb/s)**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
<b>Transmit<sup>1</sup></b>						
UI	Unit Interval	—	199.94	200	200.06	ps
B <sub>WTX-PKG-PLL2</sub>	Tx PLL bandwidth corresponding to PKGTx-PLL2	—	5	—	16	MHz
P <sub>KGTx-PLL2</sub>	Tx PLL Peaking	—	—	—	1	dB
V <sub>TX-DIFF-PP</sub>	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
V <sub>TX-DIFF-PP-LOW</sub>	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
V <sub>TX-DE-RATIO-3.5dB</sub>	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
V <sub>TX-DE-RATIO-6dB</sub>	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
T <sub>MIN-PULSE</sub>	Instantaneous lone pulse width	—	—	—	—	UI
T <sub>TX-RISE-FALL</sub>	Transmitter rise and fall time	—	—	—	—	UI
T <sub>TX-EYE</sub>	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T <sub>TX-DJ</sub>	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T <sub>TX-RJ</sub>	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
T <sub>RF-MISMATCH</sub>	Tx rise/fall time mismatch	—	—	—	—	UI
R <sub>LTX-DIFF</sub>	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R <sub>LTX-CM</sub>	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
Z <sub>TX-DIFF-DC</sub>	DC differential Impedance	—	—	—	120	Ω
V <sub>TX-CM-AC-PP</sub>	Tx AC peak common mode voltage, peak-peak	—	—	—	—	mV, p-p
I <sub>TX-SHORT</sub>	Transmitter short-circuit current	—	—	—	90	mA
V <sub>TX-DC-CM</sub>	Transmitter DC common-mode voltage	—	0	—	1.2	V
V <sub>TX-IDLE-DIFF-DC</sub>	Electrical Idle Output DC voltage	—	0	—	5	mV
V <sub>TX-IDLE-DIFF-AC-p</sub>	Electrical Idle Differential Output peak voltage	—	—	—	—	mV
V <sub>TX-RCV-DETECT</sub>	Voltage change allowed during Receiver Detect	—	—	—	600	mV
T <sub>TX-IDLE-MIN</sub>	Min. time in Electrical Idle	—	20	—	—	ns
T <sub>TX-IDLE-SET-TO-IDLE</sub>	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
T <sub>TX-IDLE-TO-DIFF-DATA</sub>	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
L <sub>TX-SKEW</sub>	Lane-to-lane output skew	—	—	—	—	ps

### 3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

**Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
<b>Transmit</b>						
UI	Unit Interval	—	203.43	203.45	203.47	ps
T <sub>DCD</sub>	Duty Cycle Distortion	—	—	—	0.05	UI
J <sub>UBHPJ</sub>	Uncorrelated Bounded High Probability Jitter	—	—	—	0.15	UI
J <sub>TOTAL</sub>	Total Jitter	—	—	—	0.3	UI
Z <sub>RX-DIFF-DC</sub>	DC differential Impedance	—	80	—	120	Ω
T <sub>SKEW</sub>	Skew between differential signals	—	—	—	9	ps
R <sub>LTX-DIFF</sub>	Tx Differential Return Loss (S22), including package and silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R <sub>LTX-CM</sub>	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	—	—	dB
I <sub>TX-SHORT</sub>	Transmitter short-circuit current	—	—	—	100	mA
T <sub>RISE_FALL-DIFF</sub>	Differential Rise and Fall Time	—	—	—	—	ps
L <sub>TX-SKEW</sub>	Lane-to-lane output skew	—	—	—	—	ps
<b>Receive</b>						
UI	Unit Interval	—	203.43	203.45	203.47	ps
V <sub>RX-DIFF-PP</sub>	Differential Rx peak-peak voltage	—	—	—	1.2	V, p-p
V <sub>RX-EYE_Y1_Y2</sub>	Receiver eye opening mask, Y1 and Y2	—	62.5	—	375	mV, diff
V <sub>RX-EYE_X1</sub>	Receiver eye opening mask, X1	—	—	—	0.3	UI
T <sub>RX-TJ</sub>	Receiver total jitter tolerance (not including sinusoidal)	—	—	—	0.6	UI
R <sub>LRX-DIFF</sub>	Receiver differential Return Loss, package plus silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R <sub>LRX-CM</sub>	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z <sub>RX-DIFF-DC</sub>	Receiver DC differential impedance	—	80	100	120	Ω

**Note:** Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

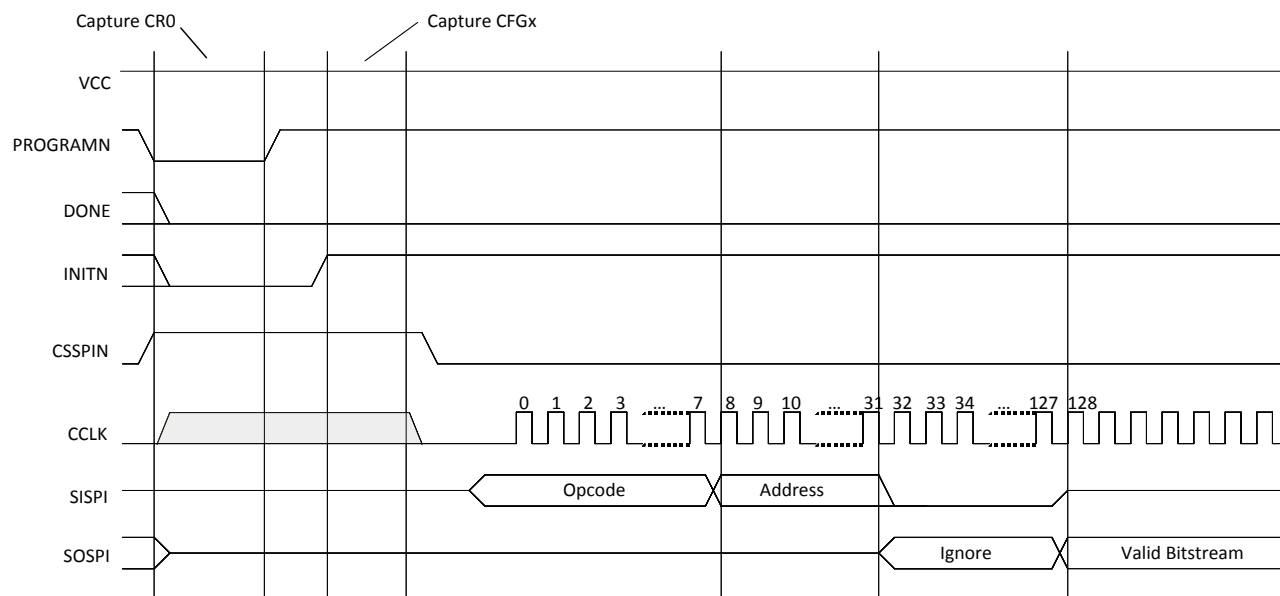


Figure 3.22. Master SPI Configuration Waveforms

### 3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
$f_{MAX}$	TCK clock frequency	—	25	MHz
$t_{BTCPH}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{BTCPL}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{BTS}$	TCK [BSCAN] setup time	10	—	ns
$t_{BTH}$	TCK [BSCAN] hold time	8	—	ns
$t_{BTRF}$	TCK [BSCAN] rise/fall time	50	—	mV/ns
$t_{BTCO}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{BTCOEN}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{BTCRS}$	BSCAN test capture register setup time	8	—	ns
$t_{BTCRH}$	BSCAN test capture register hold time	25	—	ns
$t_{BUTCO}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Signal Name	I/O	Description
<b>PLL, DLL and Clock Functions (Continued)</b>		
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
[T/R]]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
<b>Test and Programming (Dedicated Pins)</b>		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. This is a dedicated input pin.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.
<b>Configuration Pads (Used during sysCONFIG)</b>		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes (Master SPI, Master Serial). This is a dedicated pin.
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPI mode data output. This is a shared I/O pin. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DOUT/CSO	O	Serial data output. Chip select output. SPI/SPI mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O
DO/MOSI/IOO	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	No
LFE5UM-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes
LFE5UM5G-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM5G-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM5G-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM5G-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM5G-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM5G-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM5G-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM5G-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM5G-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes