Lattice Semiconductor Corporation - LFE5UM-45F-8BG381C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	203
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-8bg381c

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay-Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLL	Phase-Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SERDES	Serializer/Deserializer
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

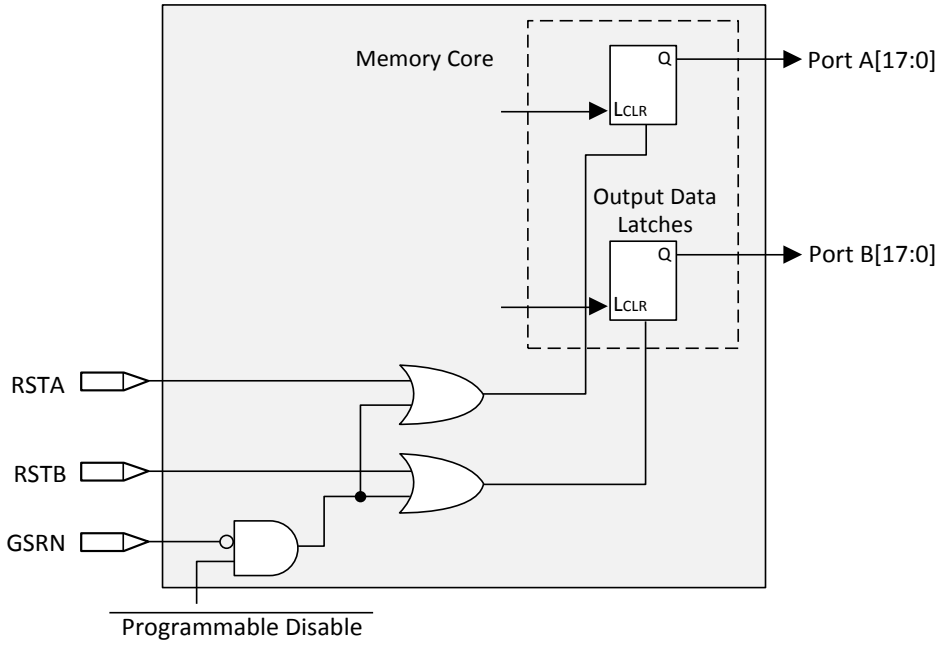


Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

2.9. sysDSP™ Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) – Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to Minimizing System Interruption During Configuration Using TransFR Technology (TN1087) for details.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3, 5]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.14.7. **MLVDS25**

The ECP5/ECP5-5G devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.

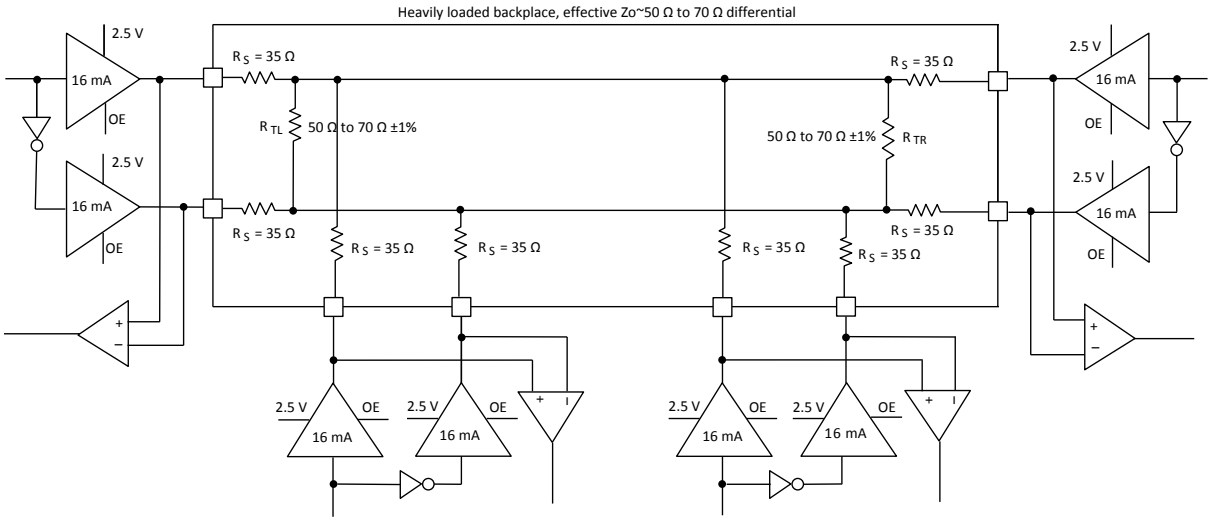


Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Table 3.17. MLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo=50 Ω	Zo=70 Ω	
V_{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (±1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (±1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

Table 3.18. Input to SLVS

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.

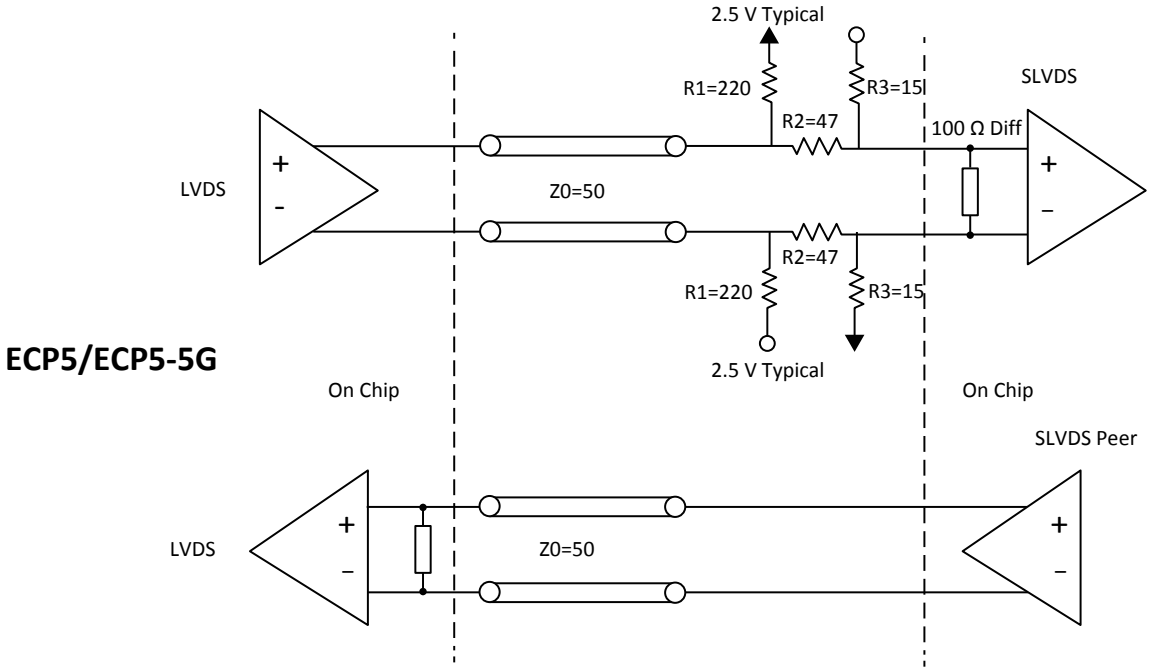


Figure 3.5. SLVS Interface

Table 3.20. Register-to-Register Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	441	MHz
32-Bit Decoder	441	MHz
64-Bit Decoder	332	MHz
4:1 Mux	441	MHz
8:1 Mux	441	MHz
16:1 Mux	441	MHz
32:1 Mux	441	MHz
8-Bit Adder	441	MHz
16-Bit Adder	441	MHz
64-Bit Adder	441	MHz
16-Bit Counter	384	MHz
32-Bit Counter	317	MHz
64-Bit Counter	263	MHz
64-Bit Accumulator	288	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	214	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	441	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	441	MHz
DSP Functions		
9 x 9 Multiplier (All Registers)	225	MHz
18 x 18 Multiplier (All Registers)	225	MHz
36 x 36 Multiplier (All Registers)	225	MHz
18 x 18 Multiply-Add/Sub (All Registers)	225	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	225	MHz

Notes:

1. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks									
Primary Clock									
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
Edge Clock									
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
t_{SKEW_EDGE}	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
Generic SDR Input									
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL									
t_{CO}	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL									
t_{COPLL}	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns

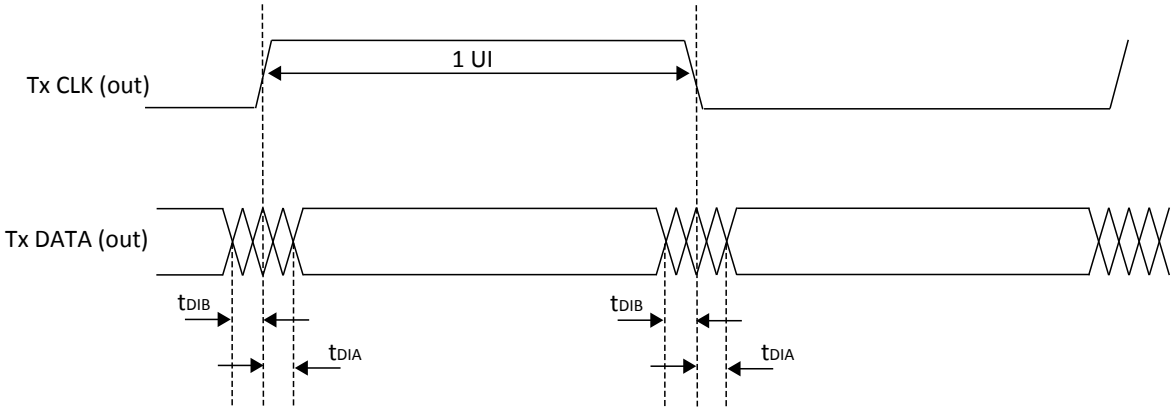
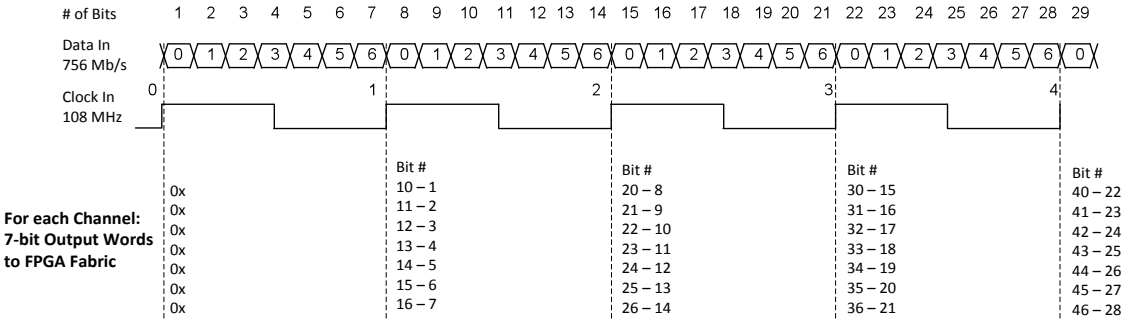


Figure 3.9. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter – Shown for one LVDS Channel

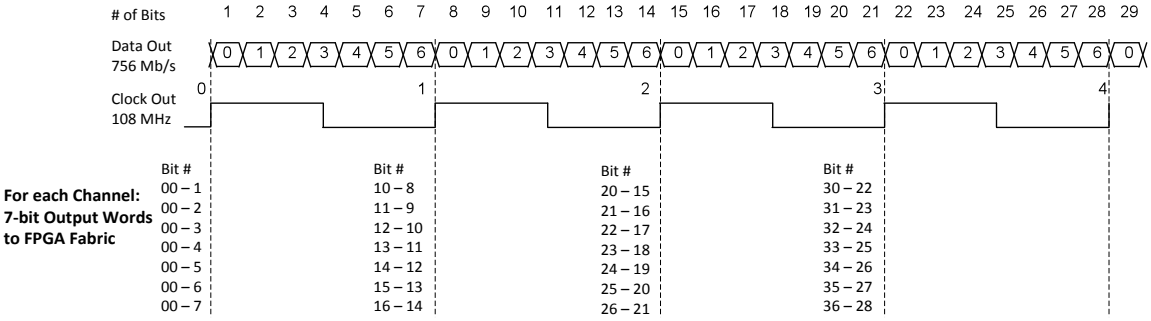


Figure 3.10. DDRX71 Video Timing Waveforms

3.25. PCI Express Electrical and Timing Characteristics

3.25.1. PCIe (2.5 Gb/s) AC and DC Characteristics

Over recommended operating conditions.

Table 3.30. PCIe (2.5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit[1]						
UI	Unit interval	—	399.88	400	400.12	ps
$V_{TX-DIFF\_P-P}$	Differential peak-to-peak output	—	0.8	1.0	1.2	V
$V_{TX-DE-RATIO}$	De-emphasis differential output voltage ratio	—	–3	–3.5	–4	dB
$V_{TX-CM-AC\_P}$	RMS AC peak common-mode output voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection	—	—	—	600	mV
$V_{TX-CM-DC}$	Tx DC common mode voltage	—	0	—	V_{CCHTX}	V
$I_{TX-SHORT}$	Output short circuit current	V_{TX-D+}=0.0 V V_{TX-D-}=0.0 V	—	—	90	mA
$Z_{TX-DIFF-DC}$	Differential output impedance	—	80	100	120	Ω
$RL_{TX-DIFF}$	Differential return loss	—	10	—	—	dB
RL_{TX-CM}	Common mode return loss	—	6.0	—	—	dB
$T_{TX-RISE}$	Tx output rise time	20% to 80%	0.125	—	—	UI
$T_{TX-FALL}$	Tx output fall time	20% to 80%	0.125	—	—	UI
$L_{TX-SKEW}$	Lane-to-lane static output skew for all lanes in port/link	—	—	—	1.3	ns
T_{TX-EYE}	Transmitter eye width	—	0.75	—	—	UI
$T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median	—	—	—	0.125	UI
Receive[1, 2]						
UI	Unit Interval	—	399.88	400	400.12	ps
$V_{RX-DIFF\_P-P}$	Differential peak-to-peak input voltage	—	0.34[3]	—	1.2	V
$V_{RX-IDLE-DET-DIFF\_P-P}$	Idle detect threshold voltage	—	65	—	340[3]	mV
$V_{RX-CM-AC\_P}$	RMS AC peak common-mode input voltage	—	—	—	150	mV
$Z_{RX-DIFF-DC}$	DC differential input impedance	—	80	100	120	Ω
Z_{RX-DC}	DC input impedance	—	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Power-down DC input impedance	—	200K	—	—	Ω
$RL_{RX-DIFF}$	Differential return loss	—	10	—	—	dB
RL_{RX-CM}	Common mode return loss	—	6.0	—	—	dB

Notes:

1. Values are measured at 2.5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express 1.1 standard.

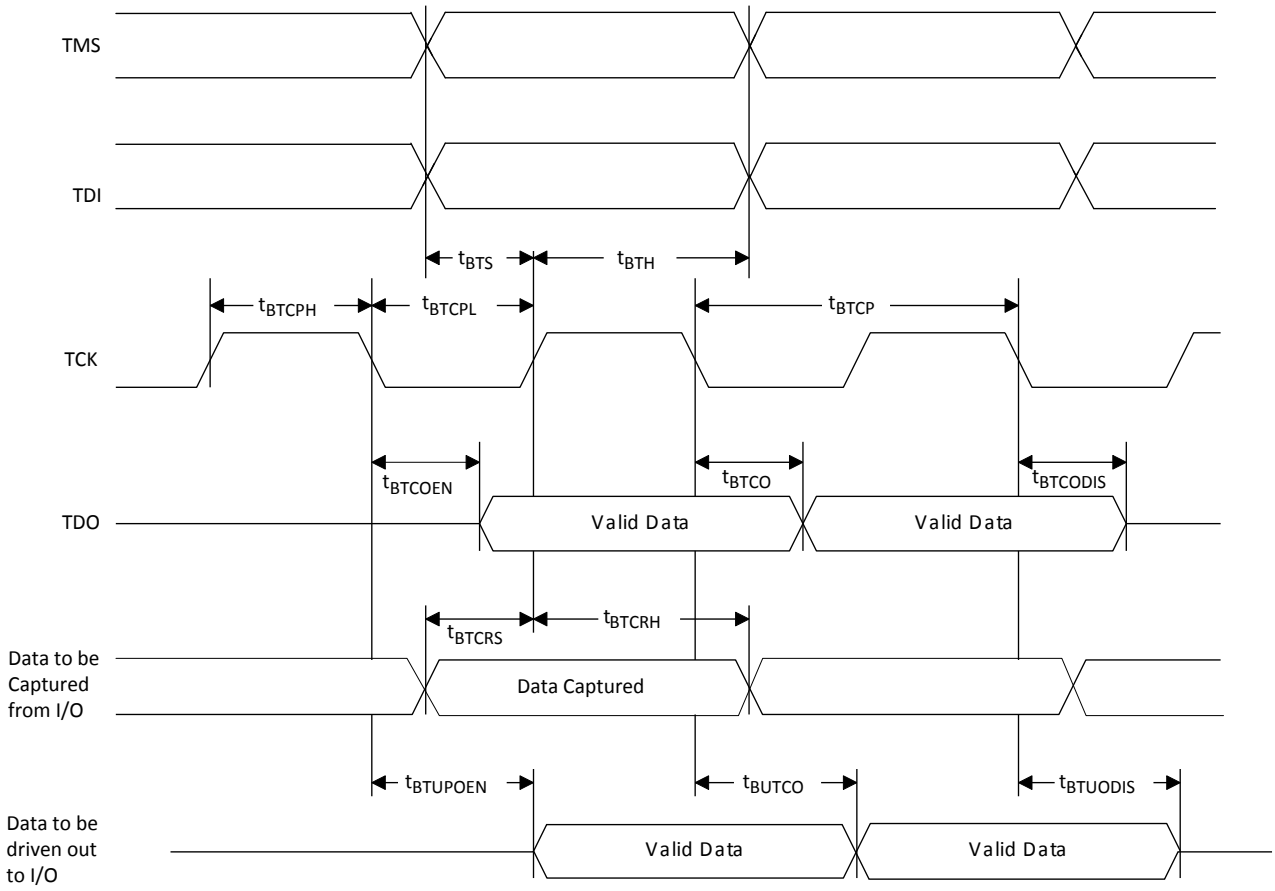
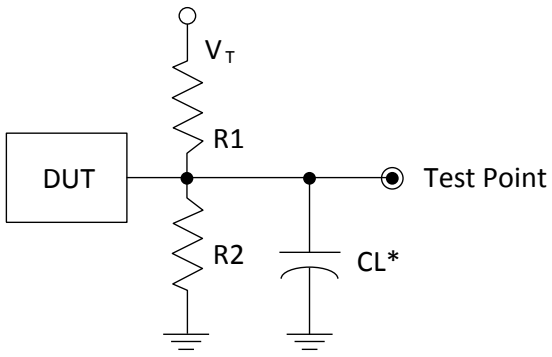


Figure 3.23. JTAG Port Timing Waveforms

3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.



*CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards

Table 3.44. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V_{OH} – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

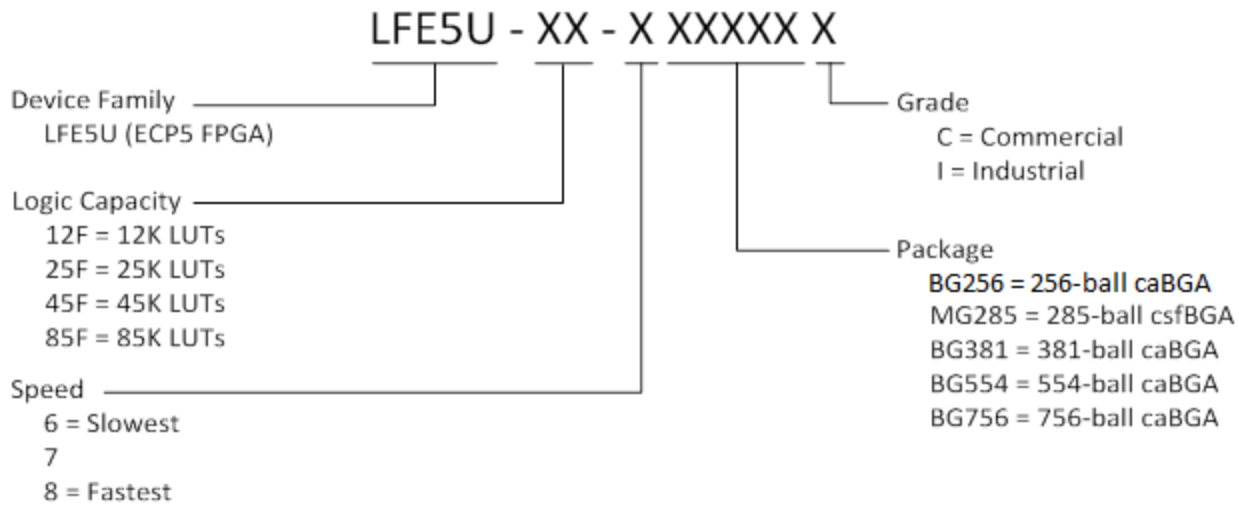
Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) *(Continued)*		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin
SERDES Function		
VCCAx	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCAx = 1.1 V for ECP5, VCCAx = 1.2 V for ECP5-5G.
VCCAUXAx	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUXAx = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

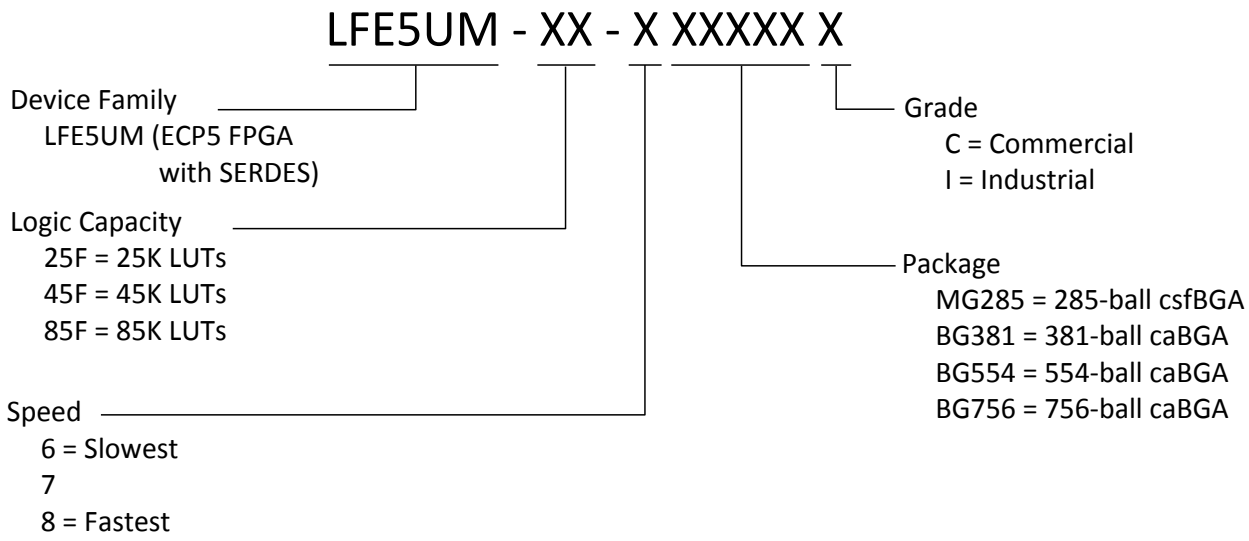
Notes:

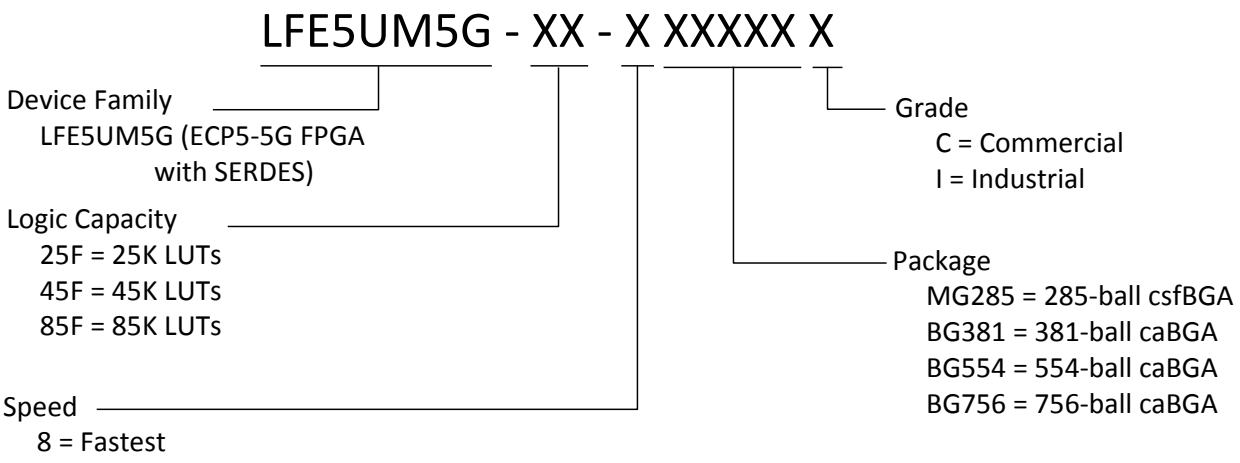
1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

5. Ordering Information

5.1. ECP5/ECP5-5G Part Number Description







5.2. Ordering Part Numbers

5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	–6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	–7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	–8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	–6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	–7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	–8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	–6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	–7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	–8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	–6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	–7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	–8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	–6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	–7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	–6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	–7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	–6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	–7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	–8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	–6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	–7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	–6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	–7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	–6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	–7	Lead free caBGA	554	Commercial	44	No

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	–8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	–8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	–8	Lead free caBGA	756	Commercial	84	Yes

5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	–6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	–7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	–8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	–6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	–7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	–8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	–6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	–7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	–8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	–6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	–7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	–8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	–6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	–7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	–8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	No

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	No
LFE5U-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	No
LFE5UM-25F-6MG285I	–6	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-7MG285I	–7	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM-25F-6BG381I	–6	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-7BG381I	–7	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM-45F-6MG285I	–6	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-7MG285I	–7	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM-45F-6BG381I	–6	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-7BG381I	–7	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM-45F-6BG554I	–6	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-7BG554I	–7	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM-85F-6MG285I	–6	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-7MG285I	–7	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM-85F-6BG381I	–6	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-7BG381I	–7	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM-85F-6BG554I	–6	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-7BG554I	–7	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM-85F-6BG756I	–6	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-7BG756I	–7	Lead free caBGA	756	Industrial	84	Yes
LFE5UM-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes
LFE5UM5G-25F-8MG285I	–8	Lead free csfBGA	285	Industrial	24	Yes
LFE5UM5G-25F-8BG381I	–8	Lead free caBGA	381	Industrial	24	Yes
LFE5UM5G-45F-8MG285I	–8	Lead free csfBGA	285	Industrial	44	Yes
LFE5UM5G-45F-8BG381I	–8	Lead free caBGA	381	Industrial	44	Yes
LFE5UM5G-45F-8BG554I	–8	Lead free caBGA	554	Industrial	44	Yes
LFE5UM5G-85F-8MG285I	–8	Lead free csfBGA	285	Industrial	84	Yes
LFE5UM5G-85F-8BG381I	–8	Lead free caBGA	381	Industrial	84	Yes
LFE5UM5G-85F-8BG554I	–8	Lead free caBGA	554	Industrial	84	Yes
LFE5UM5G-85F-8BG756I	–8	Lead free caBGA	756	Industrial	84	Yes

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section. • Deleted Serial RapidIO protocol under Embedded SERDES. • Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3. Mentioned transmit de-emphasis “pre- and post-cursors”.
		Architecture	Updated Overview section. • Revised description of PFU blocks. • Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section. • Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. • Deleted Serial RapidIO protocol. • Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section. • Deleted “130 MHz ±15% CMOS” oscillator. • Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA}.
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to t_{SKEW_PR} V_{CCA} and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.