Lattice Semiconductor Corporation - LFE5UM-45F-8BG381I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	203
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-8bg381i

1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

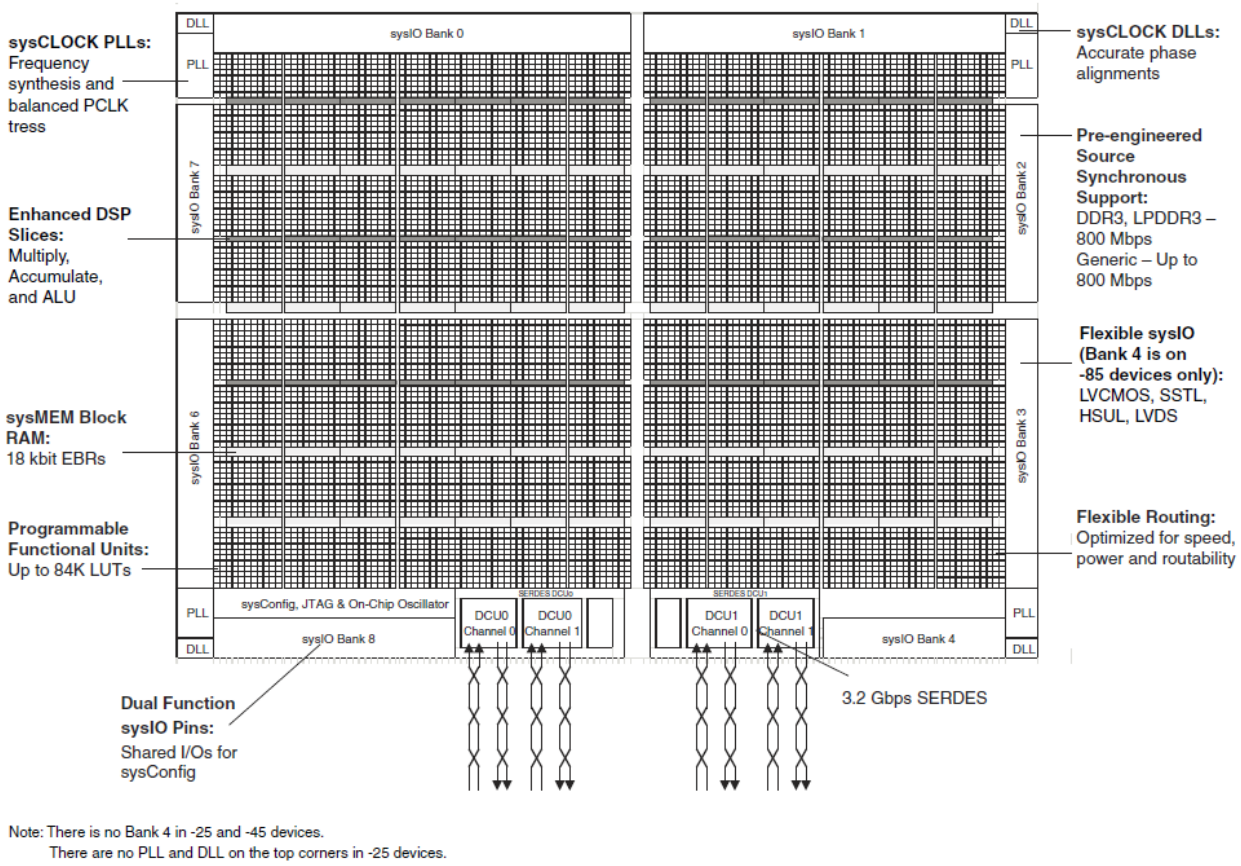
The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 84K LUTs
  - 197 to 365 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 3.744 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs



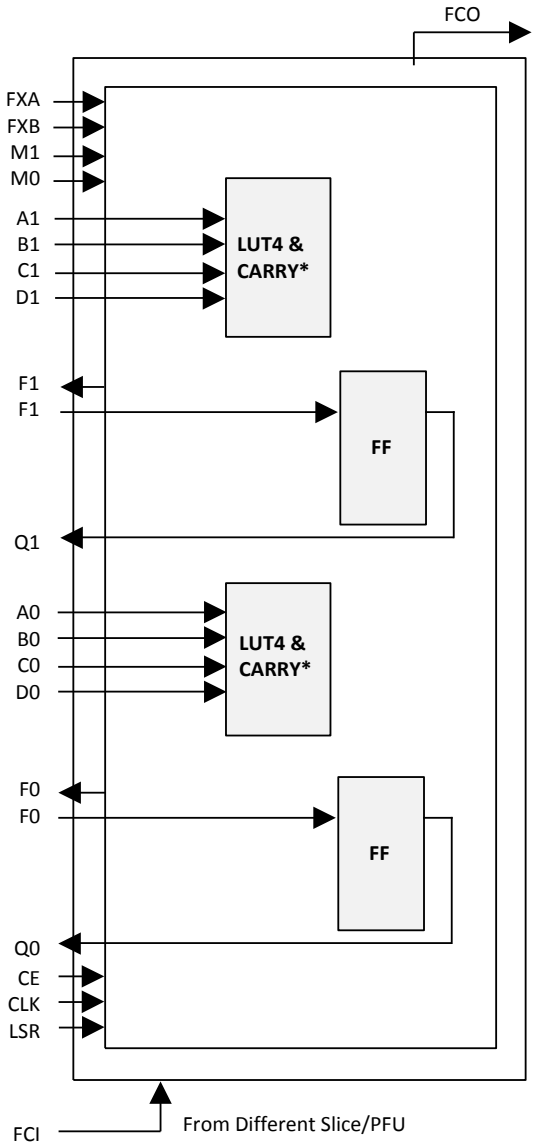
Note: There is no Bank 4 in -25 and -45 devices.
There are no PLL and DLL on the top corners in -25 devices.

Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

2.8.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.8.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.8.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.8.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- **Read-Before-Write** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

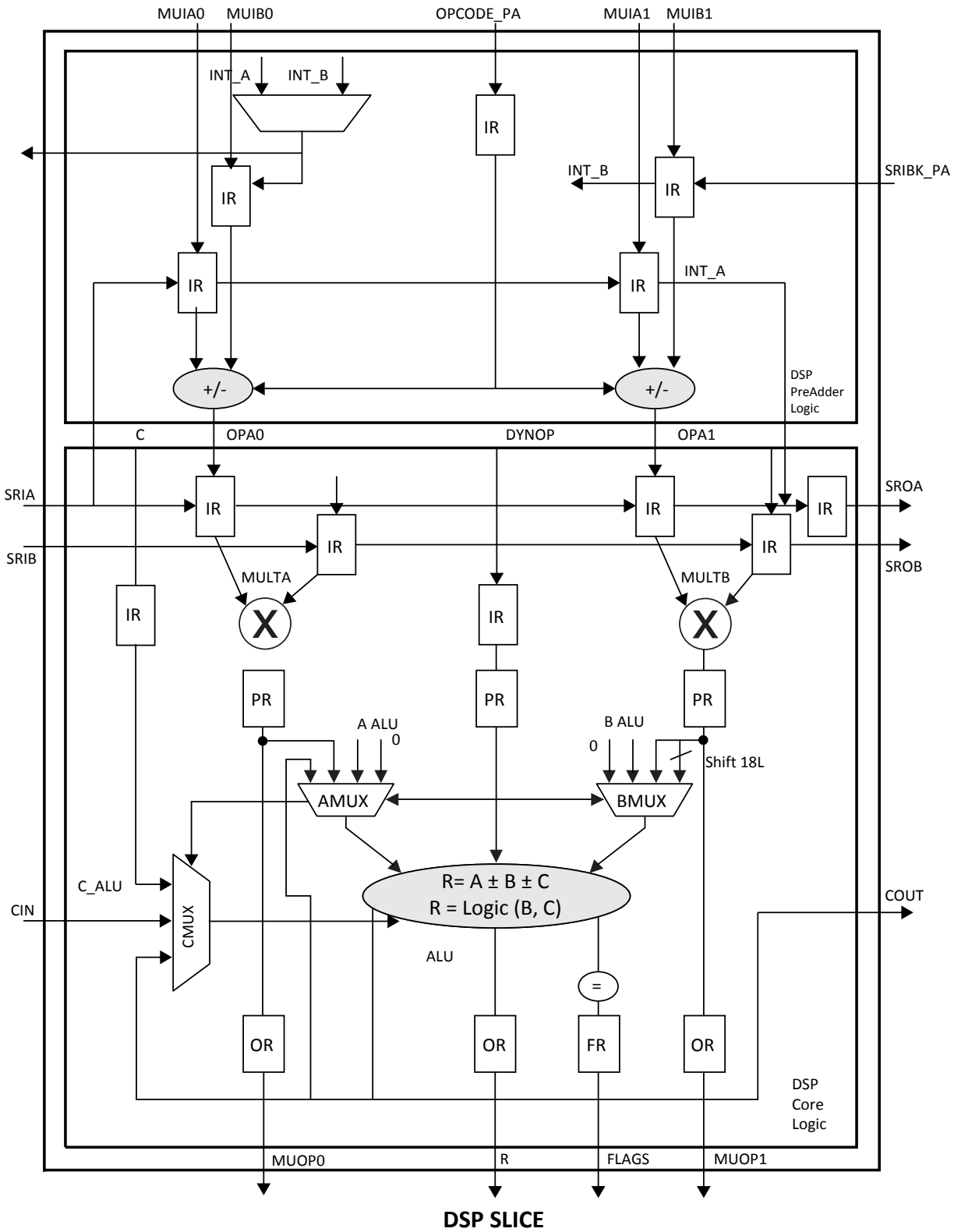


Figure 2.15. Detailed sysDSP Slice Diagram

2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in DDR Memory Support section on page 35.

Table 2.8. Input Block Port Description

Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in Figure 2.19. The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

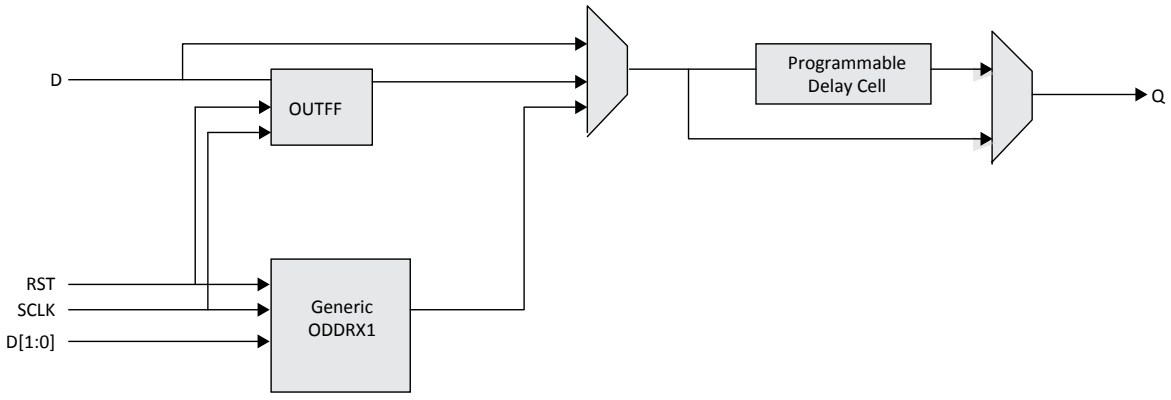


Figure 2.19. Output Register Block on Top Side

3.14. sysI/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.13. LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	±100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	±10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver outputs shorted to each other	—	—	12	mA

Note: On the left and right sides of the device, this specification is valid only for V_{CCIO} = 2.5 V or 3.3 V.

3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

Table 3.18. Input to SLVS

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.

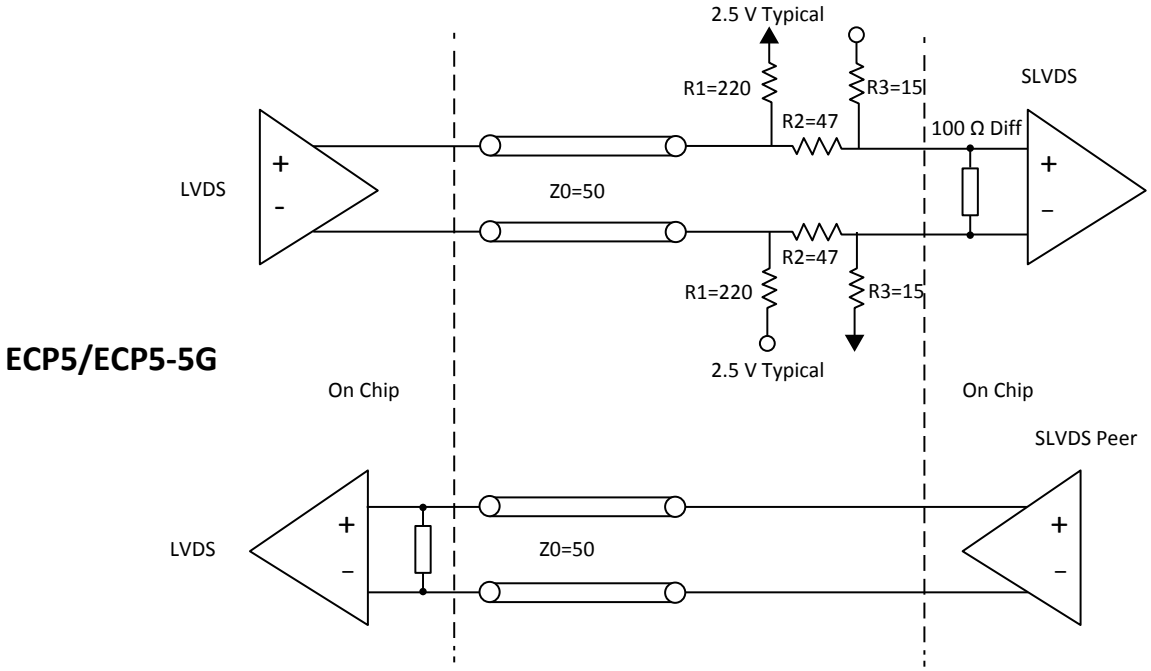


Figure 3.5. SLVS Interface

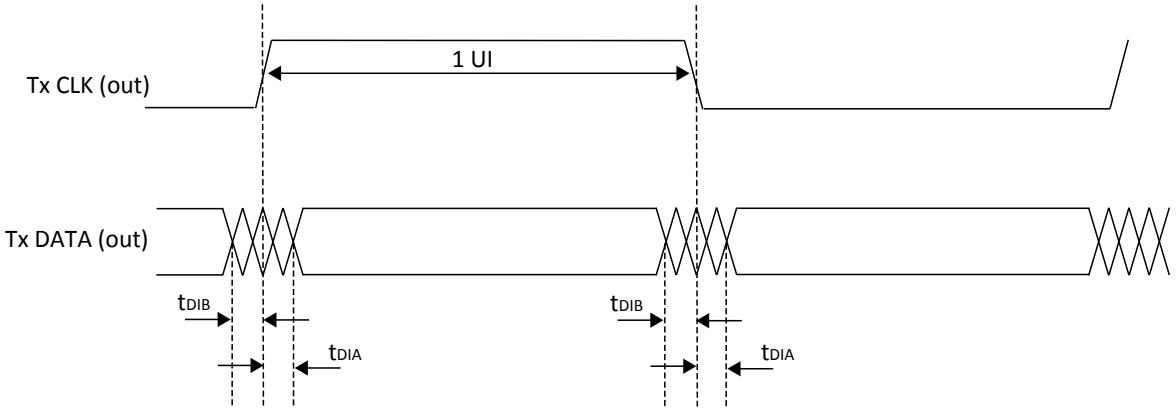
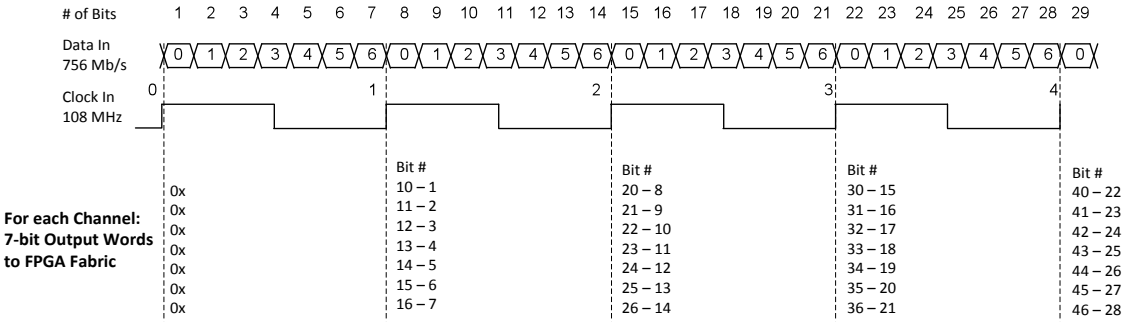


Figure 3.9. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter – Shown for one LVDS Channel

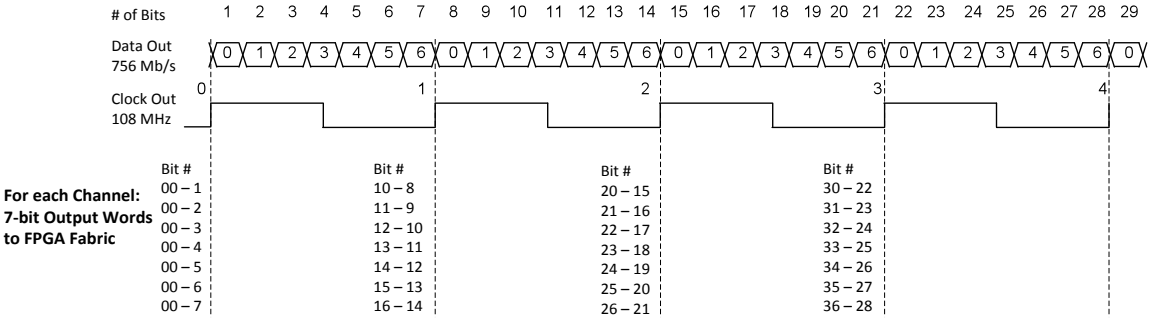


Figure 3.10. DDRX71 Video Timing Waveforms

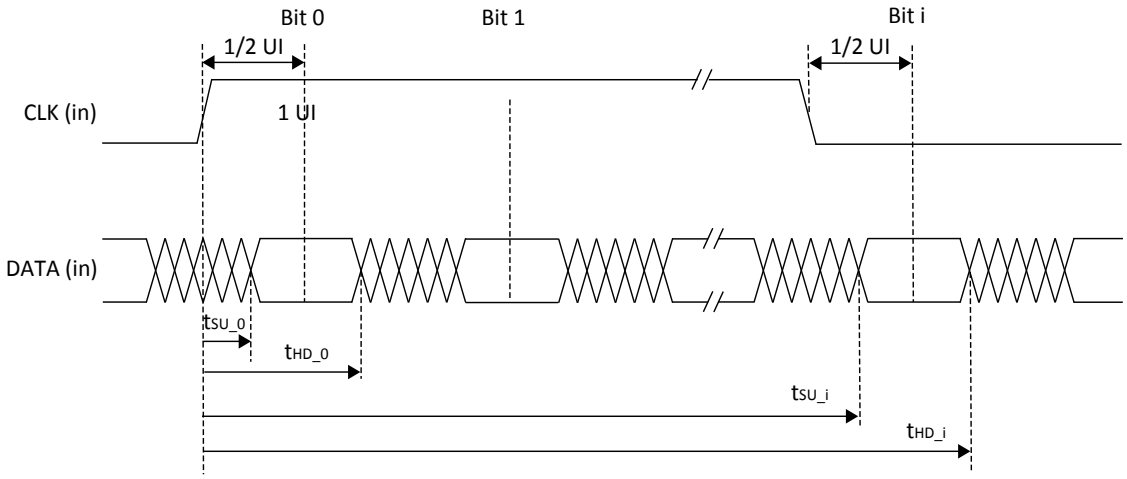


Figure 3.11. Receiver DDRX71_RX Waveforms

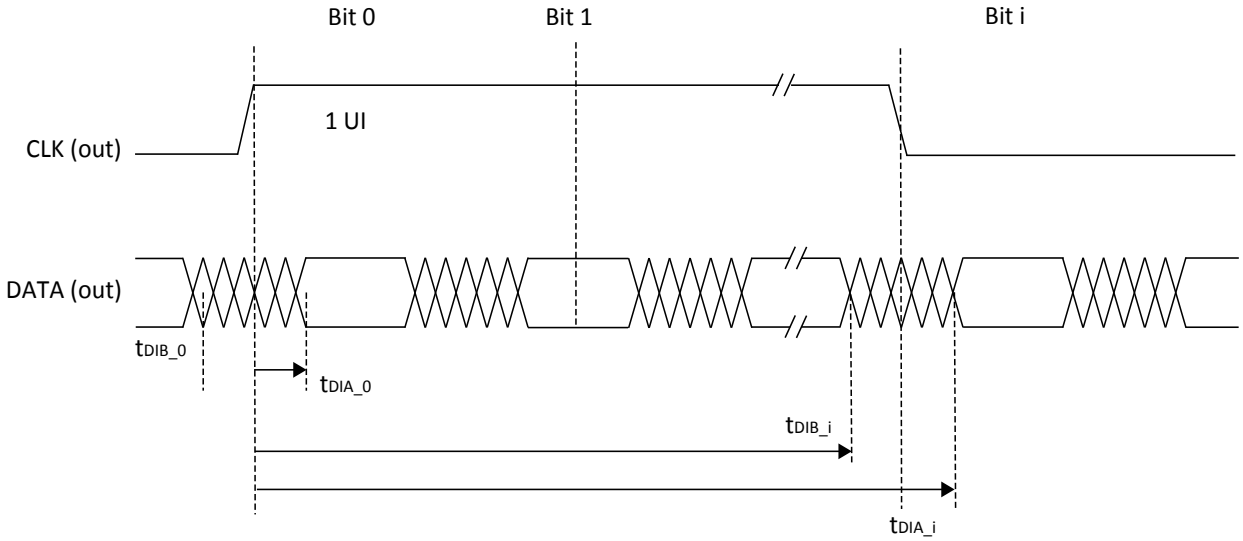


Figure 3.12. Transmitter DDRX71_TX Waveforms

3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 3.23. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
f_{VCO}	PLL VCO Frequency	—	400	800	MHz
f_{PFD}[3]	Phase Detector Input Frequency	—	10	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_W	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
t_{LOCK}[2]	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST/ Pulse Width	—	1	—	ms
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{LOAD_REG}	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain “0” or	—	4	—	VCO cycles

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit						
UI	Unit Interval	—	203.43	203.45	203.47	ps
T_{DCD}	Duty Cycle Distortion	—	—	—	0.05	UI
J_{UBHPJ}	Uncorrelated Bounded High Probability Jitter	—	—	—	0.15	UI
J_{TOTAL}	Total Jitter	—	—	—	0.3	UI
$Z_{RX-DIFF-DC}$	DC differential Impedance	—	80	—	120	Ω
T_{SKEW}	Skew between differential signals	—	—	—	9	ps
$R_{LTX-DIFF}$	Tx Differential Return Loss (S22), including package and silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	—	—	dB
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	100	mA
$T_{RISE\_FALL-DIFF}$	Differential Rise and Fall Time	—		—	—	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—		ps
Receive						
UI	Unit Interval	—	203.43	203.45	203.47	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	—	—	1.2	V, p-p
$V_{RX-EYE\_Y1\_Y2}$	Receiver eye opening mask, Y1 and Y2	—	62.5	—	375	mV, diff
V_{RX-EYE_X1}	Receiver eye opening mask, X1	—	—	—	0.3	UI
T_{RX-TJ}	Receiver total jitter tolerance (not including sinusoidal)	—	—	—	0.6	UI
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
$Z_{RX-DIFF-DC}$	Receiver DC differential impedance	—	80	100	120	Ω

Note: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.39. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDO}	Serial data rate	—	270	—	2975	Mb/s
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	270 Mb/s[6]	—	—	0.2	UI
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	1485 Mb/s	—	—	0.2	UI
$T_{JALIGNMENT}$[1, 2]	Serial output jitter, alignment	2970 Mb/s	—	—	0.3	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mb/s[6]	—	—	0.2	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mb/s	—	—	1	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mb/s	—	—	2	UI

Notes:
1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice SERDES device configured to 50 Ω output impedance connecting to the external cable driver with differential signaling.
4. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mb/s.
5. All LFE5UM/LFE5UM5G devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.
6. 270 Mb/s is supported with Rate Divider only.

Table 3.40. Receive

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDI}	Serial input data rate	—	270	—	2970	Mb/s

Table 3.41. Reference Clock

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F_{VCLK}	Video output clock frequency	—	54	—	148.5	MHz
DC_V	Duty cycle, video clock	—	45	50	55	%

Note: SD-SDI (270 Mb/s) is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

3.31. sysCONFIG Port Timing Specifications

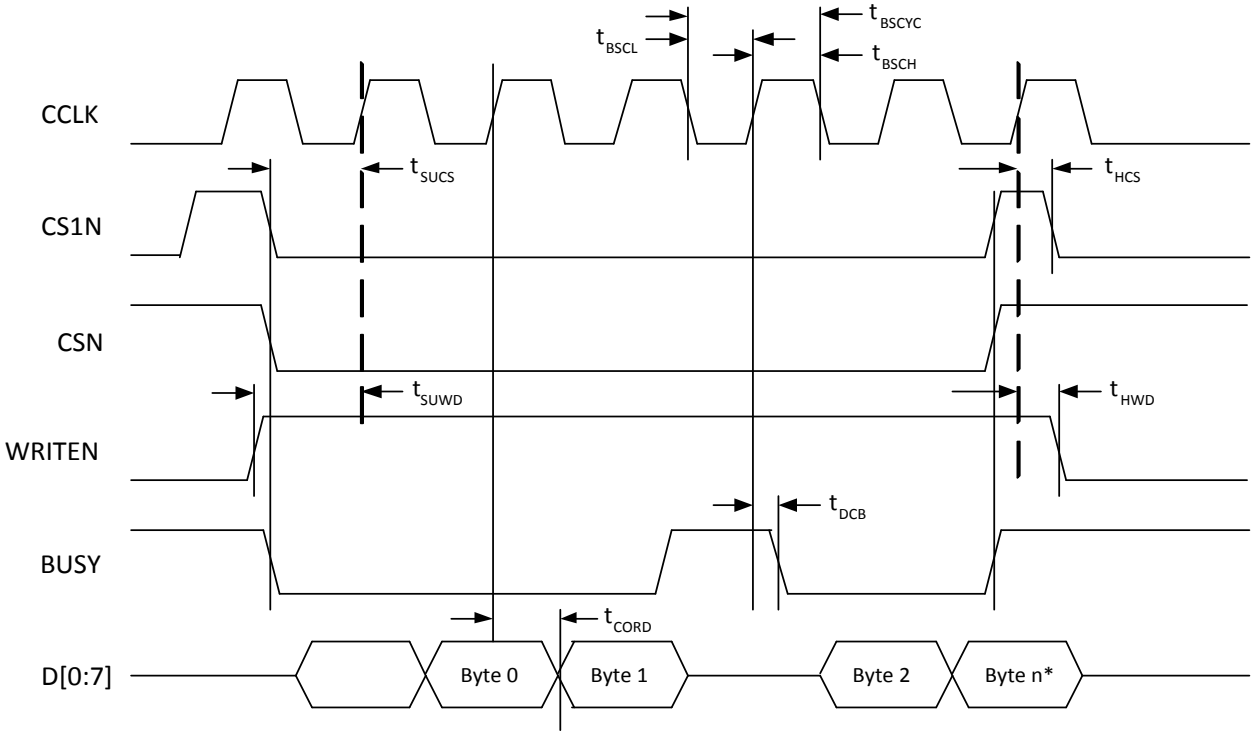
Over recommended operating conditions.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications

Symbol	Parameter		Min	Max	Unit
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC}, V_{CCAUX} or V_{CCIO8} (whichever is the last) to the rising edge of INITN	—	—	33	ms
t_{VMC}	Time from t_{ICFG} to the valid Master CCLK	—	—	5	us
t_{CZ}	CCLK from Active to High-Z	—	—	300	ns
Master CCLK					
f_{MCLK}	Frequency	All selected frequencies	–20	20	%
$t_{MCLK-DC}$	Duty Cycle	All selected frequencies	40	60	%
All Configuration Modes					
t_{PRGM}	PROGRAMN LOW pulse accepted	—	110	—	ns
t_{PRGMRJ}	PROGRAMN LOW pulse rejected	—	—	50	ns
t_{INITL}	INITN LOW time	—	—	55	ns
t_{DPPINT}	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	150	ns
Slave SPI					
f_{CCLK}	CCLK input clock frequency	—	—	60	MHz
t_{CCLKH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{CCLKL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{STSU}	CCLK setup time	—	1	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{STCO}	CCLK falling edge to valid output	—	—	10	ns
t_{STOZ}	CCLK falling edge to valid disable	—	—	10	ns
t_{STOV}	CCLK falling edge to valid enable	—	—	10	ns
t_{SCS}	Chip Select HIGH time	—	25	—	ns
t_{SCSS}	Chip Select setup time	—	3	—	ns
t_{SCSH}	Chip Select hold time	—	3	—	ns
Master SPI					
f_{CCLK}	Max selected CCLK output frequency	—	—	62	MHz
t_{CCLKH}	CCLK output clock pulse width HIGH	—	3.5	—	ns
t_{CCLKL}	CCLK output clock pulse width LOW	—	3.5	—	ns
t_{STSU}	CCLK setup time	—	5	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{CSSPI}	INITN HIGH to Chip Select LOW	—	100	200	ns
t_{CFGX}	INITN HIGH to first CCLK edge	—	—	150	ns
Slave Serial					
f_{CCLK}	CCLK input clock frequency	—	—	66	MHz
t_{SSCH}	CCLK input clock pulse width HIGH	—	5	—	ns
t_{SSCL}	CCLK input clock pulse width LOW	—	5	—	ns
t_{SUSCDI}	CCLK setup time	—	0.5	—	ns
t_{HSCDI}	CCLK hold time	—	1.5	—	ns

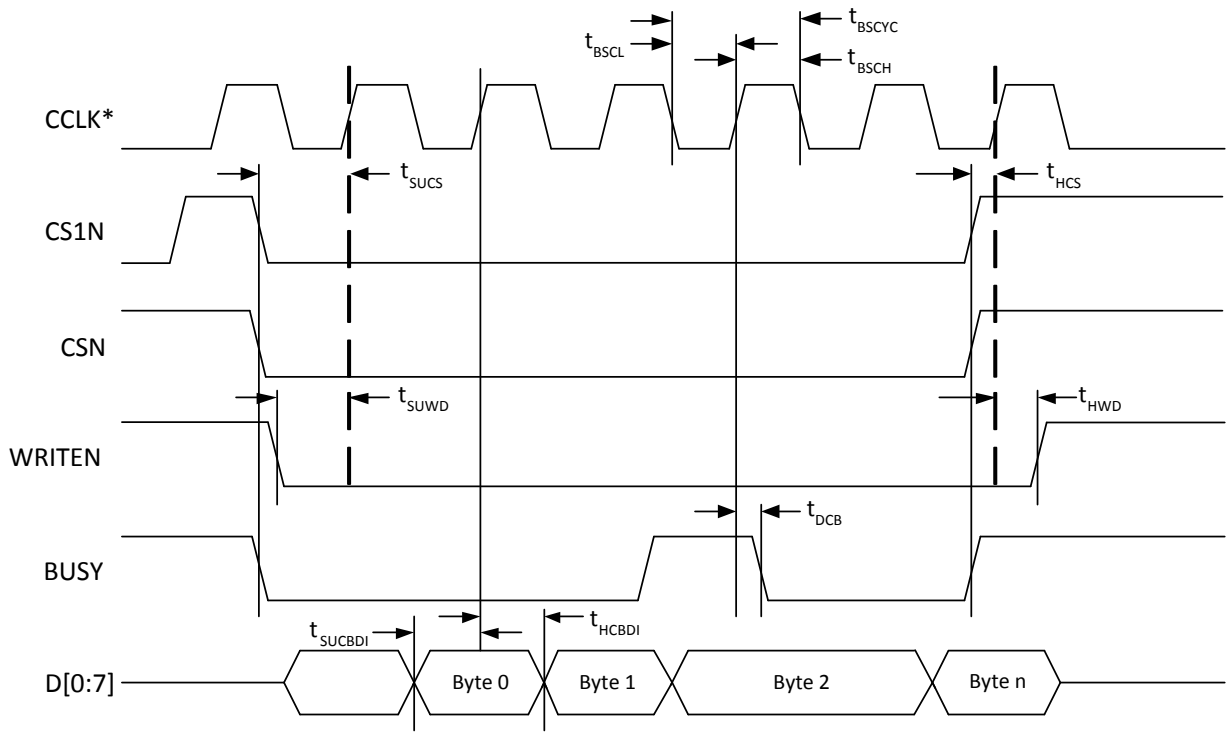
Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications *(Continued)*

Symbol	Parameter		Min	Max	Unit
Slave Parallel					
f_{CCLK}	CCLK input clock frequency	—	—	50	MHz
t_{BSCH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{BSCL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{CORD}	CCLK to DOUT for Read Data	—	—	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	—	1.5	—	ns
t_{HCBDI}	Data Hold Time to CCLK	—	1.5	—	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK	—	45	—	ns
t_{HCWD}	WRITEN Hold Time to CCLK	—	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	—	12	ns



*n = last byte of read cycle.

Figure 3.15. sysCONFIG Parallel Port Read Cycle



*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3.16. sysCONFIG Parallel Port Write Cycle

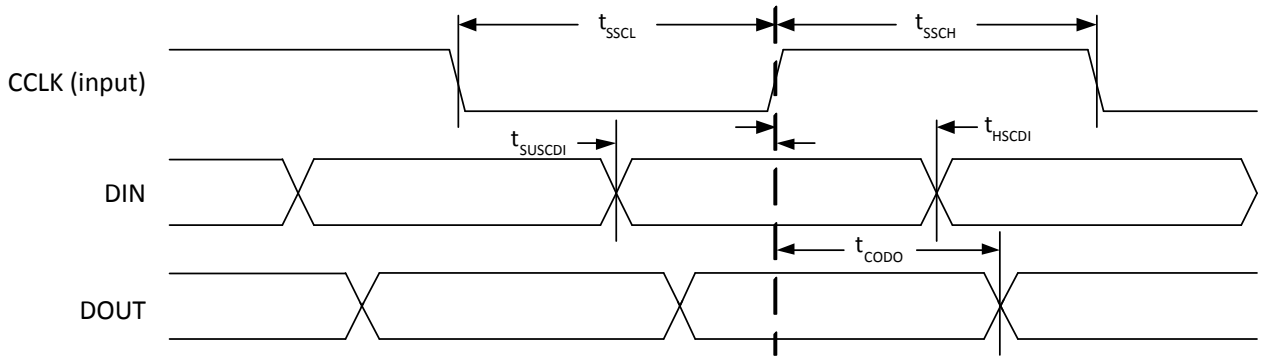


Figure 3.17. sysCONFIG Slave Serial Port Timing

Supplemental Information

For Further Information

A variety of technical notes for the ECP5/ECP5-5G family are available.

- High-Speed PCB Design Considerations (TN1033)
- Transmission of High-Speed Serial Signals Over Common Cable Media (TN1066)
- PCB Layout Recommendations for BGA Packages (TN1074)
- Minimizing System Interruption During Configuration Using TransFR Technology (TN1087)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- LatticeECP3, ECP-5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184)
- Using TraceID (TN1207)
- Sub-LVDS Signaling Using Lattice Devices (TN1210)
- Advanced Security Encryption Key Programming Guide for ECP5, ECP5-5G, LatticeECP3, and LatticeECP2/MS Devices (TN1215)
- LatticeECP3, LatticeECP2/M, ECP5 and ECP5-5G Dual Boot and Multiple Boot Feature (TN1216)
- ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260)
- ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261)
- ECP5 and ECP5-5G sysIO Usage Guide (TN1262)
- ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263)
- ECP5 and ECP5-5G Memory Usage Guide (TN1264)
- ECP5 and ECP5-5G High-Speed I/O Interface (TN1265)
- Power Consumption and Management for ECP5 and ECP5-5G Devices (TN1266)
- ECP5 and ECP5-5G sysDSP Usage Guide (TN1267)
- ECP5 and ECP5-5G Hardware Checklist (FPGA-TN-02038)
- Solder Reflow Guide for Surface Mount Devices (FPGA-TN-02041)
- ECP5 and ECP5-5G PCI Express Soft IP Ease of Use Guidelines (FPGA-TN-02045)
- Programming External SPI Flash through JTAG for ECP5/ECP5-5G (FPGA-TN-02050)
- Adding Scalable Power and Thermal Management to ECP5 Using L-ASC10 (AN6095)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL): www.jedec.org
- PCI: www.pcisig.com

(Continued)

Date	Version	Section	Change Summary
April 2017	1.7	All	Changed document number from DS1044 to FPGA-DS-02012.
		General Description	Updated Features section. Changed “1.1 V core power supply” to “1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G”.
		Architecture	Updated Overview section. Change “The ECP5/ECP5-5G devices use 1.1 V as their core voltage” to “The ECP5 devices use 1.1V, ECP5UM5G devices use 1.2V as their core voltage”
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions Added ECP5-5G on VCC to be 1.2V +/- 5% Added ECP5-5G on VCCA to be 1.2V +/- 3% Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) Changed “Core Power Supply Current” for ICC on LFE5UM5G devices Changed “SERDES Power Supply Current (Per Dual)” for ICCA on LFE5UM5G devices Updated Table 3.20. Register-to-Register Performance. Remove “(DDR/SDR)” from DSP Function Changed DSP functions to 225 MHz
		Pinout Information	Update Section 4.1 Signal Description. Revised Vcc Description to “Power supply pins for core logic. Dedicated pins. VCC = 1.1 V (ECP5), 1.2 V (ECP5UM5G)”
February 2016	1.6	All	Changed document status from Preliminary to Final.
		General Description	Updated Features section. Changed “24K to 84K LUTs” to “12K to 84K LUTs”. Added LFE5U-12 column to Table 1.1. ECP5 and ECP5-5G Family Selection Guide.
		DC and Switching Characteristics	Updated Power up Sequence section. Identified typical ICC current for specific devices in Table 3.8. ECP5/ECP5-5G Supply Current (Standby). Updated values in Table 3.9. ECP5. Updated values in Table 3.10. ECP5-5G. Added values to –8 Timing column of Table 3.19. Pin-to-Pin Performance. Added values to –8 Timing column of Table 3.20. Register-to-Register Performance. Changed LFE5-45 to All Devices in Table 3.22. ECP5/ECP5-5G External Switching Characteristics. Added table notes to Table 3.31. PCIe (5 Gb/s). Added table note to Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics.
		Pinout Information	Added LFE5U-12 column to the table in LFE5U section.
		Ordering Information	Updated LFE5U in ECP5/ECP5-5G Part Number Description section: added 12 F = 12K LUTs to Logic Capacity. Added LFE5U-12F information to Ordering Part Numbers section.