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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-8mg285c

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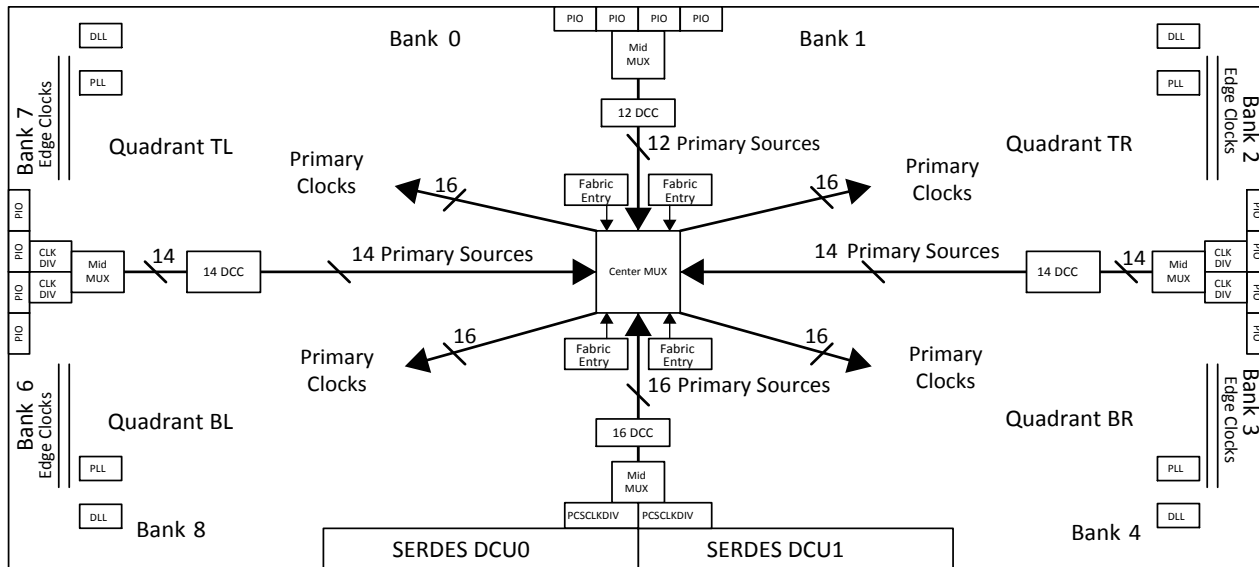


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in [DDR Memory Support](#) section on page 35.

Table 2.8. Input Block Port Description

Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in [Figure 2.19](#). The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

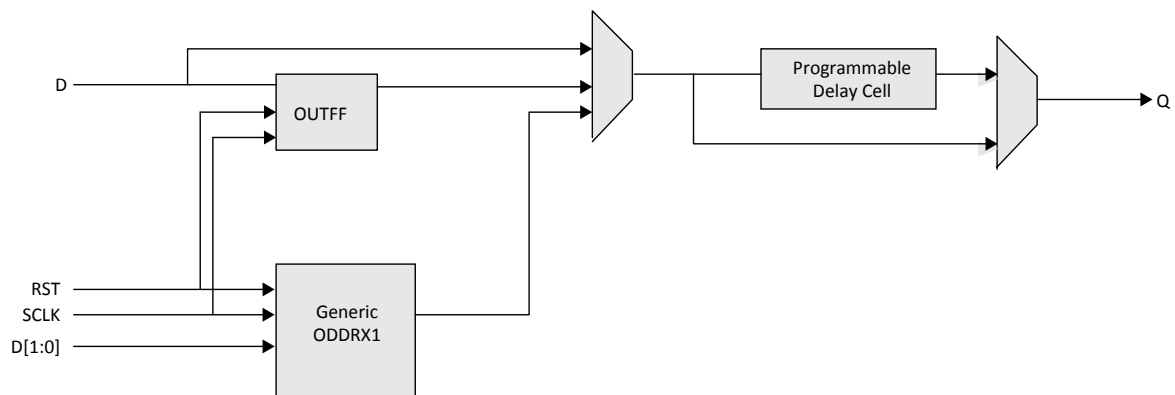
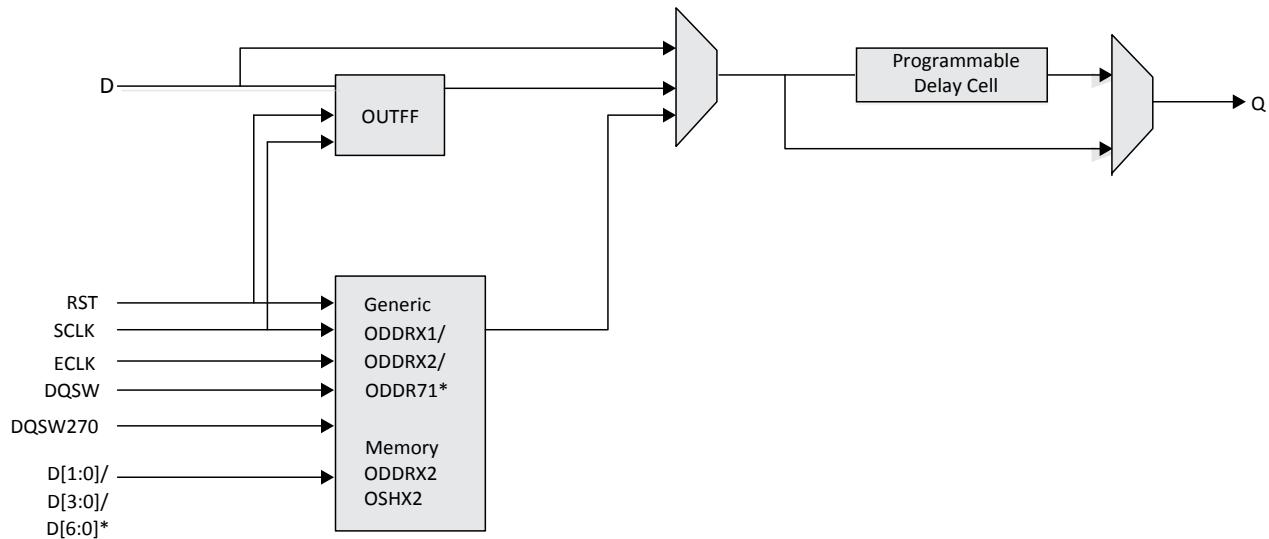


Figure 2.19. Output Register Block on Top Side



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

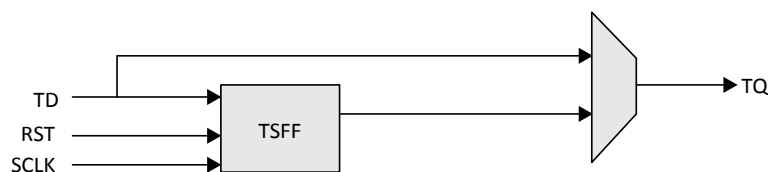


Figure 2.21. Tristate Register Block on Top Side

2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω , 75 Ω , or 150 Ω .
- Common mode termination of 100 Ω for differential inputs.

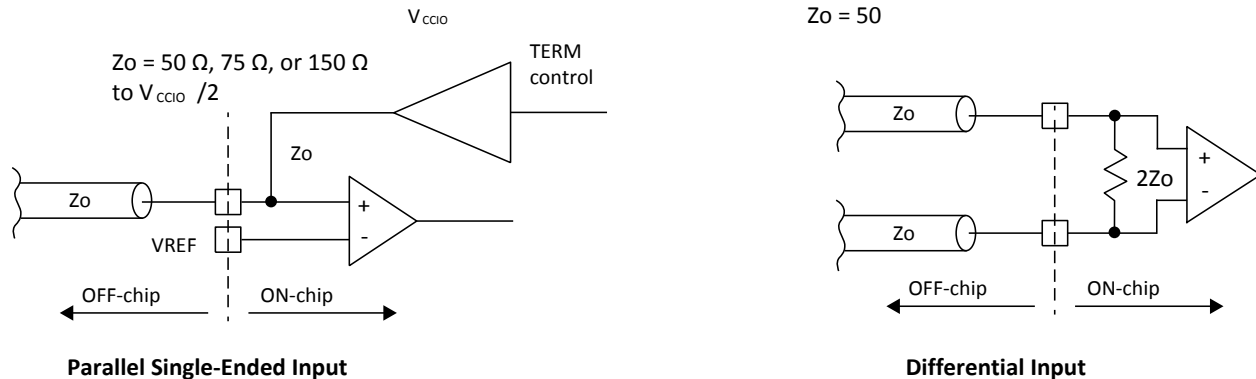


Figure 2.26. On-Chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2^*$	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Notes:**

TERMINATE to $V_{CCIO}/2$ (Single-Ended) and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance $\pm 20\%$.

Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for on-chip termination usage and value ranges.

2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the [Hot Socketing Specifications](#) section on page 48.

2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. [Figure 2.27](#) shows the position of the dual blocks for the LFE5-85. [Table 2.13](#) shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).

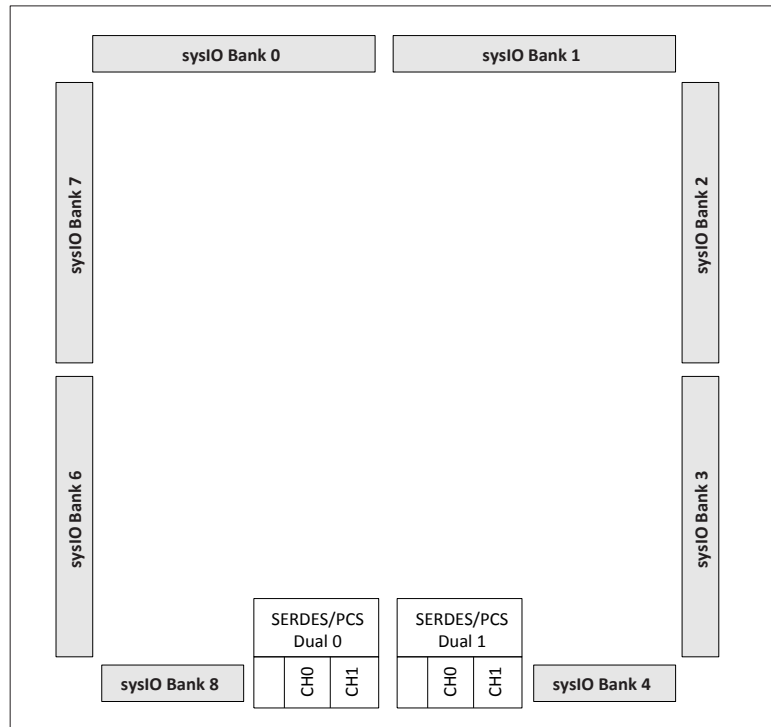


Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 ²	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 ²	x1	8b10b
SD-SDI (259M, 344M) ¹	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5	x1	NRZI/Scrambled
	1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	—	—
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to [LatticeECP3, ECP5 and ECP5-5G Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide \(TN1184\)](#).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. [Table 2.16](#) lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#) and [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

Table 3.10. ECP5-5G

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I _{CCA-SB}	V _{CCA} Power Supply Current (Per Channel)	4	9.5	mA
I _{CCHRX-SB} ⁴	V _{CCHRX} , Input Buffer Current (Per Channel)	—	0.1	mA
I _{CCHTX-SB}	V _{CCHTX} , Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 5 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	58	67	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 3.2 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	48	57	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	44	53	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	36	46	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
I _{CCA-OP}	V _{CCA} Power Supply Current (Per Channel)	30	40	mA
I _{CCHRX-OP} ⁵	V _{CCHRX} , Input Buffer Current (Per Channel)	0.4	0.5	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For I_{CCHRX-SB}, during Standby, input termination on Rx are disabled.
5. For I_{CCHRX-OP}, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

Table 3.20. Register-to-Register Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	441	MHz
32-Bit Decoder	441	MHz
64-Bit Decoder	332	MHz
4:1 Mux	441	MHz
8:1 Mux	441	MHz
16:1 Mux	441	MHz
32:1 Mux	441	MHz
8-Bit Adder	441	MHz
16-Bit Adder	441	MHz
64-Bit Adder	441	MHz
16-Bit Counter	384	MHz
32-Bit Counter	317	MHz
64-Bit Counter	263	MHz
64-Bit Accumulator	288	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	214	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	441	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	441	MHz
DSP Functions		
9 x 9 Multiplier (All Registers)	225	MHz
18 x 18 Multiplier (All Registers)	225	MHz
36 x 36 Multiplier (All Registers)	225	MHz
18 x 18 Multiply-Add/Sub (All Registers)	225	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	225	MHz

Notes:

- These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
- Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
f _{DATA_DDR2} f _{DATA_DDR3} f _{DATA_DDR3L} f _{DATA_LPDDR2} f _{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	800	—	700	—	624	Mb/s
f _{MAX_DDR2} f _{MAX_DDR3} f _{MAX_DDR3L} f _{MAX_LPDDR2} f _{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS)									
t _{DQVBS_DDR2} t _{DQVBS_DDR3} t _{DQVBS_DDR3L} t _{DQVBS_LPDDR2} t _{DQVBS_LPDDR3}	Data Output Valid before DQS Output	All Devices	—	–0.25	—	–0.25	—	–0.25	UI
t _{DQVAS_DDR2} t _{DQVAS_DDR3} t _{DQVAS_DDR3L} t _{DQVAS_LPDDR2} t _{DQVAS_LPDDR3}	Data Output Valid after DQS Output	All Devices	0.25	—	0.25	—	0.25	—	UI
f _{DATA_DDR2} f _{DATA_DDR3} f _{DATA_DDR3L} f _{DATA_LPDDR2} f _{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	800	—	700	—	624	Mb/s
f _{MAX_DDR2} f _{MAX_DDR3} f _{MAX_DDR3L} f _{MAX_LPDDR2} f _{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz

Notes:

- Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.
- General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load.
Generic DDR timing are numbers based on LVDS I/O.
DDR2 timing numbers are based on SSTL18.
DDR3 timing numbers are based on SSTL15.
LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
- Uses LVDS I/O standard for measurements.
- Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- All numbers are generated with the Diamond software.

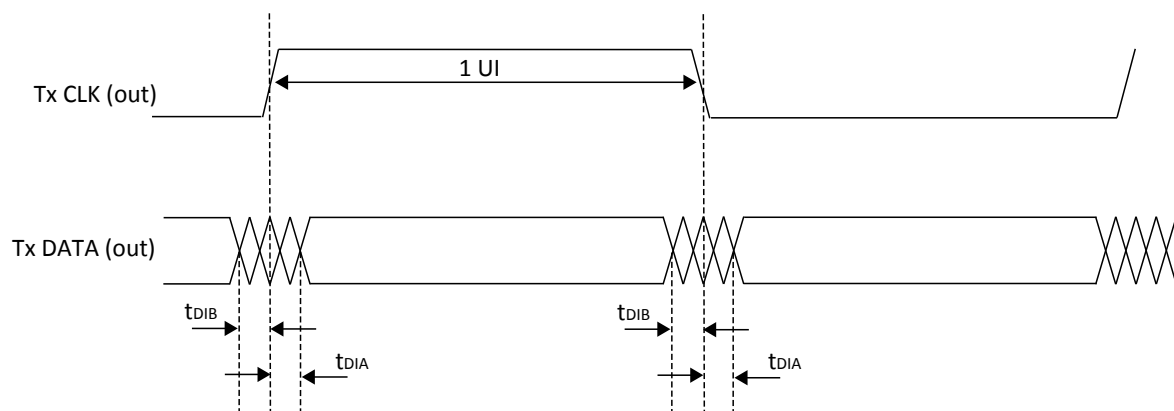
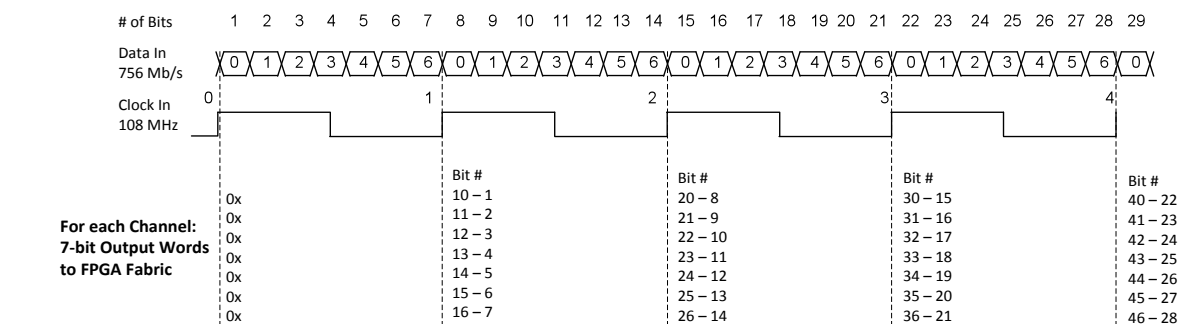


Figure 3.9. Transmit TX.CLK.Aligned Waveforms

Receiver – Shown for one LVDS Channel



Transmitter – Shown for one LVDS Channel

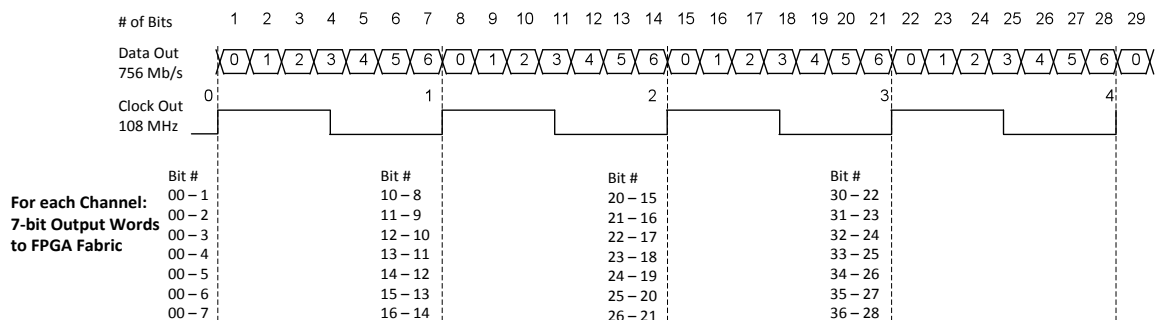


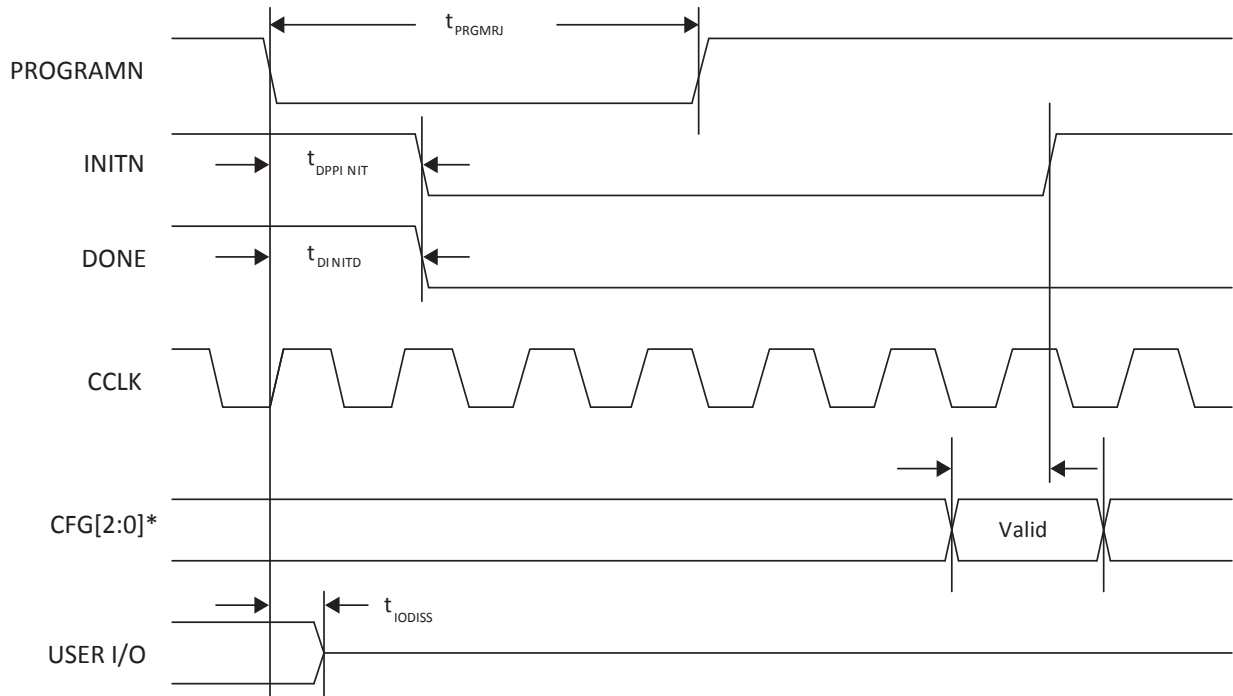
Figure 3.10. DDRX71 Video Timing Waveforms

3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

Table 3.31. PCIe (5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit¹						
UI	Unit Interval	—	199.94	200	200.06	ps
B _{WTX-PKG-PLL2}	Tx PLL bandwidth corresponding to PKGTx-PLL2	—	5	—	16	MHz
P _{KGTx-PLL2}	Tx PLL Peaking	—	—	—	1	dB
V _{TX-DIFF-PP}	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
V _{TX-DIFF-PP-LOW}	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
V _{TX-DE-RATIO-3.5dB}	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
V _{TX-DE-RATIO-6dB}	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
T _{MIN-PULSE}	Instantaneous lone pulse width	—	—	—	—	UI
T _{TX-RISE-FALL}	Transmitter rise and fall time	—	—	—	—	UI
T _{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T _{TX-DJ}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T _{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
T _{RF-MISMATCH}	Tx rise/fall time mismatch	—	—	—	—	UI
R _{LTX-DIFF}	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R _{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
Z _{TX-DIFF-DC}	DC differential Impedance	—	—	—	120	Ω
V _{TX-CM-AC-PP}	Tx AC peak common mode voltage, peak-peak	—	—	—	—	mV, p-p
I _{TX-SHORT}	Transmitter short-circuit current	—	—	—	90	mA
V _{TX-DC-CM}	Transmitter DC common-mode voltage	—	0	—	1.2	V
V _{TX-IDLE-DIFF-DC}	Electrical Idle Output DC voltage	—	0	—	5	mV
V _{TX-IDLE-DIFF-AC-p}	Electrical Idle Differential Output peak voltage	—	—	—	—	mV
V _{TX-RCV-DETECT}	Voltage change allowed during Receiver Detect	—	—	—	600	mV
T _{TX-IDLE-MIN}	Min. time in Electrical Idle	—	20	—	—	ns
T _{TX-IDLE-SET-TO-IDLE}	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
T _{TX-IDLE-TO-DIFF-DATA}	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
L _{TX-SKEW}	Lane-to-lane output skew	—	—	—	—	ps



*The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

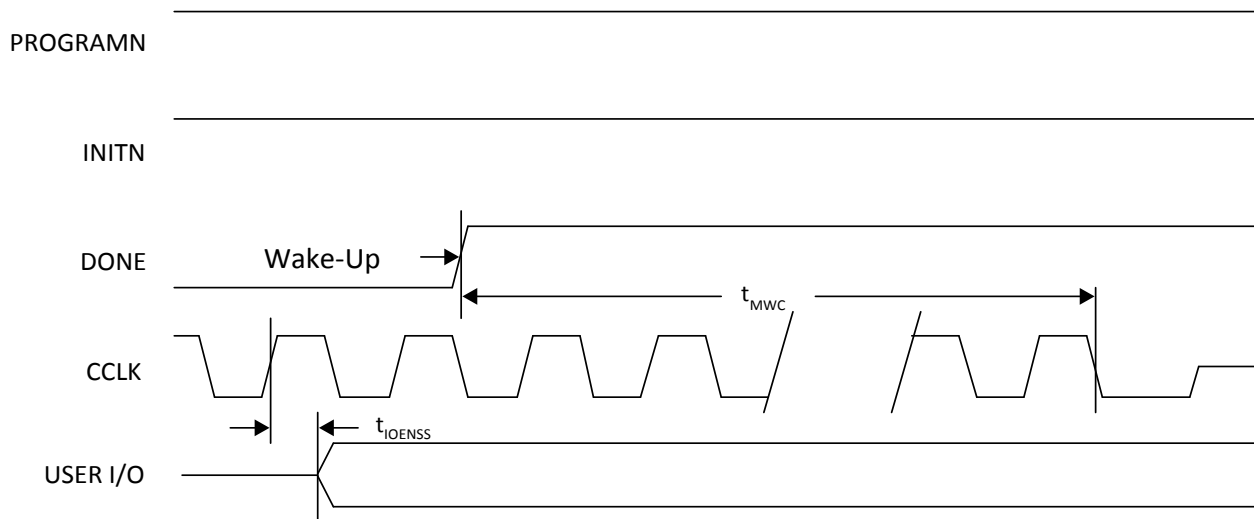


Figure 3.21. Wake-Up Timing

Table 3.44. Test Fixture Required Components, Non-Terminated Interfaces

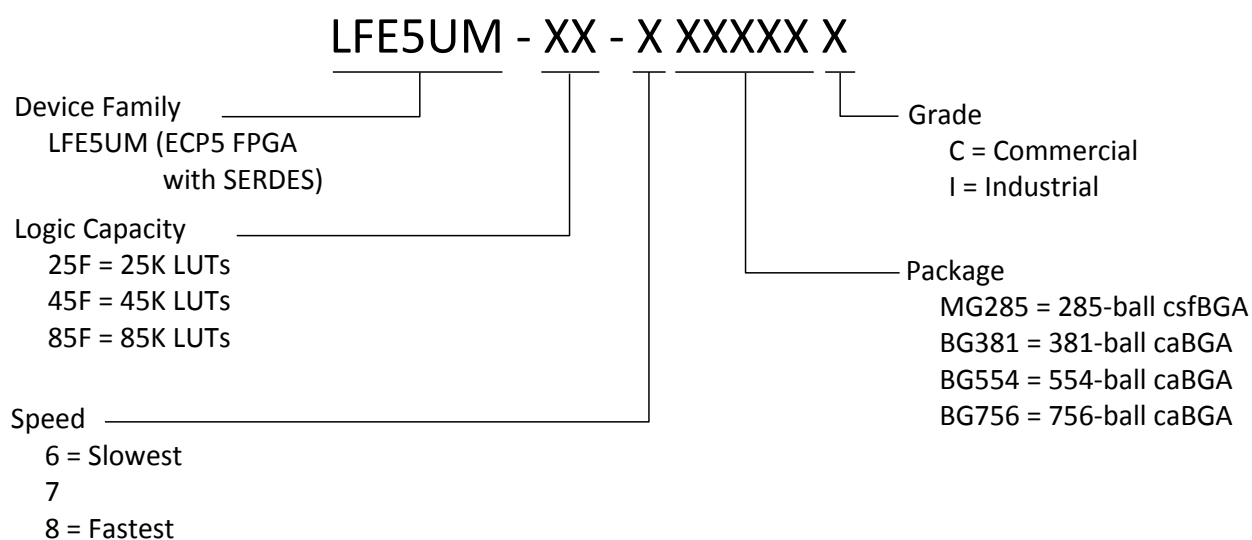
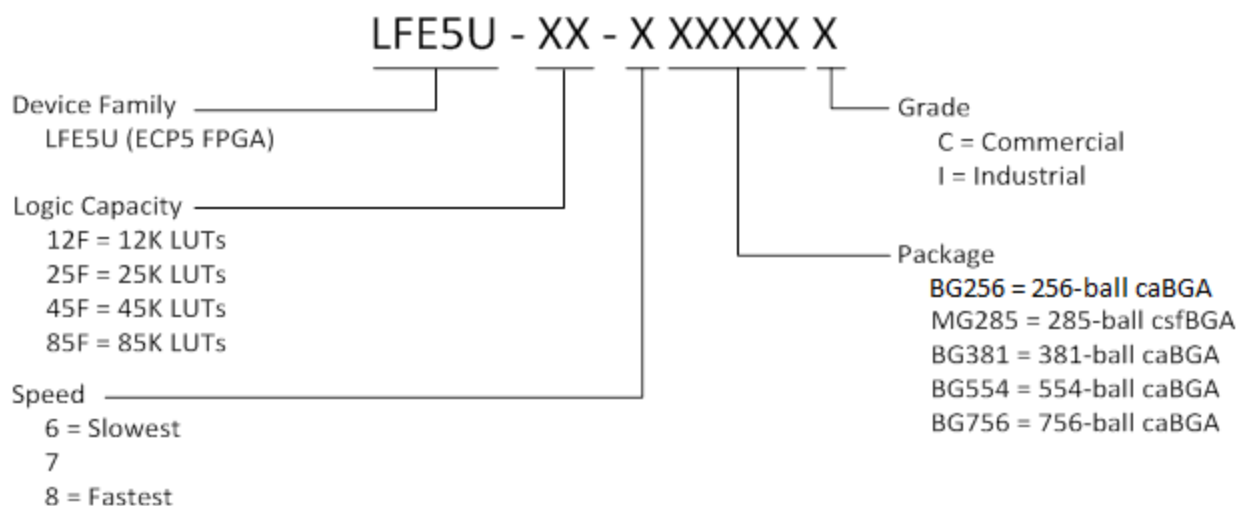
Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V _{OH} – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

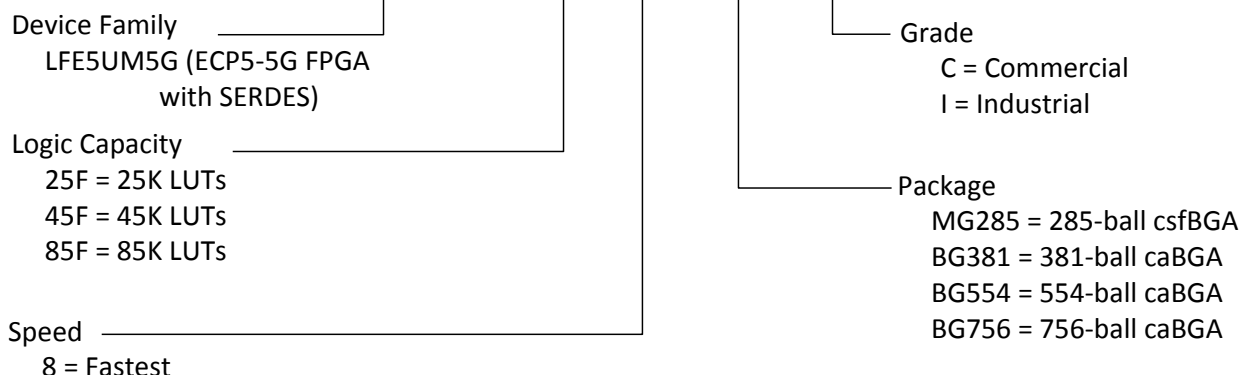
Signal Name	I/O	Description
PLL, DLL and Clock Functions (Continued)		
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
[T/R]]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. This is a dedicated input pin.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.
Configuration Pads (Used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes (Master SPI, Master Serial). This is a dedicated pin.
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPI mode data output. This is a shared I/O pin. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DOUT/CSO	O	Serial data output. Chip select output. SPI/SPI mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O
DO/MOSI/IOO	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.

5. Ordering Information

5.1. ECP5/ECP5-5G Part Number Description



LFE5UM5G - XX - X XXXXX X



5.2. Ordering Part Numbers

5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	-6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	-7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	-8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	-6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	-7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	-8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	-6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	-7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	-8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	-6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	-7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	-8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	-6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	-7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	-8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	No

(Continued)

Date	Version	Section	Change Summary
April 2017	1.7	All	Changed document number from DS1044 to FPGA-DS-02012.
		General Description	Updated Features section. Changed “1.1 V core power supply” to “1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G”.
		Architecture	Updated Overview section. Change “The ECP5/ECP5-5G devices use 1.1 V as their core voltage” to “The ECP5 devices use 1.1V, ECP5UM5G devices use 1.2V as their core voltage”
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions Added ECP5-5G on VCC to be 1.2V +/- 5% Added ECP5-5G on VCCA to be 1.2V +/- 3% Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) Changed “Core Power Supply Current” for ICC on LFE5UM5G devices Changed “SERDES Power Supply Current (Per Dual)” for ICCA on LFE5UM5G devices Updated Table 3.20. Register-to-Register Performance. Remove “(DDR/SDR)” from DSP Function Changed DSP functions to 225 MHz
		Pinout Information	Update Section 4.1 Signal Description. Revised Vcc Description to “Power supply pins for core logic. Dedicated pins. VCC = 1.1 V (ECP5), 1.2 V (ECP5UM5G)”
February 2016	1.6	All	Changed document status from Preliminary to Final.
		General Description	Updated Features section. Changed “24K to 84K LUTs” to “12K to 84K LUTs”. Added LFE5U-12 column to Table 1.1. ECP5 and ECP5-5G Family Selection Guide.
		DC and Switching Characteristics	Updated Power up Sequence section. Identified typical ICC current for specific devices in Table 3.8. ECP5/ECP5-5G Supply Current (Standby). Updated values in Table 3.9. ECP5. Updated values in Table 3.10. ECP5-5G. Added values to –8 Timing column of Table 3.19. Pin-to-Pin Performance. Added values to –8 Timing column of Table 3.20. Register-to-Register Performance. Changed LFE5-45 to All Devices in Table 3.22. ECP5/ECP5-5G External Switching Characteristics. Added table notes to Table 3.31. PCIe (5 Gb/s). Added table note to Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics.
		Pinout Information	Added LFE5U-12 column to the table in LFE5U section.
		Ordering Information	Updated LFE5U in ECP5/ECP5-5G Part Number Description section: added 12 F = 12K LUTs to Logic Capacity. Added LFE5U-12F information to Ordering Part Numbers section.