Lattice Semiconductor Corporation - LFE5UM-45F-8MG285I Datasheet

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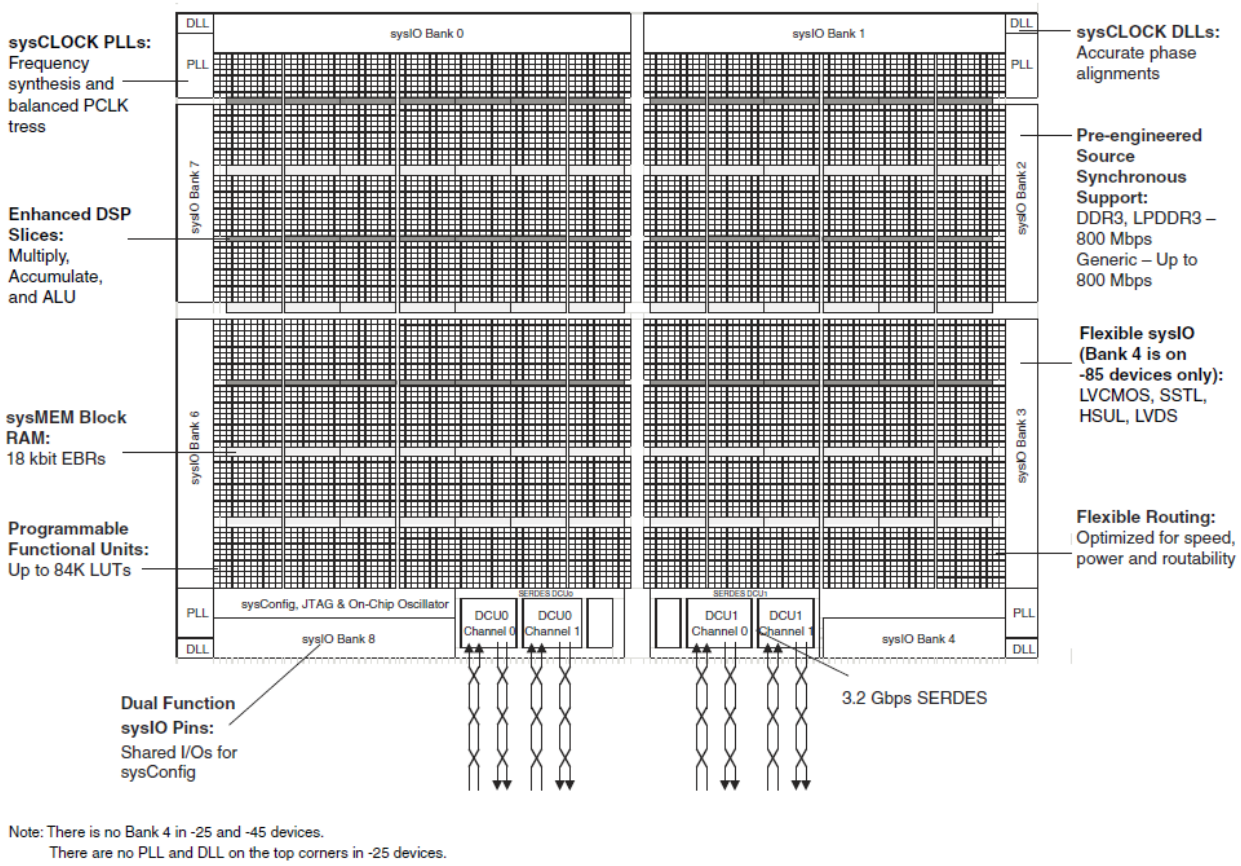
Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11000
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-45f-8mg285i



Note: There is no Bank 4 in -25 and -45 devices.
There are no PLL and DLL on the top corners in -25 devices.

Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

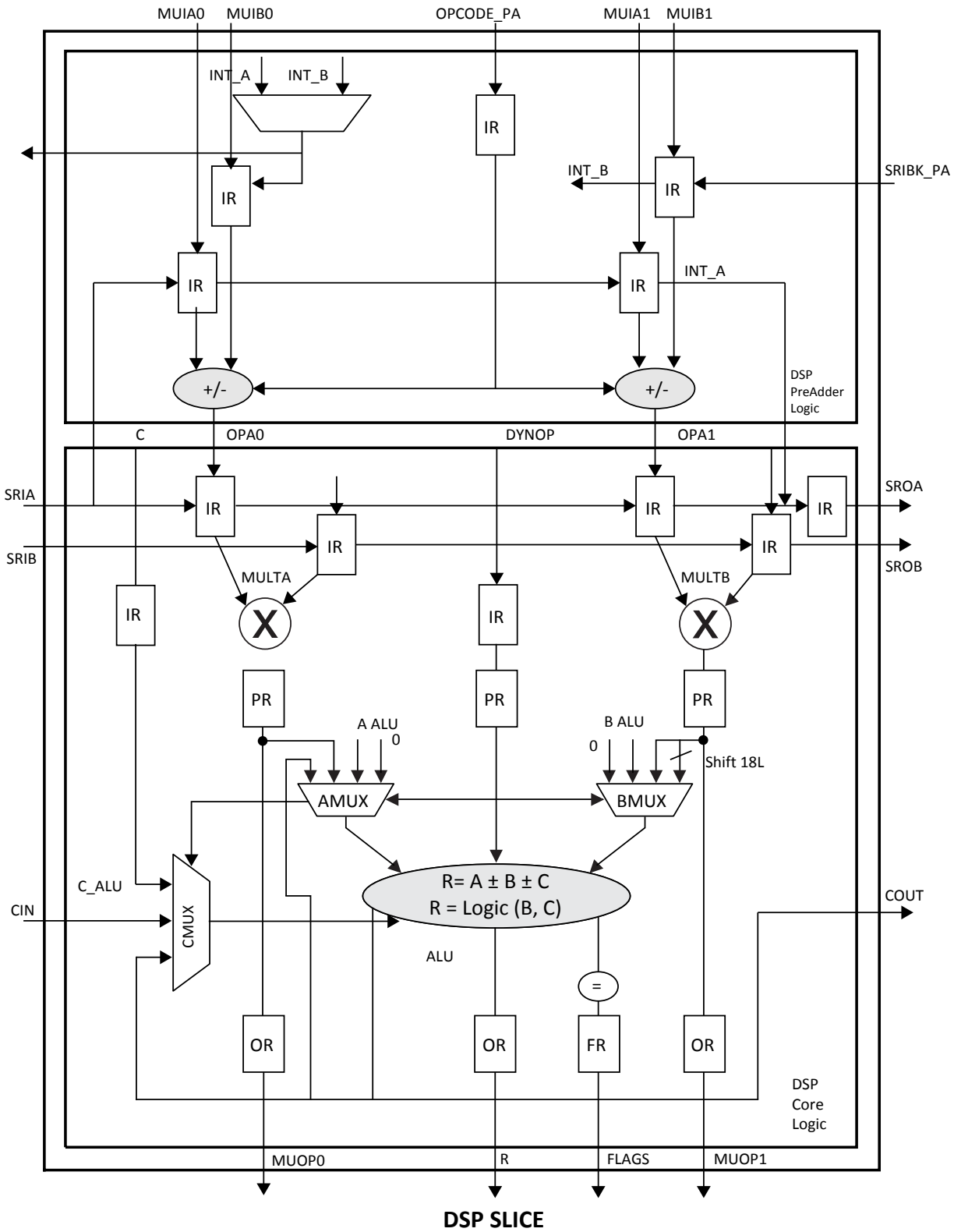


Figure 2.15. Detailed sysDSP Slice Diagram

2.11.1.1. Input FIFO

The ECP5/ECP5-5G PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in DDR Memory Support section on page 35.

Table 2.8. Input Block Port Description

Name	Type	Description
D	Input	High Speed Data Input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low Speed Data to the device core
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQS	Input	Clock from DQS control Block used to clock DDR memory data
ALIGNWD	Input	Data Alignment signal from device core.

2.11.2. Output Register Block

The output register block registers signal from the core of the device before they are passed to the sysIO buffers.

ECP5/ECP5-5G output data path has output programmable flip flops and output gearing logic. On the left and right sides, the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks support 1x gearing. ECP5/ECP5-5G output data path diagram is shown in Figure 2.19. The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

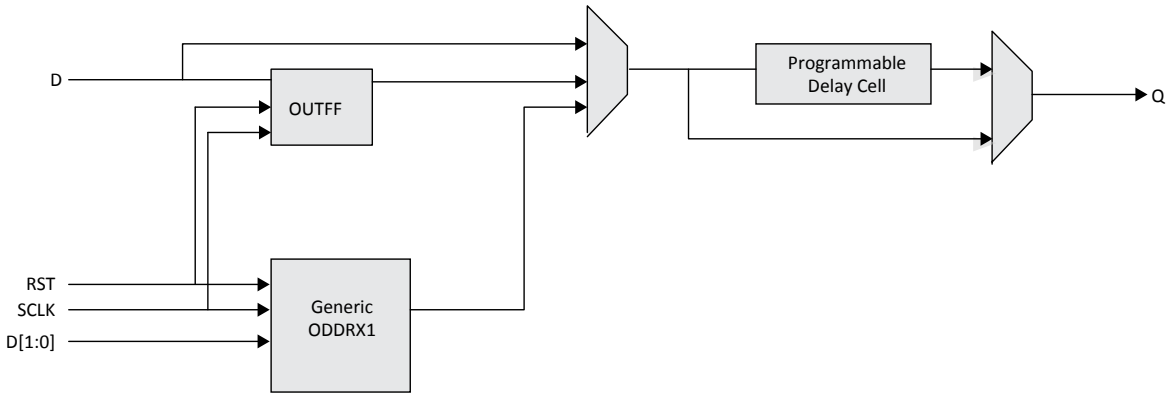


Figure 2.19. Output Register Block on Top Side

2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.

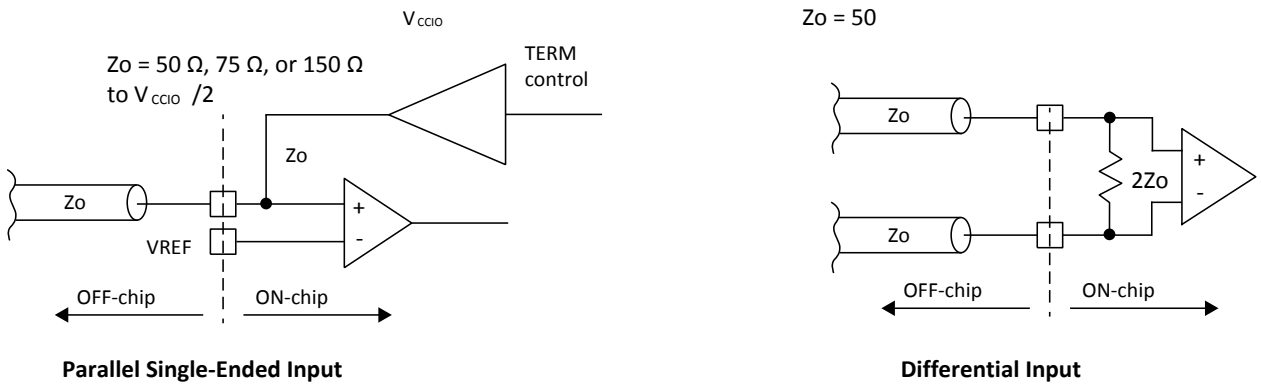


Figure 2.26. On-Chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2$*	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Notes**:

TERMINATE to $V_{CCIO}/2$ (Single-Ended) and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance ±20%.

Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for on-chip termination usage and value ranges.

2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the Hot Socketing Specifications section on page 48.

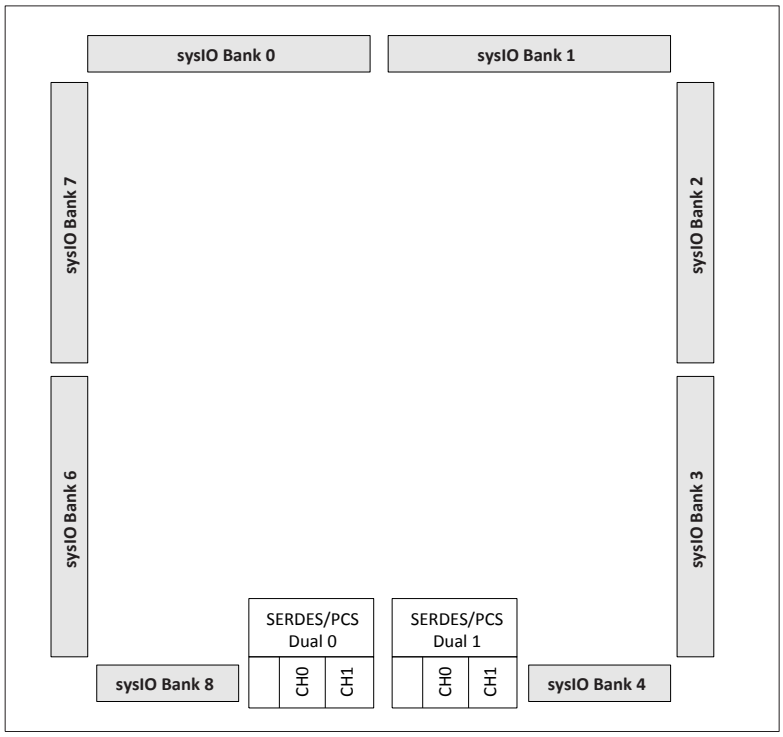


Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 [2]	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 [2]	x1	8b10b
SD-SDI (259M, 344M) [1]	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	—	—
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.

2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2.15 lists the allowable combination of primary and secondary protocol combinations.

2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

Table 2.15 lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.15. Typical Building Block Function Performance

Table 3.19. Pin-to-Pin Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	5.06	ns
32-Bit Decoder	6.08	ns
64-Bit Decoder	5.06	ns
4:1 Mux	4.45	ns
8:1 Mux	4.63	ns
16:1 Mux	4.81	ns
32:1 Mux	4.85	ns

Notes:

1. I/Os are configured with LVCMOS25 with V_{CCIO}=2.5, 12 mA drive.
2. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
3. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss (without package)	—	—	–10	dB

Notes:
1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Notes:
1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit						
UI	Unit Interval	—	203.43	203.45	203.47	ps
T_{DCD}	Duty Cycle Distortion	—	—	—	0.05	UI
J_{UBHPJ}	Uncorrelated Bounded High Probability Jitter	—	—	—	0.15	UI
J_{TOTAL}	Total Jitter	—	—	—	0.3	UI
$Z_{RX-DIFF-DC}$	DC differential Impedance	—	80	—	120	Ω
T_{SKEW}	Skew between differential signals	—	—	—	9	ps
$R_{LTX-DIFF}$	Tx Differential Return Loss (S22), including package and silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	—	—	dB
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	100	mA
$T_{RISE\_FALL-DIFF}$	Differential Rise and Fall Time	—		—	—	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—		ps
Receive						
UI	Unit Interval	—	203.43	203.45	203.47	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	—	—	1.2	V, p-p
$V_{RX-EYE\_Y1\_Y2}$	Receiver eye opening mask, Y1 and Y2	—	62.5	—	375	mV, diff
V_{RX-EYE_X1}	Receiver eye opening mask, X1	—	—	—	0.3	UI
T_{RX-TJ}	Receiver total jitter tolerance (not including sinusoidal)	—	—	—	0.6	UI
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
$Z_{RX-DIFF-DC}$	Receiver DC differential impedance	—	80	100	120	Ω

Note: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

Table 3.36. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J_{RX_DJ}[2, 3, 4]	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J_{RX_RJ}[2, 3, 4]	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J_{RX_SJ}[2, 3, 4]	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J_{RX_TJ}[1, 2, 3, 4]	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening	—	0.35	—	—	UI

Notes:
1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.29. Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics

3.29.1. AC and DC Characteristics

Table 3.37. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	Ω
J_{TX_DDJ}[2, 3]	Output data deterministic jitter	—	—	—	0.10	UI
J_{TX_TJ}[1, 2, 3]	Total output data jitter	—	—	—	0.24	UI

Notes:
1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.38. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J_{RX_DJ}[1, 2, 3, 4]	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.34	UI
J_{RX_RJ}[1, 2, 3, 4]	Random jitter tolerance (peak-to-peak)	—	—	—	0.26	UI
J_{RX_SJ}[1, 2, 3, 4]	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.11	UI
J_{RX_TJ}[1, 2, 3, 4]	Total jitter tolerance (peak-to-peak)	—	—	—	0.71	UI
T_{RX_EYE}	Receiver eye opening	—	0.29	—	—	UI

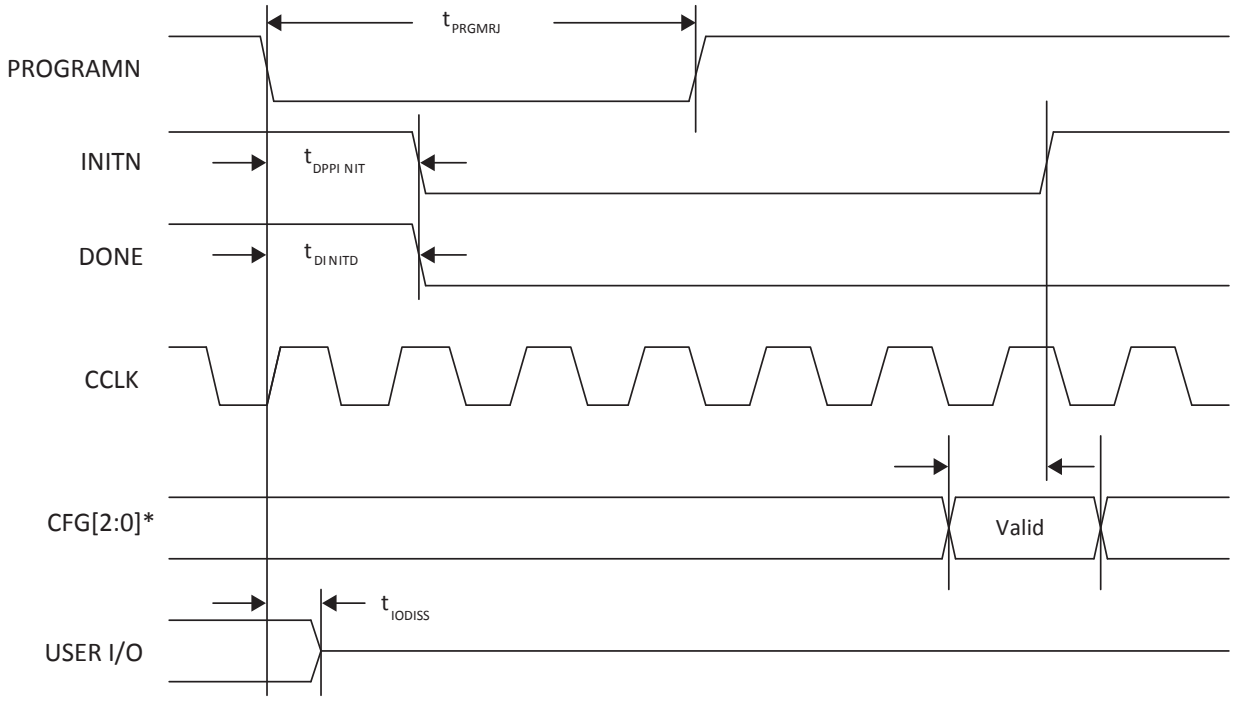
Notes:
1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.31. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications

Symbol	Parameter		Min	Max	Unit
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC}, V_{CCAUX} or V_{CCIO8} (whichever is the last) to the rising edge of INITN	—	—	33	ms
t_{VMC}	Time from t_{ICFG} to the valid Master CCLK	—	—	5	us
t_{CZ}	CCLK from Active to High-Z	—	—	300	ns
Master CCLK					
f_{MCLK}	Frequency	All selected frequencies	–20	20	%
$t_{MCLK-DC}$	Duty Cycle	All selected frequencies	40	60	%
All Configuration Modes					
t_{PRGM}	PROGRAMN LOW pulse accepted	—	110	—	ns
t_{PRGMRJ}	PROGRAMN LOW pulse rejected	—	—	50	ns
t_{INITL}	INITN LOW time	—	—	55	ns
t_{DPPINT}	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	150	ns
Slave SPI					
f_{CCLK}	CCLK input clock frequency	—	—	60	MHz
t_{CCLKH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{CCLKL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{STSU}	CCLK setup time	—	1	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{STCO}	CCLK falling edge to valid output	—	—	10	ns
t_{STOZ}	CCLK falling edge to valid disable	—	—	10	ns
t_{STOV}	CCLK falling edge to valid enable	—	—	10	ns
t_{SCS}	Chip Select HIGH time	—	25	—	ns
t_{SCSS}	Chip Select setup time	—	3	—	ns
t_{SCSH}	Chip Select hold time	—	3	—	ns
Master SPI					
f_{CCLK}	Max selected CCLK output frequency	—	—	62	MHz
t_{CCLKH}	CCLK output clock pulse width HIGH	—	3.5	—	ns
t_{CCLKL}	CCLK output clock pulse width LOW	—	3.5	—	ns
t_{STSU}	CCLK setup time	—	5	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{CSSPI}	INITN HIGH to Chip Select LOW	—	100	200	ns
t_{CFGX}	INITN HIGH to first CCLK edge	—	—	150	ns
Slave Serial					
f_{CCLK}	CCLK input clock frequency	—	—	66	MHz
t_{SSCH}	CCLK input clock pulse width HIGH	—	5	—	ns
t_{SSCL}	CCLK input clock pulse width LOW	—	5	—	ns
t_{SUSCDI}	CCLK setup time	—	0.5	—	ns
t_{HSCDI}	CCLK hold time	—	1.5	—	ns



*The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

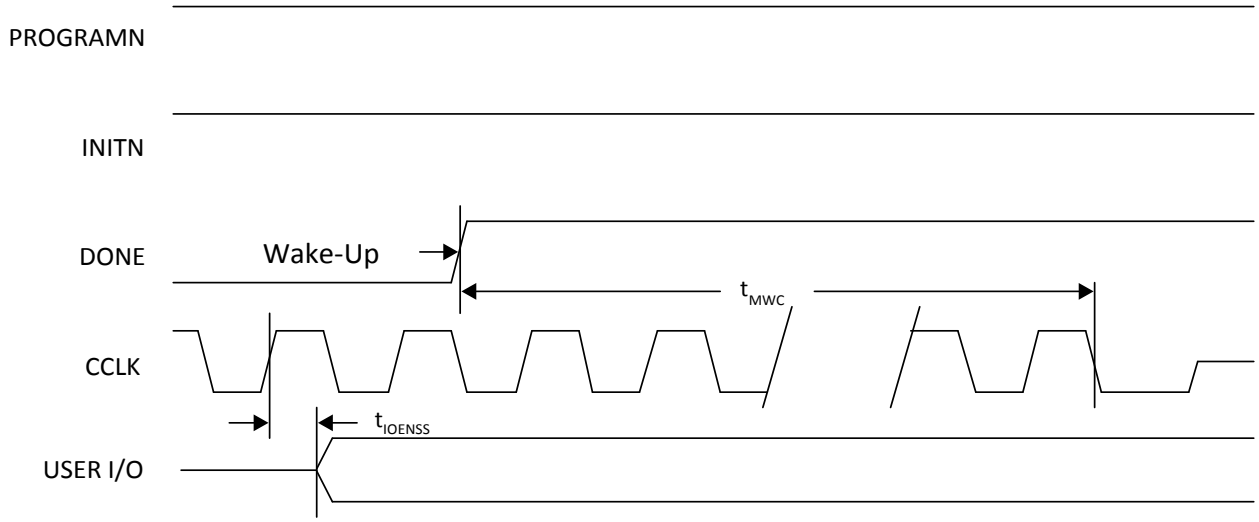


Figure 3.21. Wake-Up Timing

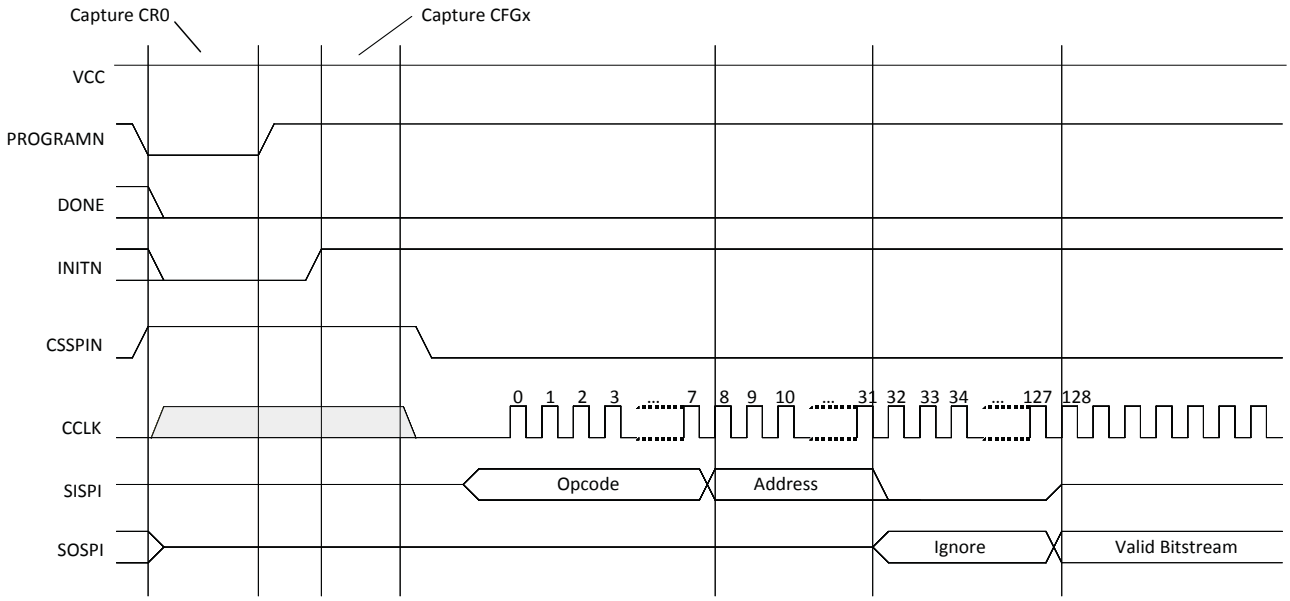


Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

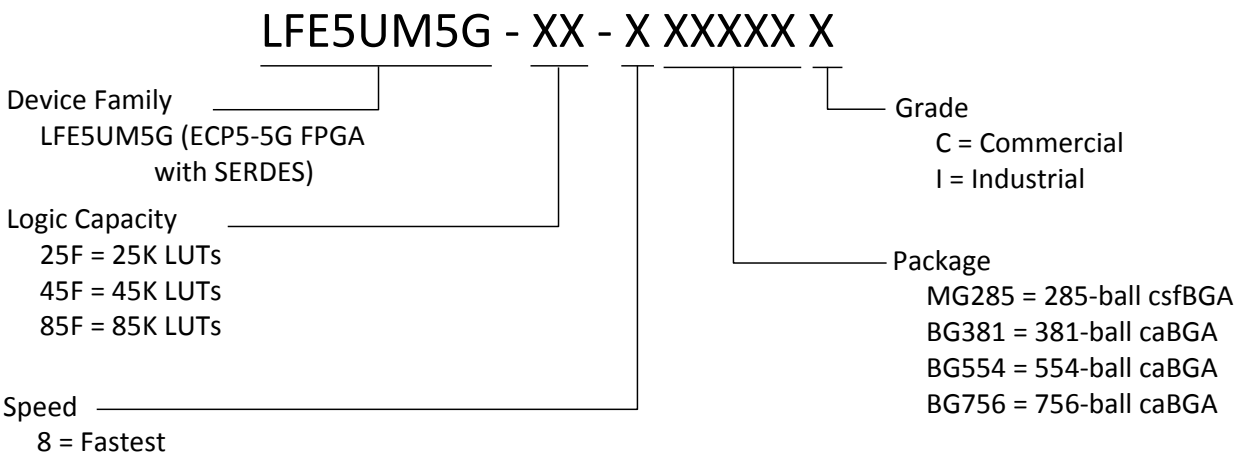
Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) *(Continued)*		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin
SERDES Function		
VCCAx	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCAx = 1.1 V for ECP5, VCCAx = 1.2 V for ECP5-5G.
VCCAUXAx	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUXAx = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.



5.2. Ordering Part Numbers

5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	–6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	–7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	–8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	–6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	–7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	–8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	–6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	–7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	–8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	–6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	–7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	–8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	–6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	–7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	–8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	–6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	–7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	–8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	–6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	–7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	–8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	–6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	–7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	–8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	–6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	–7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	–8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	–6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	–7	Lead free caBGA	554	Commercial	44	No

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.