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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

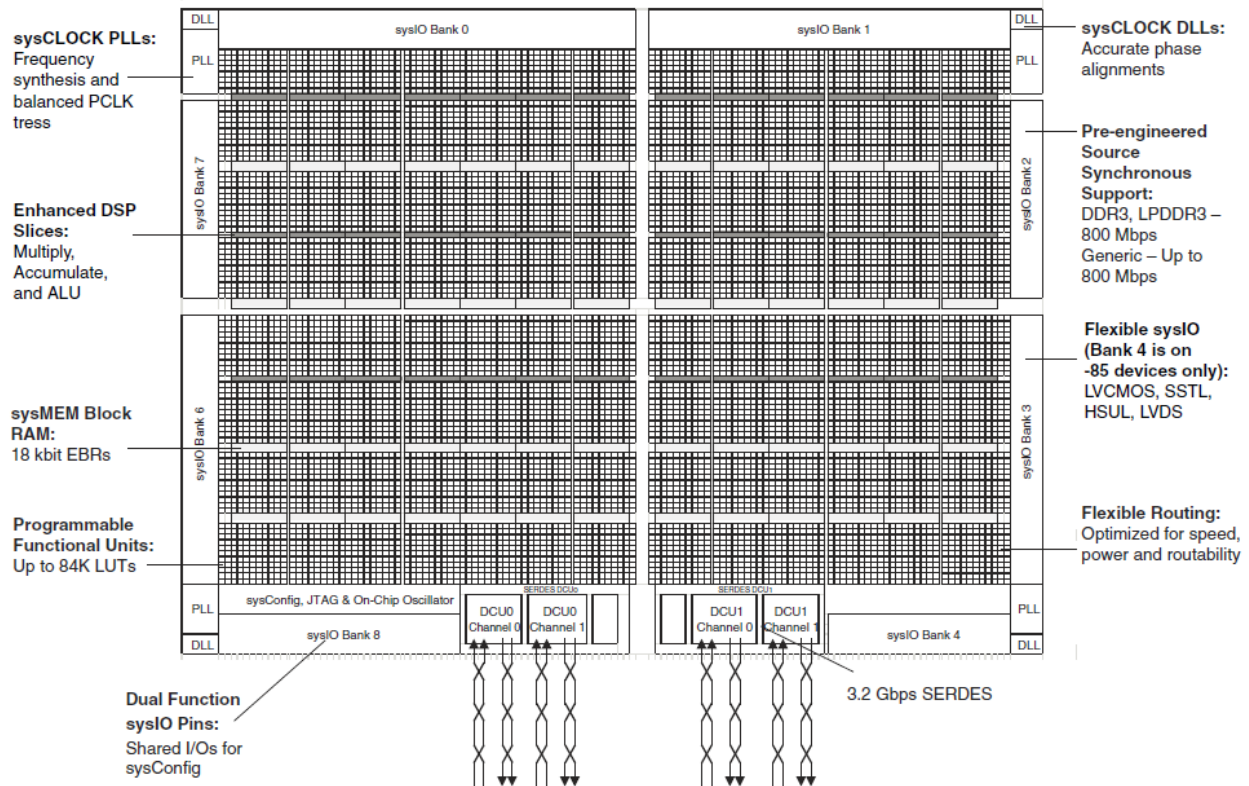
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	205
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-6bg381c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-6bg381c</a>

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Note: There is no Bank 4 in -25 and -45 devices.  
There are no PLL and DLL on the top corners in -25 devices.

**Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level)**

## 2.2. PFU Blocks

The core of the ECP5/ECP5-5G device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3, as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in either mode.

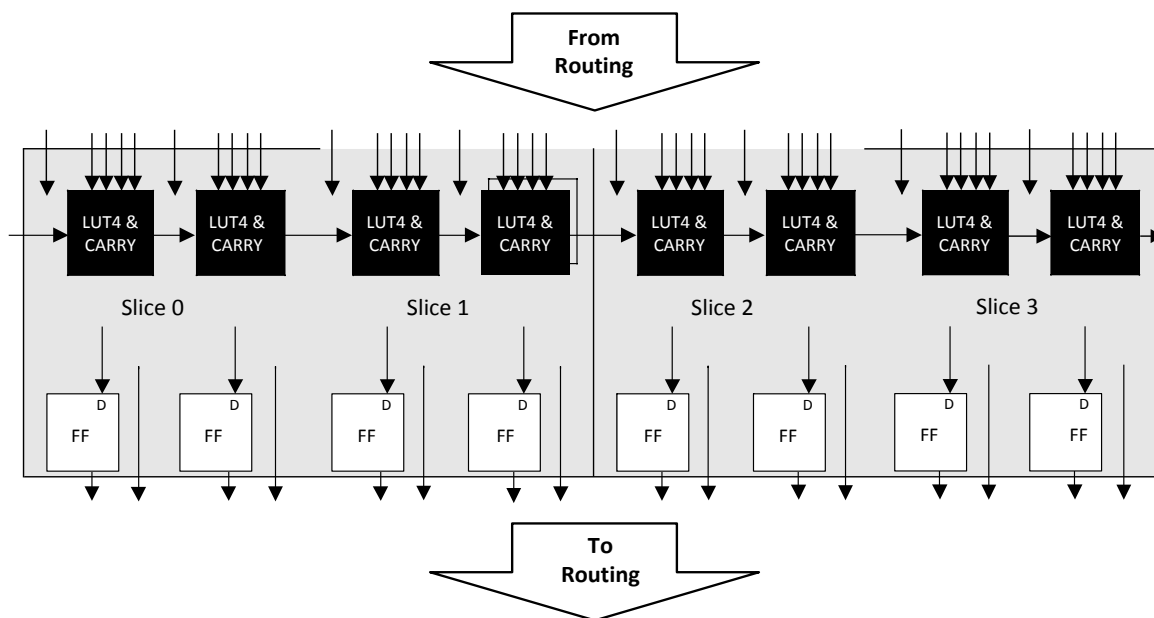


Figure 2.2. PFU Diagram

### 2.2.1. Slice

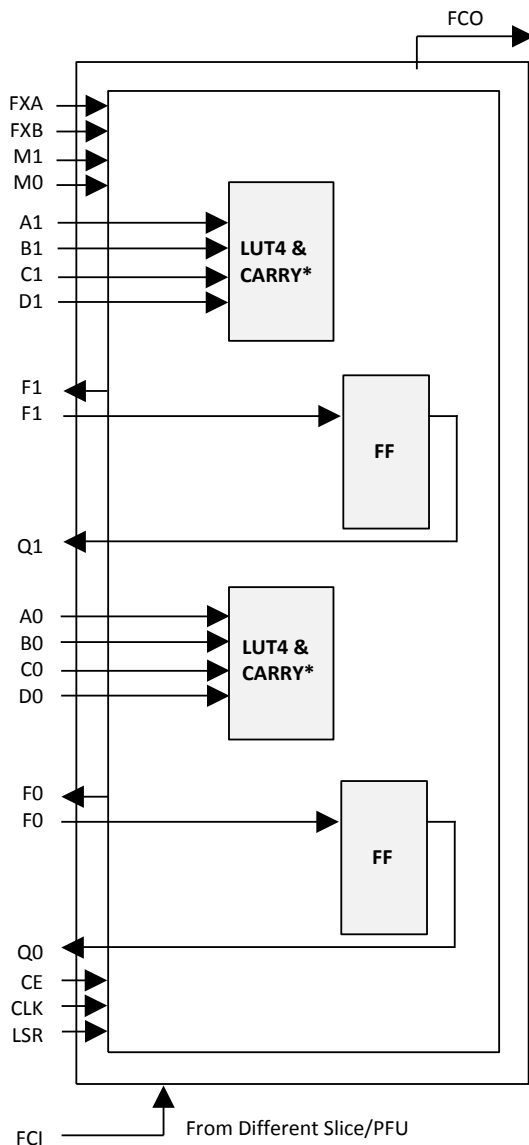
Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals, 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are five outputs, four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/ PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7 and LUT8. Table 2.2 and Figure 2.3 list the signals associated with all the slices. Figure 2.4 on page 16 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7 and LUT8.



**Notes:** For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

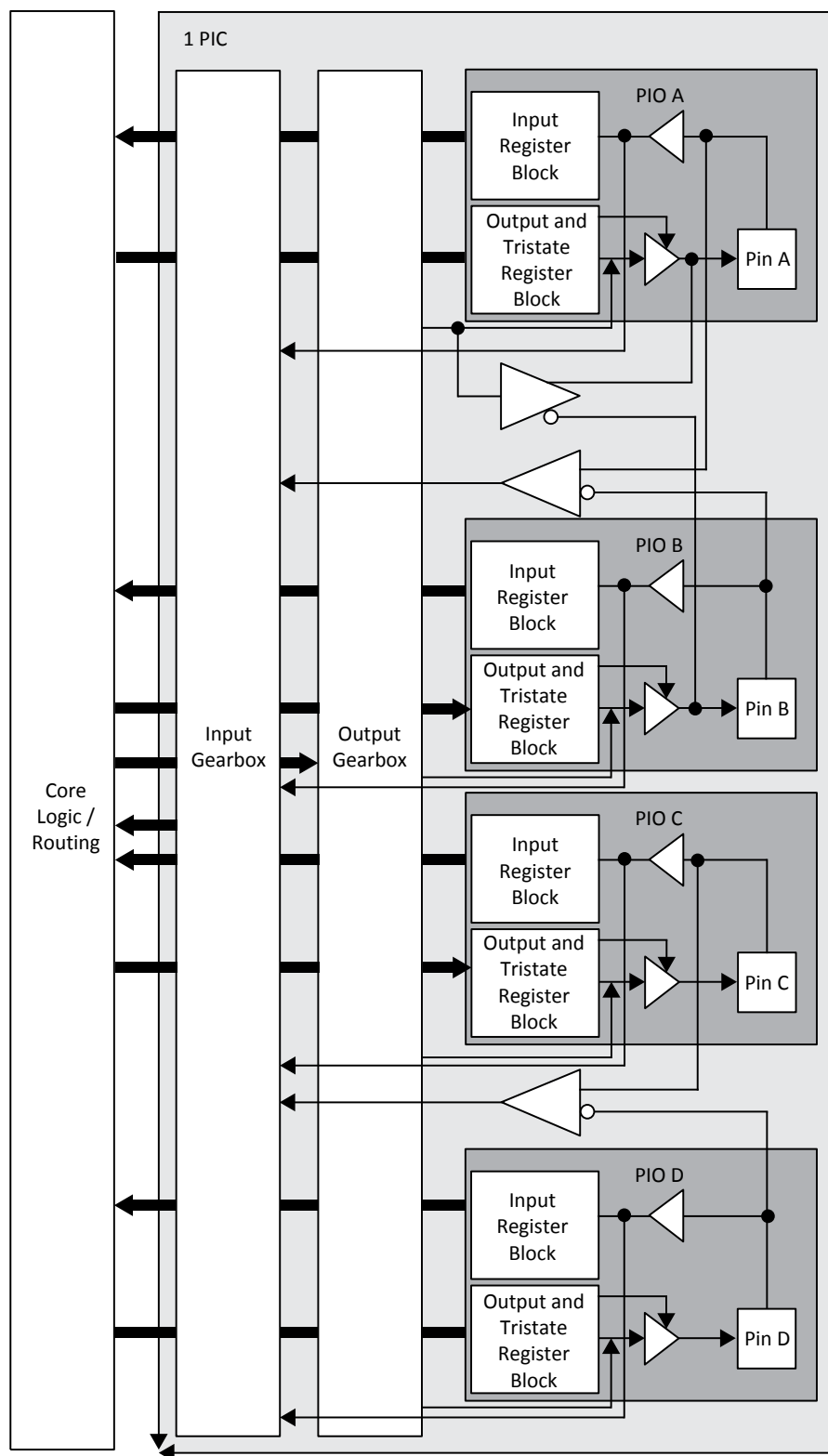
WCK is CLK

WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2

WAD [A:D] is a 4-bit address from slice 2 LUT input

**Figure 2.3. Slice Diagram**



**Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Sides**

### 2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. [Table 2.15](#) lists the allowable combination of primary and secondary protocol combinations.

## 2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

[Table 2.15](#) lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

**Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support**

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

## 2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#).

## 2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) – Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

### 2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

#### TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to [Minimizing System Interruption During Configuration Using TransFR Technology \(TN1087\)](#) for details.

#### Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#).

### 2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.



## 3. DC and Switching Characteristics

### 3.1. Absolute Maximum Ratings

**Table 3.1. Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	−0.5	1.32	V
V <sub>CCA</sub>	Supply Voltage	−0.5	1.32	V
V <sub>CCAUX</sub> , V <sub>CCAUXA</sub>	Supply Voltage	−0.5	2.75	V
V <sub>CCIO</sub>	Supply Voltage	−0.5	3.63	V
—	Input or I/O Transient Voltage Applied	−0.5	3.63	V
V <sub>CCHRX</sub> , V <sub>CCHTX</sub>	SERDES RX/TX Buffer Supply Voltages	−0.5	1.32	V
—	Voltage Applied on SERDES Pins	−0.5	1.80	V
T <sub>A</sub>	Storage Temperature (Ambient)	−65	150	°C
T <sub>J</sub>	Junction Temperature	—	+125	°C

**Notes:**

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

### 3.2. Recommended Operating Conditions

**Table 3.2. Recommended Operating Conditions**

Symbol	Parameter		Min	Max	Unit
V <sub>CC</sub> <sup>2</sup>	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
V <sub>CCAUX</sub> <sup>2,4</sup>	Auxiliary Supply Voltage	—	2.375	2.625	V
V <sub>CCIO</sub> <sup>2,3</sup>	I/O Driver Supply Voltage	—	1.14	3.465	V
V <sub>REF</sub> <sup>1</sup>	Input Reference Voltage	—	0.5	1.0	V
t <sub>JCOM</sub>	Junction Temperature, Commercial Operation	—	0	85	°C
t <sub>JIND</sub>	Junction Temperature, Industrial Operation	—	−40	100	°C
<b>SERDES External Power Supply<sup>5</sup></b>					
V <sub>CCA</sub>	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V <sub>CCAUXA</sub>	SERDES Auxiliary Supply Voltage	—	2.374	2.625	V
V <sub>CCHRX</sub> <sup>6</sup>	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V <sub>CCHTX</sub>	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

**Notes:**

1. For correct operation, all supplies except V<sub>REF</sub> must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in [Table 3.4](#) on page 48.
4. V<sub>CCAUX</sub> ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
5. Refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#) for information on board considerations for SERDES power supplies.
6. V<sub>CCHRX</sub> is used for Rx termination. It can be biased to V<sub>cm</sub> if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

### 3.3. Power Supply Ramp Rates

**Table 3.3. Power Supply Ramp Rates**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{RAMP}$	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

**Note:** Assumes monotonic ramp rates.

### 3.4. Power-On-Reset Voltage Levels

**Table 3.4. Power-On-Reset Voltage Levels**

Symbol	Parameter			Min	Typ	Max	Unit
$V_{PORUP}$	All Devices	Power-On-Reset ramp-up trip point (Monitoring $V_{CC}$ , $V_{CCAUX}$ , and $V_{CCIO8}$ )	$V_{CC}$	0.90	—	1.00	V
			$V_{CCAUX}$	2.00	—	2.20	V
			$V_{CCIO8}$	0.95	—	1.06	V
$V_{PORDN}$	All Devices	Power-On-Reset ramp-down trip point (Monitoring $V_{CC}$ , and $V_{CCAUX}$ )	$V_{CC}$	0.77	—	0.87	V
			$V_{CCAUX}$	1.80	—	2.00	V

**Notes:**

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only  $V_{CCIO8}$  has a Power-On-Reset ramp up trip point. All other  $V_{CCIOs}$  do not have Power-On-Reset ramp up detection.
- $V_{CCIO8}$  does not have a Power-On-Reset ramp down detection.  $V_{CCIO8}$  must remain within the Recommended Operating Conditions to ensure proper operation.

### 3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5/ECP5-5G device in a reset state. POR is released when  $V_{CC}$ ,  $V_{CCAUX}$ , and  $V_{CCIO8}$  are ramped above the  $V_{PORUP}$  voltage, as specified above.

$V_{CCIO8}$  controls the voltage on the configuration I/O pins. If the ECP5/ECP5-5G device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp  $V_{CCIO8}$  above  $V_{IH}$  of the external SPI Flash, before at least one of the other two supplies ( $V_{CC}$  and/or  $V_{CCAUX}$ ) is ramped to  $V_{PORUP}$  voltage level. If the system cannot meet this power up sequence requirement, and requires the  $V_{CCIO8}$  to be ramped last, then the system must keep either PROGRAMN or INITN pin LOW during power up, until  $V_{CCIO8}$  reaches  $V_{IH}$  of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meet the  $V_{IH}$  voltage requirement of the SPI Flash. For LFE5UM/LFE5UM5G devices, it is required to power up  $V_{CCA}$ , before  $V_{CCAUXA}$  is powered up.

### 3.6. Hot Socketing Specifications

**Table 3.5. Hot Socketing Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \leq V_{IN} \leq V_{IH} \text{ (Max)}$	—	—	$\pm 1$	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \leq V_{IN} < V_{CCIO}$	—	—	$\pm 1$	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5 \text{ V}$	—	18	—	mA

**Notes:**

1.  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$  should rise/fall monotonically.
2.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PW}$  or  $I_{BH}$ .
3. LVCMOS and LVTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the  $I_{DK}$  current can exceed  $\pm 1$  mA.

### 3.12. sysI/O Recommended Operating Conditions

**Table 3.11. sysI/O Recommended Operating Conditions**

Standard	V <sub>CCIO</sub>			V <sub>REF</sub> (V)		
	Min	Typ	Max	Min	Typ	Max
LVC MOS33 <sup>1</sup>	3.135	3.3	3.465	—	—	—
LVC MOS33D <sup>3</sup> Output	3.135	3.3	3.465	—	—	—
LVC MOS25 <sup>1</sup>	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 <sup>1</sup>	1.14	1.2	1.26	—	—	—
LVTTL33 <sup>1</sup>	3.135	3.3	3.465	—	—	—
SSTL15_I, _II <sup>2</sup>	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II <sup>2</sup>	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II <sup>2</sup>	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12 <sup>2</sup>	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input <sup>3, 5</sup>	1.425	1.5	1.575	—	—	—
LVDS25 <sup>1, 3</sup> Output	2.375	2.5	2.625	—	—	—
subLVDS <sup>3</sup> (Input only)	—	—	—	—	—	—
SLVS <sup>3</sup> (Input only)	—	—	—	—	—	—
LVDS25E <sup>3</sup> Output	2.375	2.5	2.625	—	—	—
MLVDS <sup>3</sup> Output	2.375	2.5	2.625	—	—	—
LVPECL33 <sup>1, 3</sup> Output	3.135	3.3	3.465	—	—	—
BLVDS25 <sup>1, 3</sup> Output	2.375	2.5	2.625	—	—	—
HSULD12D <sup>2, 3</sup>	1.14	1.2	1.26	—	—	—
SSTL135D_I, II <sup>2, 3</sup>	1.28	1.35	1.42	—	—	—
SSTL15D_I, II <sup>2, 3</sup>	1.43	1.5	1.57	—	—	—
SSTL18D_I <sup>1, 2, 3</sup> , II <sup>1, 2, 3</sup>	1.71	1.8	1.89	—	—	—

**Notes:**

1. For input voltage compatibility, refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#).
2. V<sub>REF</sub> is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V<sub>CCAUX</sub> power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V<sub>IH</sub> and V<sub>IL</sub>. It can also be implemented as LVC MOS12 with VCCIO at 1.2V, which would meet V<sub>IH</sub>/V<sub>IL</sub> spec on LVCOM12.

### 3.14.7. MLVDS25

The ECP5/ECP5-5G devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.

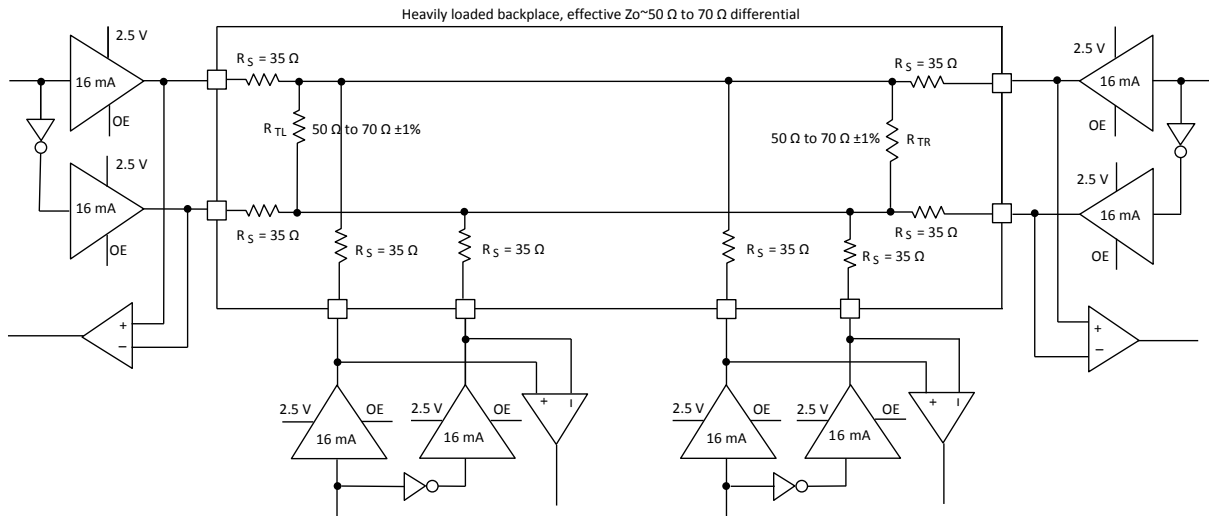


Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Table 3.17. MLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo=50 Ω	Zo=70 Ω	
V <sub>CCIO</sub>	Output Driver Supply (±5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
R <sub>S</sub>	Driver Series Resistor (±1%)	35.00	35.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
R <sub>TR</sub>	Receiver Termination (±1%)	50.00	70.00	Ω
V <sub>OH</sub>	Output High Voltage	1.52	1.60	V
V <sub>OL</sub>	Output Low Voltage	0.98	0.90	V
V <sub>OD</sub>	Output Differential Voltage	0.54	0.70	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	21.74	20.00	mA

**Note:** For input buffer, see LVDS Table 3.13 on page 55.

### 3.17. Maximum I/O Buffer Speed

Over recommended operating conditions.

**Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed**

Buffer	Description	Max	Unit
<b>Maximum Input Frequency</b>			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MIPI D-PHY (HS Mode)	MIPI Video	400	MHz
SLVS	SLVS similar to MIPI	400	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, $V_{CCIO} = 1.5\text{ V}$	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, $V_{CCIO} = 1.35\text{ V}$	400	MHz
HSUL12 (all supported classes)	HSUL_12 class I, II, $V_{CCIO} = 1.2\text{ V}$	400	MHz
LVTTL33	LVTTL, $V_{CCIO} = 3.3\text{ V}$	200	MHz
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	200	MHz
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	200	MHz
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	200	MHz
LVC MOS15	LVC MOS 1.5, $V_{CCIO} = 1.5\text{ V}$	200	MHz
LVC MOS12	LVC MOS 1.2, $V_{CCIO} = 1.2\text{ V}$	200	MHz
<b>Maximum Output Frequency</b>			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	150	MHz
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	150	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	150	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	150	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, $V_{CCIO} = 1.5\text{ V}$	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, $V_{CCIO} = 1.35\text{ V}$	400	MHz
HSUL12 (all supported classes)	HSUL12 class I, II, $V_{CCIO} = 1.2\text{ V}$	400	MHz
LVTTL33	LVTTL, $V_{CCIO} = 3.3\text{ V}$	150	MHz
LVC MOS33 (For all drives)	LVC MOS, 3.3 V	150	MHz
LVC MOS25 (For all drives)	LVC MOS, 2.5 V	150	MHz
LVC MOS18 (For all drives)	LVC MOS, 1.8 V	150	MHz
LVC MOS15 (For all drives)	LVC MOS, 1.5 V	150	MHz
LVC MOS12 (For all drives)	LVC MOS, 1.2 V	150	MHz

**Notes:**

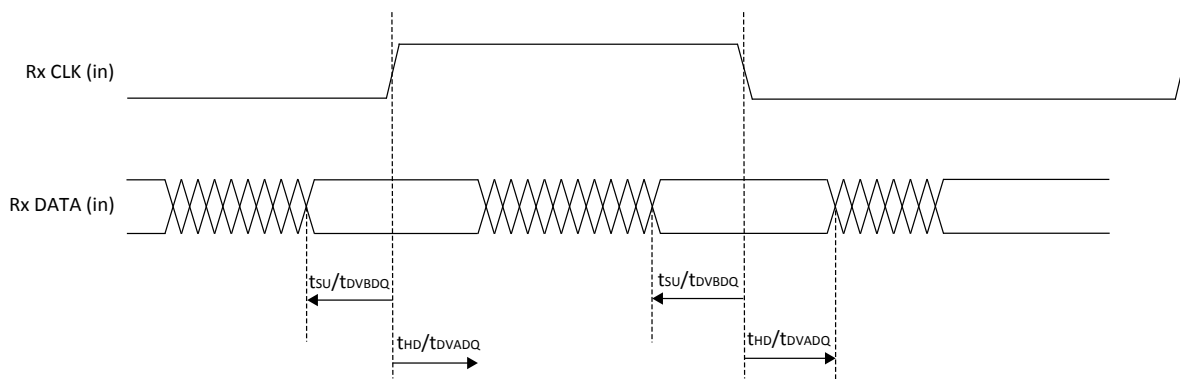
1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVC MOS timing is measured with the load specified in Switching Test Conditions, Table 3.44 on page 90.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

### 3.18. External Switching Characteristics

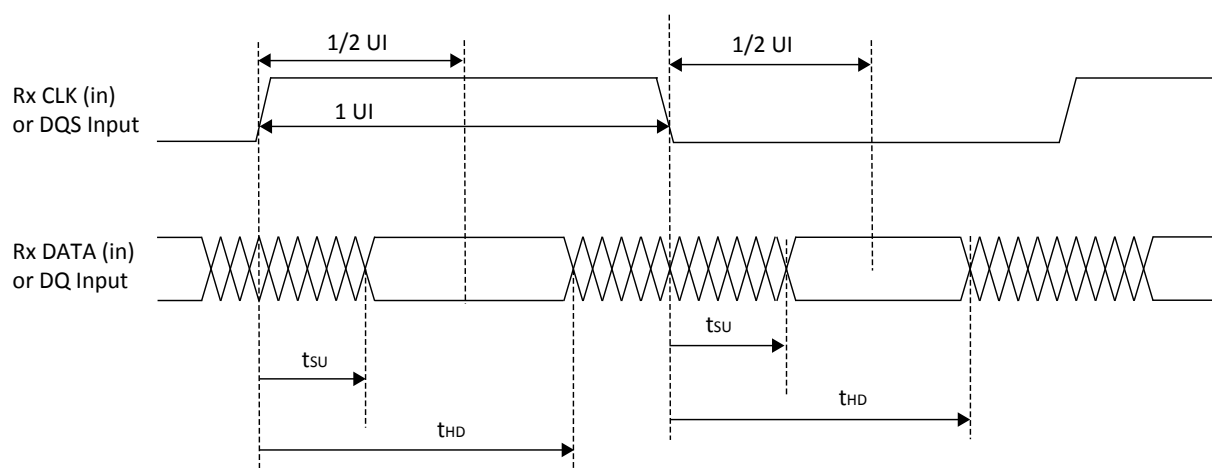
Over recommended commercial operating conditions.

**Table 3.22. ECP5/ECP5-5G External Switching Characteristics**

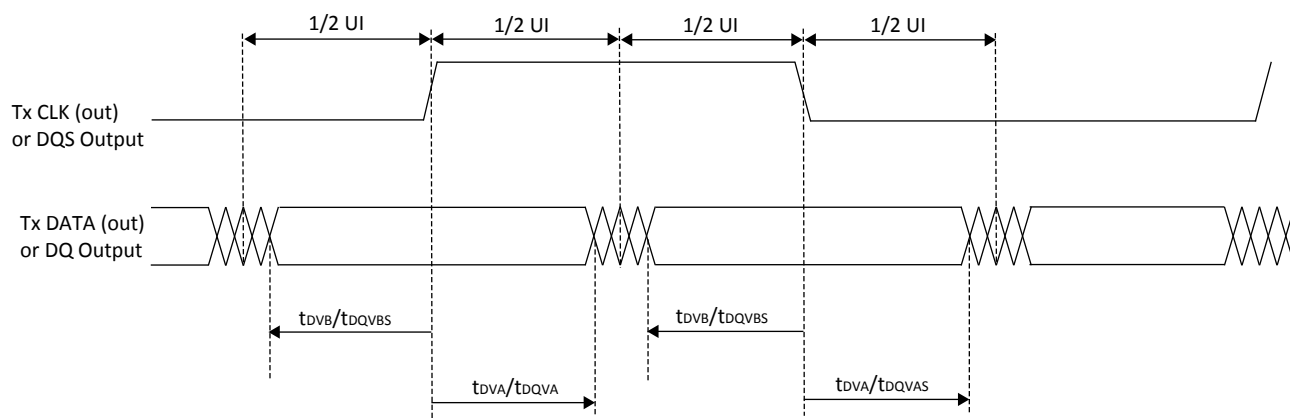
Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks									
Primary Clock									
f <sub>MAX_PRI</sub>	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
t <sub>SKEW_PRI</sub>	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
Edge Clock									
f <sub>MAX_EDGE</sub>	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
t <sub>W_EDGE</sub>	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
t <sub>SKEW_EDGE</sub>	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
Generic SDR Input									
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL									
t <sub>CO</sub>	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
t <sub>SU</sub>	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
t <sub>SU_DEL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
t <sub>H_DEL</sub>	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL									
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
t <sub>SU_DEPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns



**Figure 3.6. Receiver RX.CLK.Centered Waveforms**



**Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms**



**Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms**

## 3.24. SERDES External Reference Clock

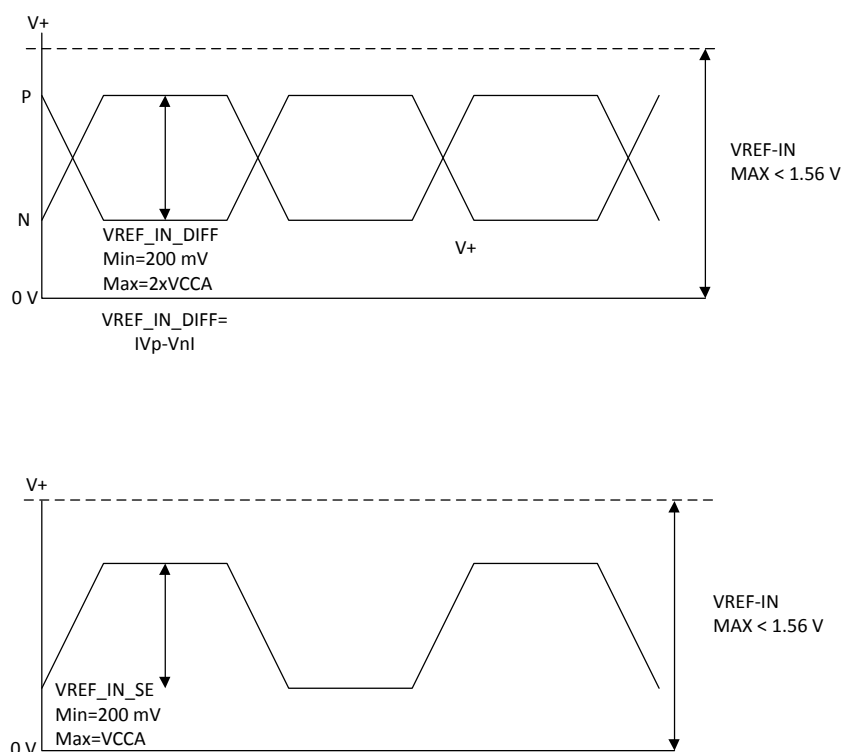
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3.29 specifies reference clock requirements, over the full range of operating conditions.

**Table 3.29. External Reference Clock Specification (refclkp/refclkn)**

Symbol	Description	Min	Typ	Max	Unit
$F_{REF}$	Frequency range	50	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance <sup>1</sup>	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock <sup>2,4</sup>	200	—	$V_{CCAUXA}$	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2 \cdot V_{CCAUXA}$	mV, p-p differential
$V_{REF-IN}$	Input levels	0	—	$V_{CCAUXA} + 0.4$	V
$D_{REF}$	Duty cycle <sup>3</sup>	40	—	60	%
$T_{REF-R}$	Rise time (20% to 80%)	200	500	1000	ps
$T_{REF-F}$	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–30%	100/HiZ	+30%	$\Omega$
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

**Notes:**

- Depending on the application, the PLL\_LOL\_SET and CDR\_LOL\_SET control registers may be adjusted for other tolerance values as described in [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).
- The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
- Measured at 50% amplitude.
- Single-ended clocking is achieved by applying a reference voltage  $V_{REF}$  on REFCLKN input, with the clock applied to REFCLKP input pin.  $V_{REF}$  should be set to mid-point of the REFCLKP voltage swing.



**Figure 3.14. SERDES External Reference Clock Waveforms**



### 3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

**Table 3.31. PCIe (5 Gb/s)**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
<b>Transmit<sup>1</sup></b>						
UI	Unit Interval	—	199.94	200	200.06	ps
B <sub>WTX-PKG-PLL2</sub>	Tx PLL bandwidth corresponding to PKGTx-PLL2	—	5	—	16	MHz
P <sub>KGTx-PLL2</sub>	Tx PLL Peaking	—	—	—	1	dB
V <sub>TX-DIFF-PP</sub>	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
V <sub>TX-DIFF-PP-LOW</sub>	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
V <sub>TX-DE-RATIO-3.5dB</sub>	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
V <sub>TX-DE-RATIO-6dB</sub>	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
T <sub>MIN-PULSE</sub>	Instantaneous lone pulse width	—	—	—	—	UI
T <sub>TX-RISE-FALL</sub>	Transmitter rise and fall time	—	—	—	—	UI
T <sub>TX-EYE</sub>	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T <sub>TX-DJ</sub>	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T <sub>TX-RJ</sub>	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
T <sub>RF-MISMATCH</sub>	Tx rise/fall time mismatch	—	—	—	—	UI
R <sub>LTX-DIFF</sub>	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R <sub>LTX-CM</sub>	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
Z <sub>TX-DIFF-DC</sub>	DC differential Impedance	—	—	—	120	Ω
V <sub>TX-CM-AC-PP</sub>	Tx AC peak common mode voltage, peak-peak	—	—	—	—	mV, p-p
I <sub>TX-SHORT</sub>	Transmitter short-circuit current	—	—	—	90	mA
V <sub>TX-DC-CM</sub>	Transmitter DC common-mode voltage	—	0	—	1.2	V
V <sub>TX-IDLE-DIFF-DC</sub>	Electrical Idle Output DC voltage	—	0	—	5	mV
V <sub>TX-IDLE-DIFF-AC-p</sub>	Electrical Idle Differential Output peak voltage	—	—	—	—	mV
V <sub>TX-RCV-DETECT</sub>	Voltage change allowed during Receiver Detect	—	—	—	600	mV
T <sub>TX-IDLE-MIN</sub>	Min. time in Electrical Idle	—	20	—	—	ns
T <sub>TX-IDLE-SET-TO-IDLE</sub>	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
T <sub>TX-IDLE-TO-DIFF-DATA</sub>	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
L <sub>TX-SKEW</sub>	Lane-to-lane output skew	—	—	—	—	ps

## 3.27. XAUI/CPRI LV E.30 Electrical and Timing Characteristics

### 3.27.1. AC and DC Characteristics

Over recommended operating conditions.

**Table 3.33. Transmit**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T <sub>RF</sub>	Differential rise/fall time	20% to 80%	—	80	—	ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance	—	80	100	120	Ω
J <sub>TX_DDJ</sub> <sup>2,3</sup>	Output data deterministic jitter	—	—	—	0.17	UI
J <sub>TX_TJ</sub> <sup>1, 2, 3</sup>	Total output data jitter	—	—	—	0.35	UI

**Notes:**

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Over recommended operating conditions.

**Table 3.34. Receive and Jitter Tolerance**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z <sub>RX_DIFF</sub>	Differential termination resistance	—	80	100	120	Ω
J <sub>RX_DJ</sub> <sup>1, 2, 3</sup>	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J <sub>RX_RJ</sub> <sup>1, 2, 3</sup>	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J <sub>RX_SJ</sub> <sup>1, 2, 3</sup>	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3</sup>	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T <sub>RX_EYE</sub>	Receiver eye opening	—	0.35	—	—	UI

**Notes:**

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

## 3.28. CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics

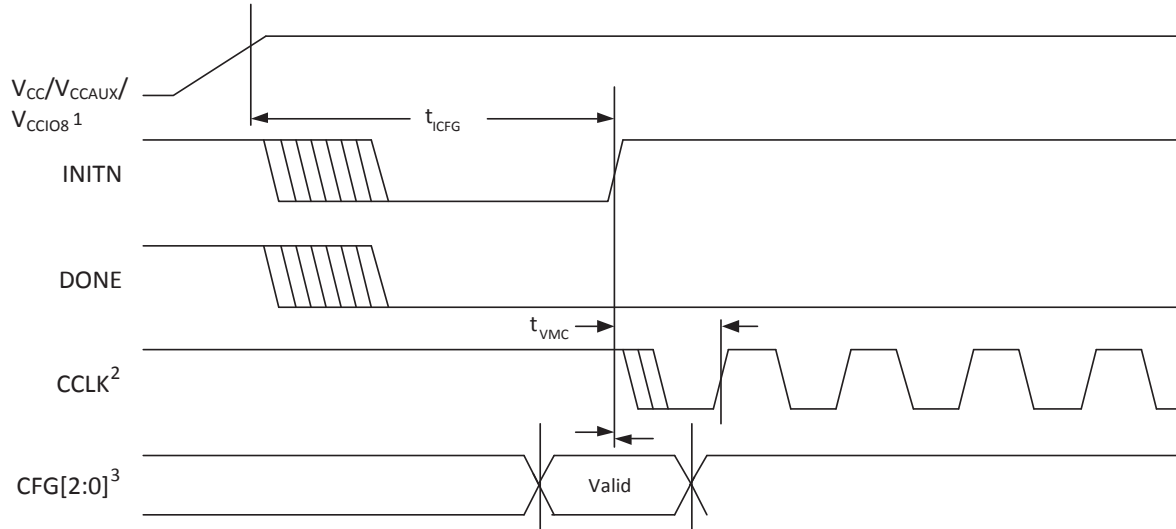
### 3.28.1. AC and DC Characteristics

**Table 3.35. Transmit**

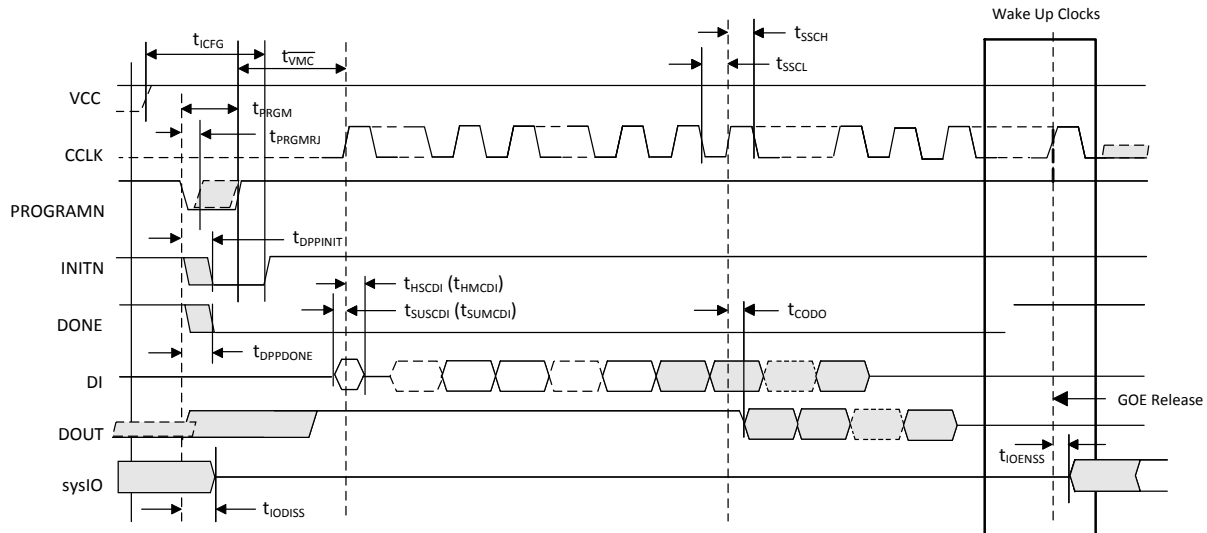
Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T <sub>RF</sub> <sup>1</sup>	Differential rise/fall time	20% to 80%	—	80	—	ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance	—	80	100	120	Ω
J <sub>TX_DDJ</sub> <sup>3,4</sup>	Output data deterministic jitter	—	—	—	0.17	UI
J <sub>TX_TJ</sub> <sup>2, 3, 4</sup>	Total output data jitter	—	—	—	0.35	UI

**Notes:**

1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.



**Figure 3.18. Power-On-Reset (POR) Timing**



**Figure 3.19. sysCONFIG Port Timing**

Signal Name	I/O	Description
<b>Configuration Pads (Used during sysCONFIG) (Continued)</b>		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
<b>SERDES Function</b>		
VCCA <sub>x</sub>	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCA <sub>x</sub> = 1.1 V for ECP5, VCCA <sub>x</sub> = 1.2 V for ECP5-5G.
VCCAUX <sub>Ax</sub>	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUX <sub>Ax</sub> = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

**Notes:**

- When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
- These pins are dedicated inputs or can be used as general purpose I/O.
- m defines the associated channel in the quad.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclk).
			Modified section heading to XXAU/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.