Lattice Semiconductor Corporation - LFE5UM-85F-6BG554C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	259
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-6bg554c

2. Architecture

2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2.1 on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG™ ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.

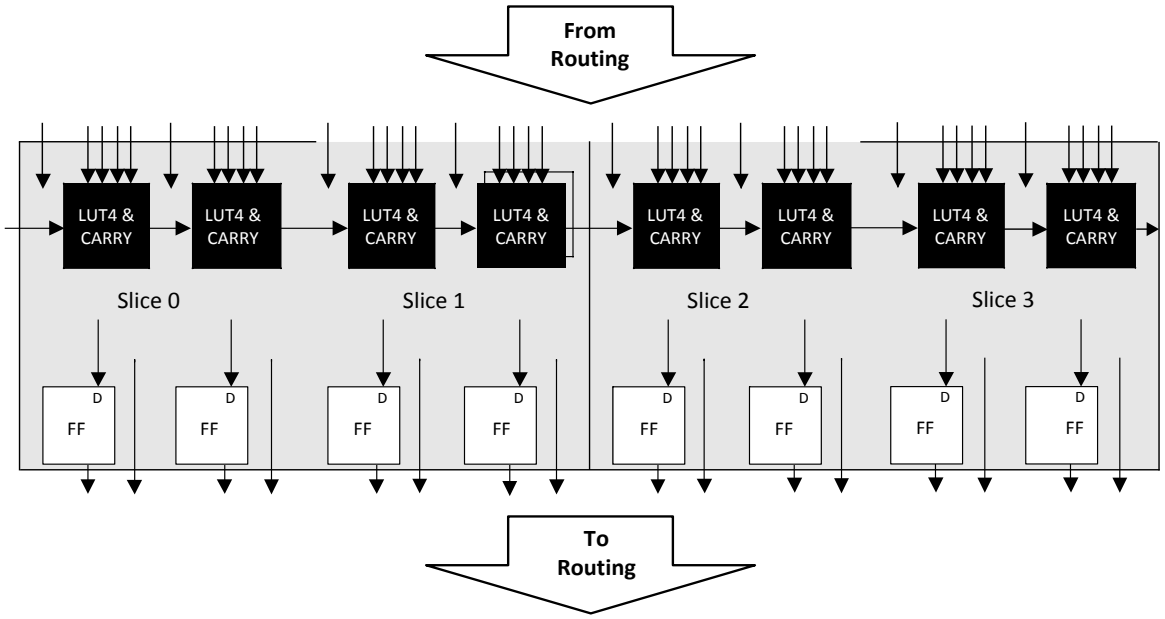


Figure 2.2. PFU Diagram

2.2.1. Slice

Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals, 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are five outputs, four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/ PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7 and LUT8. Table 2.2 and Figure 2.3 list the signals associated with all the slices. Figure 2.4 on page 16 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7 and LUT8.

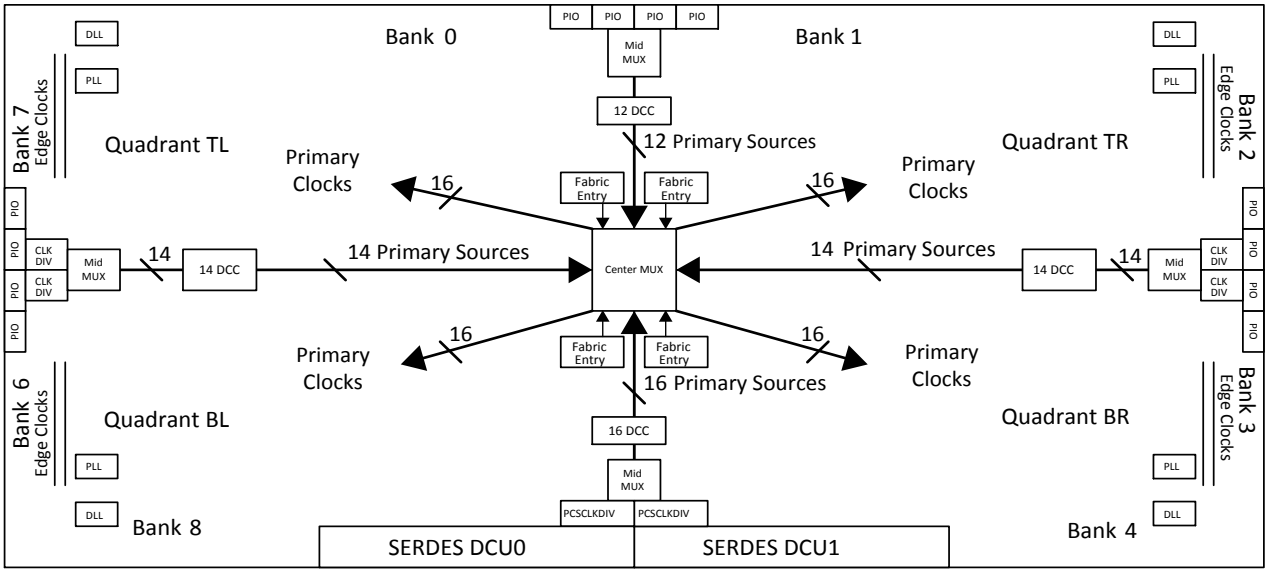


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.2. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it is not required running clocks when used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

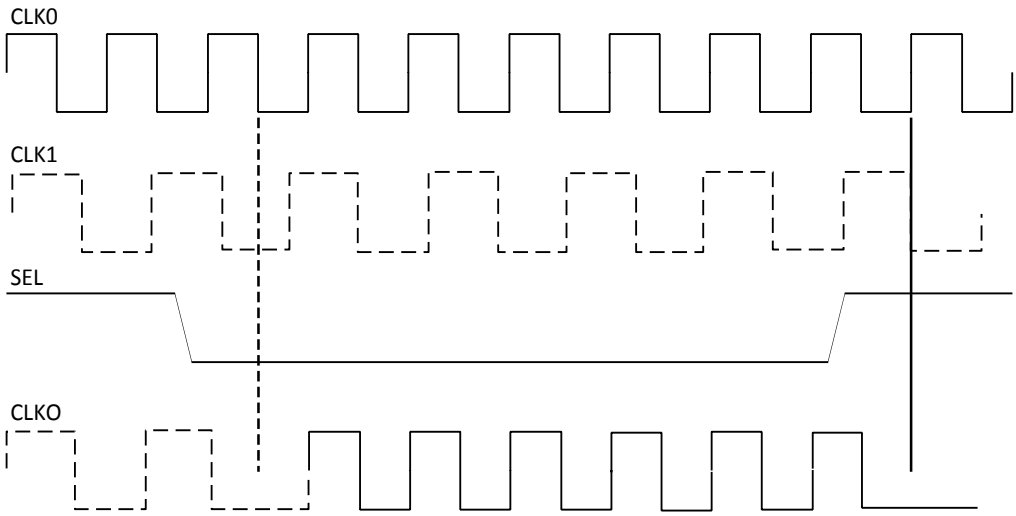


Figure 2.7. DCS Waveforms

2.5.2. Edge Clock

ECP5/ECP5-5G devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90o)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

2.8.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.8.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.8.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.8.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- **Read-Before-Write** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

2.11. PIO

The PIO contains three blocks: an input register block, output register block, and tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

2.11.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers to shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers samples the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The top side of the device supports IDDRX1 gearing function. For more information on gearing function, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

Figure 2.17 shows the input register block for the PIOs on the top edge.

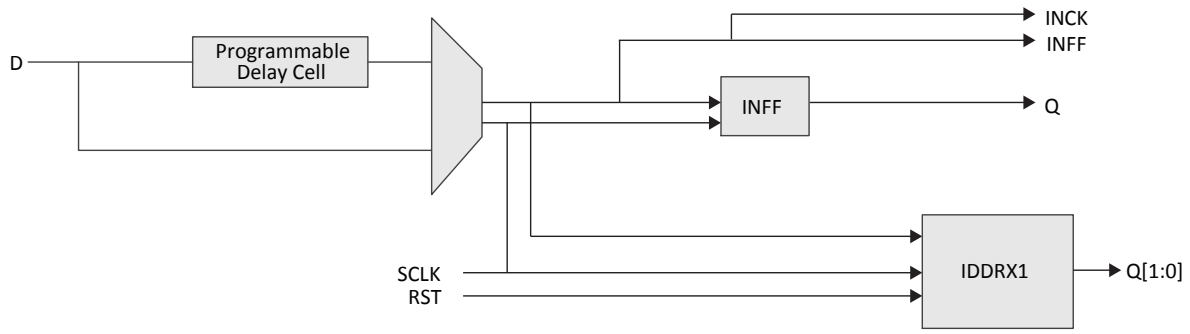
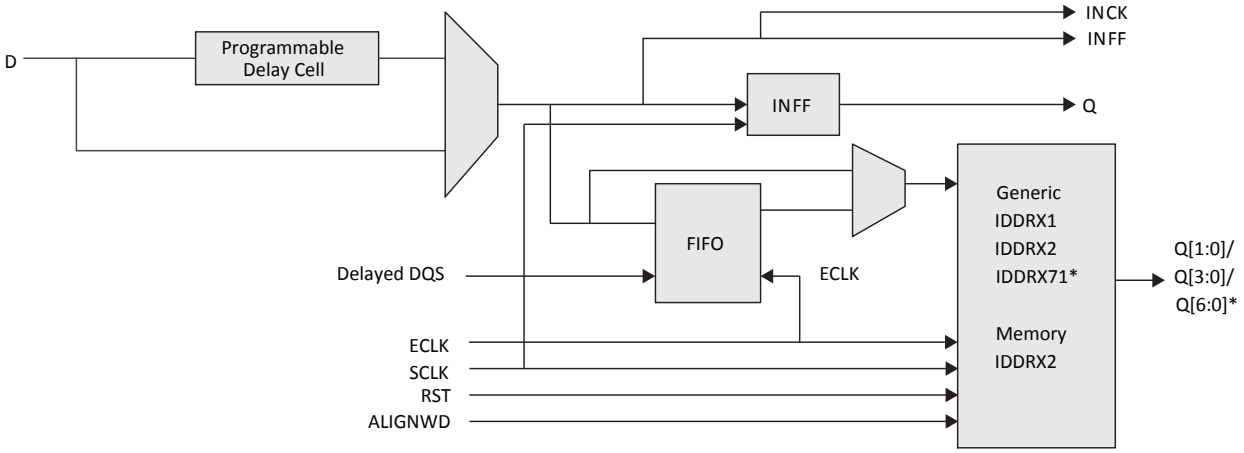


Figure 2.17. Input Register Block for PIO on Top Side of the Device

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

Figure 2.18. Input Register Block for PIO on Left and Right Side of the Device

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.11. SERDES Power Supply Requirements[1,2,3]

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I_{CCA-SB}	V_{CCA} Power Supply Current (Per Channel)	4	9.5	mA
$I_{CCHRX-SB}$[4]	V_{CCHRX}, Input Buffer Current (Per Channel)	—	0.1	mA
$I_{CCHTX-SB}$	V_{CCHTX}, Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 3.125 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	43	54	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	40	50	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	34	43	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	28	38	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For $I_{CCHRX-SB}$, during Standby, input termination on Rx are disabled.
5. For $I_{CCHRX-OP}$, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3, 5]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
Generic DDR Output									
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDRX1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{DVB\_GDDRX1\_centered}$	Data Output Valid before CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$t_{DVA\_GDDRX1\_centered}$	Data Output Valid after CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9									
$t_{DIB\_GDDRX1\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.3	—	–0.3	—	–0.3	—	ns
$t_{DIA\_GDDRX1\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.3	—	0.3	—	0.3	ns
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8									
$t_{DVB\_GDDRX2\_centered}$	Data Output Valid Before CLK Output	All Devices	–0.442	—	–0.56	—	–0.676	—	ns + 1/2 UI
$t_{DVA\_GDDRX2\_centered}$	Data Output Valid After CLK Output	All Devices	—	0.442	—	0.56	—	0.676	ns + 1/2 UI
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9									
$t_{DIB\_GDDRX2\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns
$t_{DIA\_GDDRX2\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDRX71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12									
$t_{DIB\_LVDS71\_i}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns + (i) * UI
$t_{DIA\_LVDS71\_i}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns + (i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz
Memory Interface									
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)									
t_{DVBDQ_DDR2} t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	–0.26	—	–0.317	—	–0.374	ns + 1/2 UI
t_{DVADQ_DDR2} t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.26	—	0.317	—	0.374	—	ns + 1/2 UI

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

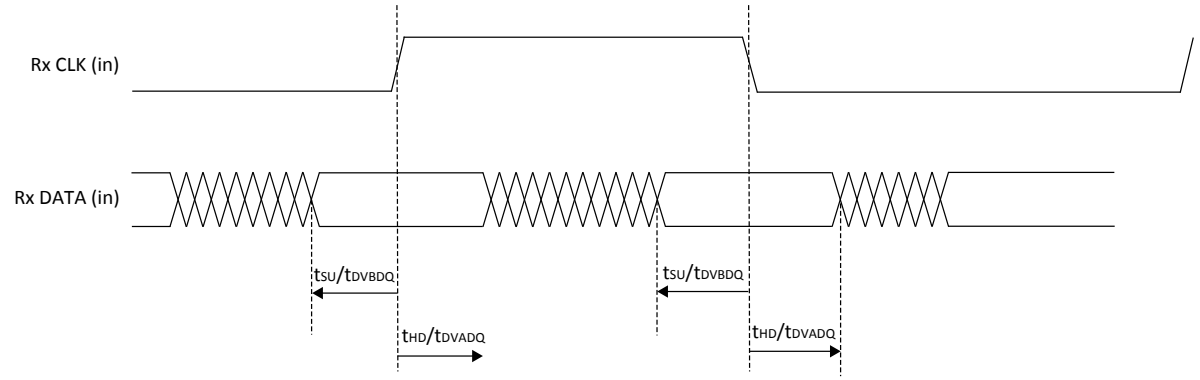


Figure 3.6. Receiver RX.CLK.Centered Waveforms

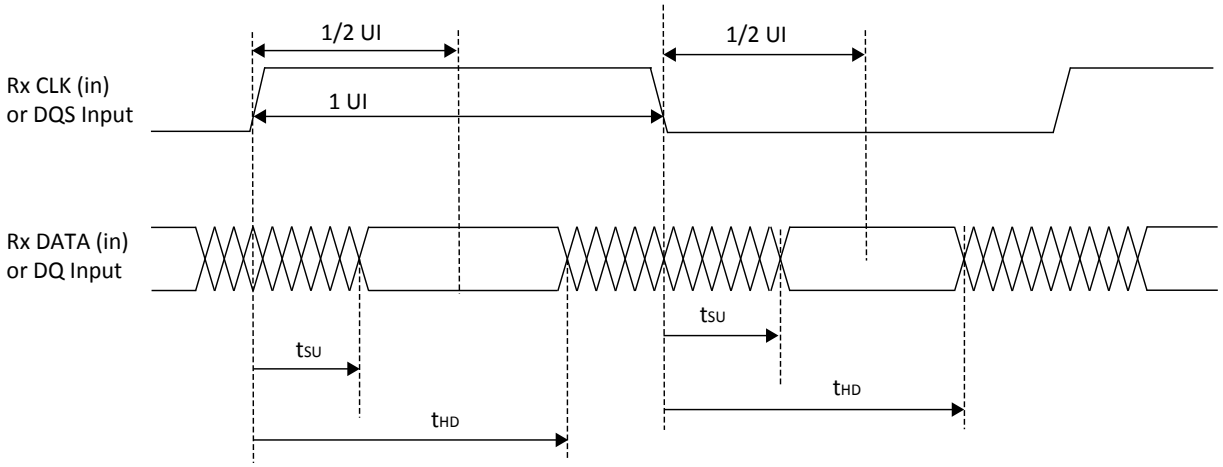


Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

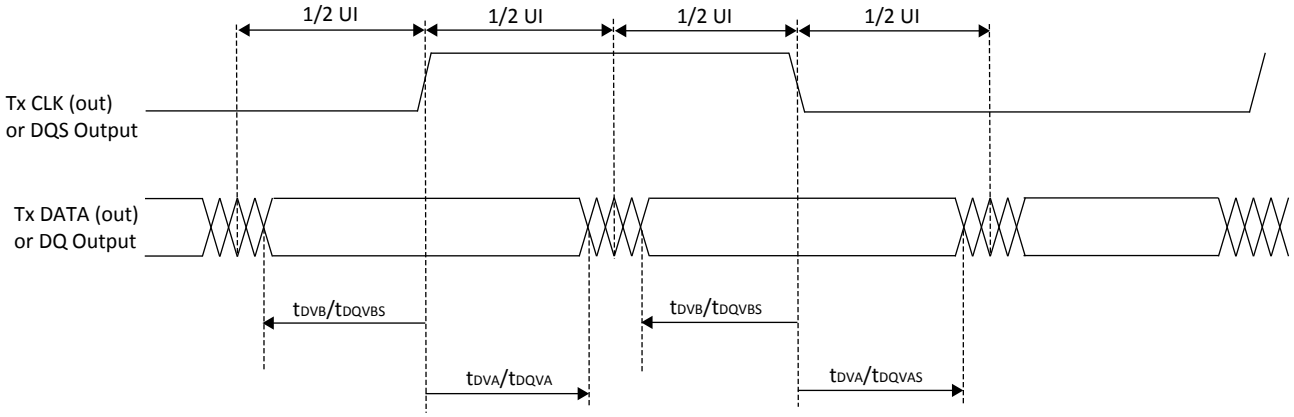


Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 3.23. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
f_{VCO}	PLL VCO Frequency	—	400	800	MHz
f_{PFD}[3]	Phase Detector Input Frequency	—	10	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_W	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
t_{LOCK}[2]	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST/ Pulse Width	—	1	—	ms
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{LOAD_REG}	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain “0” or	—	4	—	VCO cycles

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit						
UI	Unit Interval	—	203.43	203.45	203.47	ps
T_{DCD}	Duty Cycle Distortion	—	—	—	0.05	UI
J_{UBHPJ}	Uncorrelated Bounded High Probability Jitter	—	—	—	0.15	UI
J_{TOTAL}	Total Jitter	—	—	—	0.3	UI
$Z_{RX-DIFF-DC}$	DC differential Impedance	—	80	—	120	Ω
T_{SKEW}	Skew between differential signals	—	—	—	9	ps
$R_{LTX-DIFF}$	Tx Differential Return Loss (S22), including package and silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	—	—	dB
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	100	mA
$T_{RISE\_FALL-DIFF}$	Differential Rise and Fall Time	—		—	—	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—		ps
Receive						
UI	Unit Interval	—	203.43	203.45	203.47	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	—	—	1.2	V, p-p
$V_{RX-EYE\_Y1\_Y2}$	Receiver eye opening mask, Y1 and Y2	—	62.5	—	375	mV, diff
V_{RX-EYE_X1}	Receiver eye opening mask, X1	—	—	—	0.3	UI
T_{RX-TJ}	Receiver total jitter tolerance (not including sinusoidal)	—	—	—	0.6	UI
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
$Z_{RX-DIFF-DC}$	Receiver DC differential impedance	—	80	100	120	Ω

Note: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

3.27. XAUI/CPRI LV E.30 Electrical and Timing Characteristics

3.27.1. AC and DC Characteristics

Over recommended operating conditions.

Table 3.33. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	Ω
J_{TX_DDJ}[2, 3]	Output data deterministic jitter	—	—	—	0.17	UI
J_{TX_TJ}[1, 2, 3]	Total output data jitter	—	—	—	0.35	UI

Notes:
1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Over recommended operating conditions.

Table 3.34. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J_{RX_DJ}[1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J_{RX_RJ}[1, 2, 3]	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J_{RX_SJ}[1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J_{RX_TJ}[1, 2, 3]	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening	—	0.35	—	—	UI

Notes:
1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

3.28. CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics

3.28.1. AC and DC Characteristics

Table 3.35. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}[1]	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	Ω
J_{TX_DDJ}[3, 4]	Output data deterministic jitter	—	—	—	0.17	UI
J_{TX_TJ}[2, 3, 4]	Total output data jitter	—	—	—	0.35	UI

Notes:
1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.39. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDO}	Serial data rate	—	270	—	2975	Mb/s
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	270 Mb/s[6]	—	—	0.2	UI
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	1485 Mb/s	—	—	0.2	UI
$T_{JALIGNMENT}$[1, 2]	Serial output jitter, alignment	2970 Mb/s	—	—	0.3	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mb/s[6]	—	—	0.2	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mb/s	—	—	1	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mb/s	—	—	2	UI

Notes:
1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice SERDES device configured to 50 Ω output impedance connecting to the external cable driver with differential signaling.
4. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mb/s.
5. All LFE5UM/LFE5UM5G devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.
6. 270 Mb/s is supported with Rate Divider only.

Table 3.40. Receive

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDI}	Serial input data rate	—	270	—	2970	Mb/s

Table 3.41. Reference Clock

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F_{VCLK}	Video output clock frequency	—	54	—	148.5	MHz
DC_V	Duty cycle, video clock	—	45	50	55	%

Note: SD-SDI (270 Mb/s) is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

3.31. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications

Symbol	Parameter		Min	Max	Unit
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC}, V_{CCAUX} or V_{CCIO8} (whichever is the last) to the rising edge of INITN	—	—	33	ms
t_{VMC}	Time from t_{ICFG} to the valid Master CCLK	—	—	5	us
t_{CZ}	CCLK from Active to High-Z	—	—	300	ns
Master CCLK					
f_{MCLK}	Frequency	All selected frequencies	–20	20	%
$t_{MCLK-DC}$	Duty Cycle	All selected frequencies	40	60	%
All Configuration Modes					
t_{PRGM}	PROGRAMN LOW pulse accepted	—	110	—	ns
t_{PRGMRJ}	PROGRAMN LOW pulse rejected	—	—	50	ns
t_{INITL}	INITN LOW time	—	—	55	ns
t_{DPPINT}	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	150	ns
Slave SPI					
f_{CCLK}	CCLK input clock frequency	—	—	60	MHz
t_{CCLKH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{CCLKL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{STSU}	CCLK setup time	—	1	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{STCO}	CCLK falling edge to valid output	—	—	10	ns
t_{STOZ}	CCLK falling edge to valid disable	—	—	10	ns
t_{STOV}	CCLK falling edge to valid enable	—	—	10	ns
t_{SCS}	Chip Select HIGH time	—	25	—	ns
t_{SCSS}	Chip Select setup time	—	3	—	ns
t_{SCSH}	Chip Select hold time	—	3	—	ns
Master SPI					
f_{CCLK}	Max selected CCLK output frequency	—	—	62	MHz
t_{CCLKH}	CCLK output clock pulse width HIGH	—	3.5	—	ns
t_{CCLKL}	CCLK output clock pulse width LOW	—	3.5	—	ns
t_{STSU}	CCLK setup time	—	5	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{CSSPI}	INITN HIGH to Chip Select LOW	—	100	200	ns
t_{CFGX}	INITN HIGH to first CCLK edge	—	—	150	ns
Slave Serial					
f_{CCLK}	CCLK input clock frequency	—	—	66	MHz
t_{SSCH}	CCLK input clock pulse width HIGH	—	5	—	ns
t_{SSCL}	CCLK input clock pulse width LOW	—	5	—	ns
t_{SUSCDI}	CCLK setup time	—	0.5	—	ns
t_{HSCDI}	CCLK hold time	—	1.5	—	ns

4. Pinout Information

4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[L/R] [Group Number]_[A/B/C/D]	I/O	[L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIO A and B are grouped as a pair, and PIO C and D are group as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer. Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω.
P[T/B][Group Number]_[A/B]	I/O	[T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration. PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer. PIO A/B forms a pair of emulated differential output buffer.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins. V_{CC} = 1.1 V (ECP5), 1.2 V (ECP5UM5G)
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. V_{CCAUX} = 2.5 V.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x. V_{CCIO8} is used for configuration and JTAG.
VREF1_x	—	Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as VREF1 input. When not used, they may be used as I/O pins.
PLL, DLL and Clock Functions		
[LOC][_GPLL[T, C]_IN	I	General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not configured as GPLL input pads, they can be used as general purpose I/O pins.
GR_PCLK[Bank][num]	I	General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to ECP5 sysClock PLL/DLL Design and Usage Guide (TN1263). These pins are shared I/O pins. When not configured as GR pins, they can be used as general purpose I/O pins.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/ O pins. When not configured as PCLK pins, they can be used as general purpose I/O pins.

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.