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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	259
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-7bg554c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-7bg554c</a>

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## 2. Architecture

### 2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in [Figure 2.1](#) on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

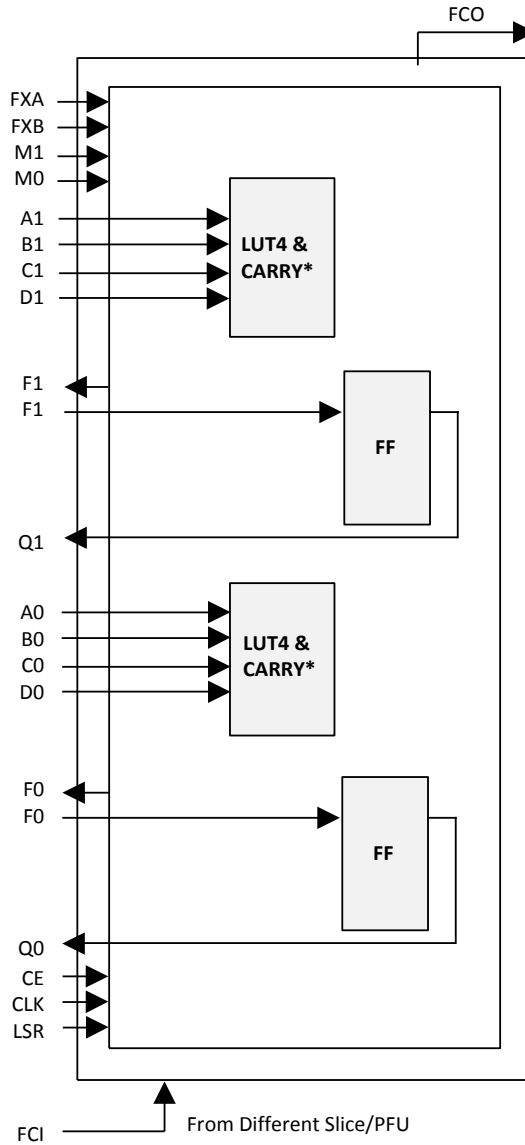
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG™ ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.



**Notes:** For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:  
WCK is CLK  
WRE is from LSR  
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2  
WAD [A:D] is a 4-bit address from slice 2 LUT input

**Figure 2.3. Slice Diagram**

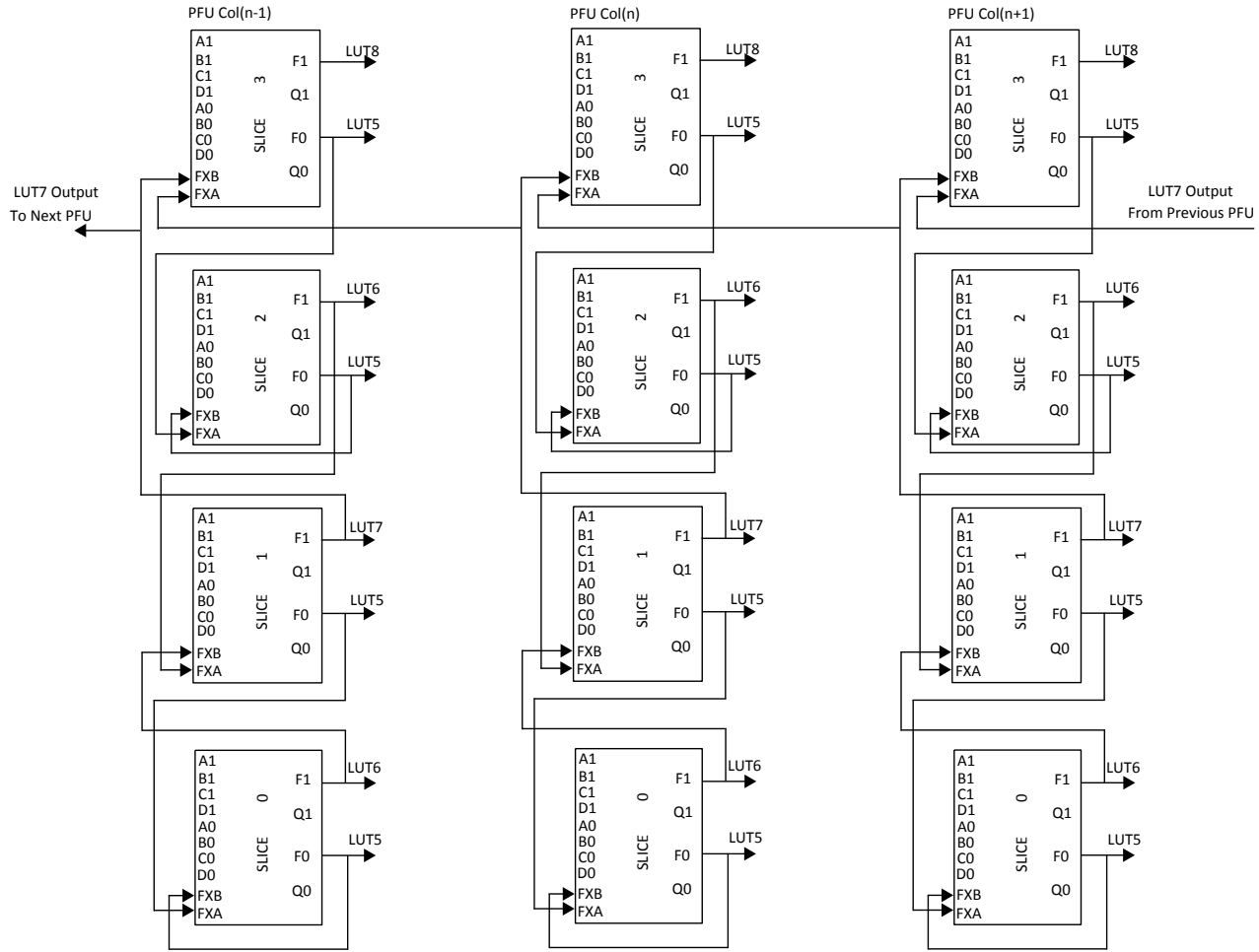


Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in <sup>1</sup>
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8 <sup>2</sup>
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8 <sup>2</sup>
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output <sup>1</sup>

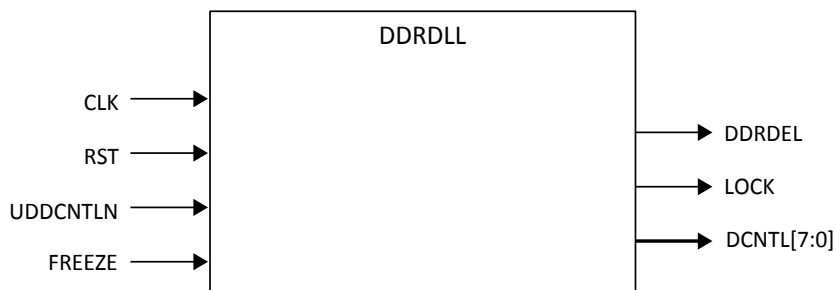
Notes:

1. See Figure 2.3 on page 15 for connection details.
2. Requires two adjacent PFUs.

## 2.7. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. [Figure 2.10](#) shows DDRDLL functional diagram.



**Figure 2.10. DDRDLL Functional Diagram**

**Table 2.5. DDRDLL Ports List**

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. [Figure 2.11](#) shows the DDRDLL and the slave DLLs on the top level view.

In [Figure 2.15](#), note that A\_ALU, B\_ALU and C\_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

[Table 2.7](#) shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

**Table 2.7. Maximum Number of Elements in a Slice**

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

**\*Note:** One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to [ECP5 and ECP5-5G sysDSP Usage Guide \(TN1267\)](#).

## 2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.



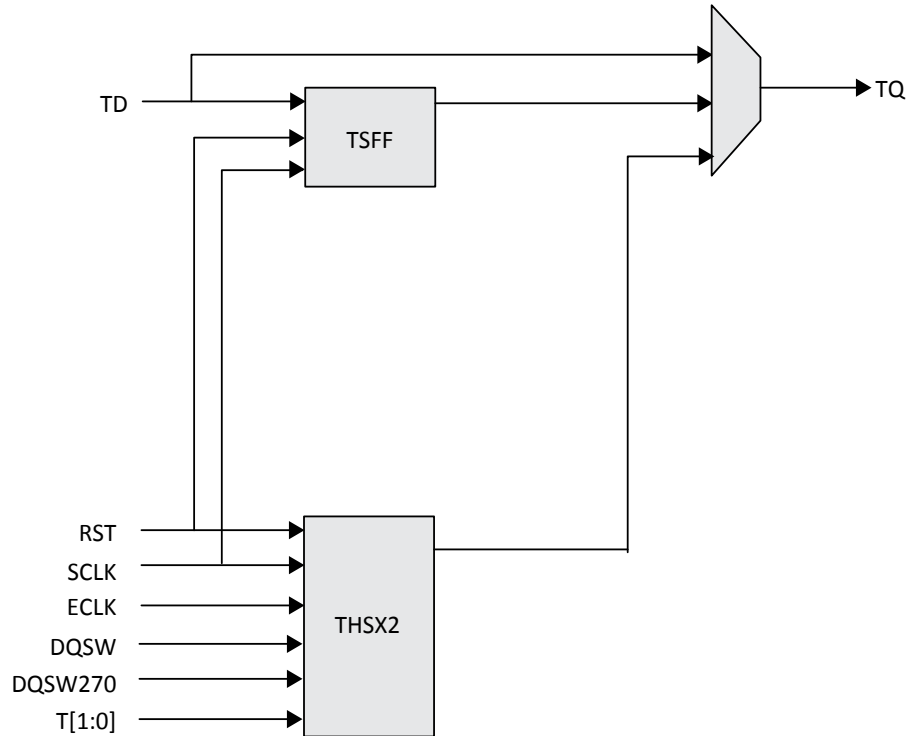


Figure 2.22. Tristate Register Block on Left and Right Sides

Table 2.10. Tristate Block Port Description

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR Register
RST	Input	Reset to the Tristate Block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

## 2.13. DDR Memory Support

### 2.13.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in Figure 2.23 on page 36. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as "virtual" VCCIO, by driving these pins to HIGH, with the user connecting these pins to VCCIO power supply. These connections create "soft" connections to VCCIO thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).

## 2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today’s systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTTL, LVPECL, and MIPI.

### 2.14.1. sysI/O Buffer Banks

ECP5/ECP5-5G devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank (Bank 8) is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O. For LFE5-85 devices, there is an additional I/O bank (Bank 4) that is not available in other device in the family.

In ECP5/ECP5-5G devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysI/O bank has its own I/O supply voltage ( $V_{CCIO}$ ). In addition, the banks on the Left and Right sides of the device, have voltage reference input (shared I/O pin),  $V_{REF1}$  per bank, which allow it to be completely independent of each other. The  $V_{REF}$  voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5/ECP5-5G devices, single-ended output buffers and ratioed input buffers (LVTTTL, and LVCMOS) are powered using  $V_{CCIO}$ . LVTTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of  $V_{CCIO}$ .

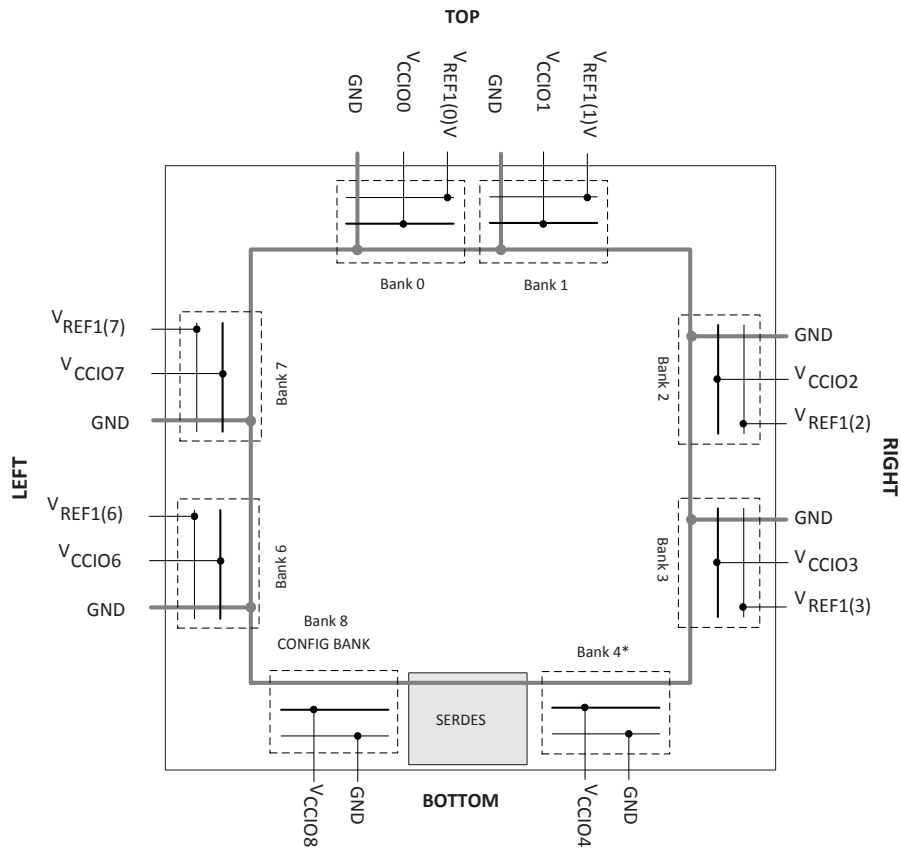


Figure 2.25. ECP5/ECP5-5G Device Family Banks

### 2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.

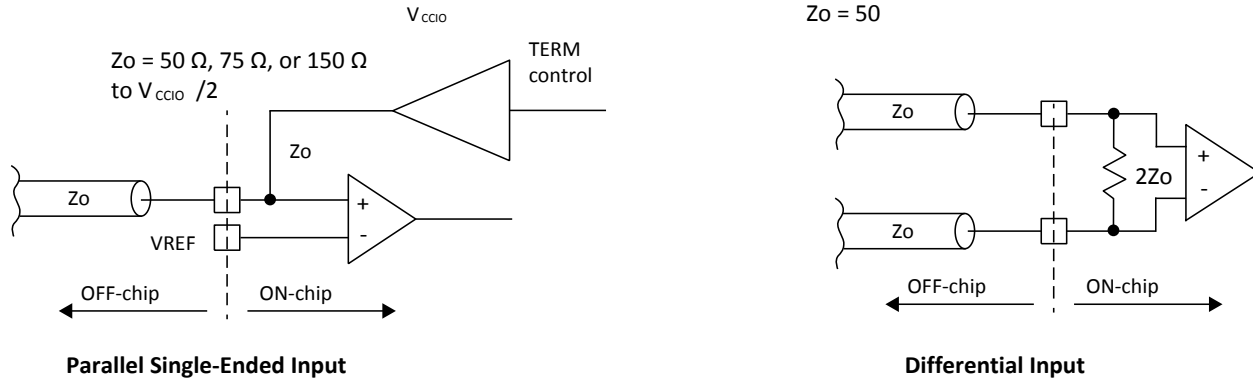


Figure 2.26. On-Chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2^*$	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

**\*Notes:**

TERMINATE to  $V_{CCIO}/2$  (Single-Ended) and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to  $V_{CCIO}/2$  and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance  $\pm 20\%$ .

Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for on-chip termination usage and value ranges.

### 2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the [Hot Socketing Specifications](#) section on page 48.

### 2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. [Table 2.15](#) lists the allowable combination of primary and secondary protocol combinations.

### 2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

[Table 2.15](#) lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

**Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support**

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

### 2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#).

### 3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

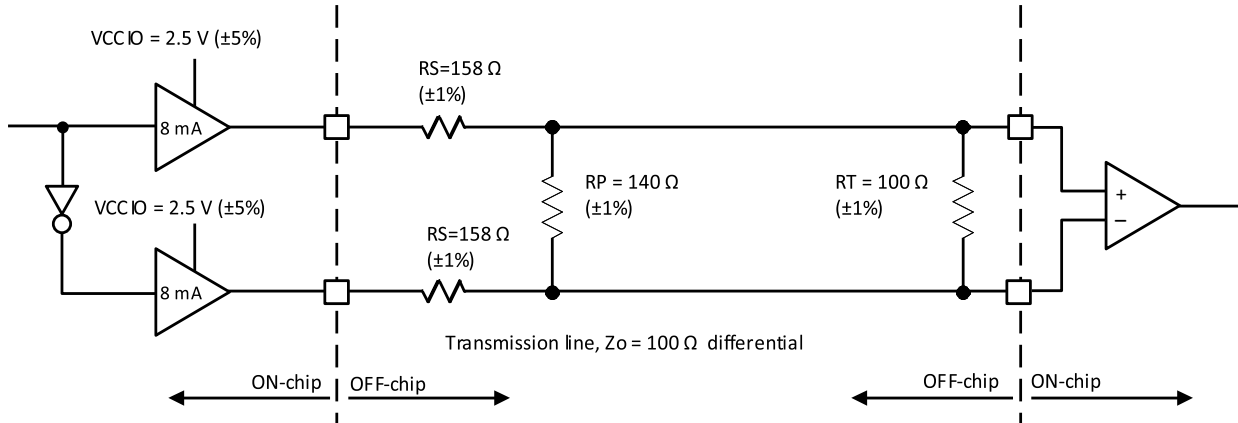


Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V <sub>CCIO</sub>	Output Driver Supply (±5%)	2.50	V
Z <sub>OUT</sub>	Driver Impedance	20	Ω
R <sub>S</sub>	Driver Series Resistor (±1%)	158	Ω
R <sub>P</sub>	Driver Parallel Resistor (±1%)	140	Ω
R <sub>T</sub>	Receiver Termination (±1%)	100	Ω
V <sub>OH</sub>	Output High Voltage	1.43	V
V <sub>OL</sub>	Output Low Voltage	1.07	V
V <sub>OD</sub>	Output Differential Voltage	0.35	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	V
Z <sub>BACK</sub>	Back Impedance	100.5	Ω
I <sub>DC</sub>	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

### 3.14.8. SLVS

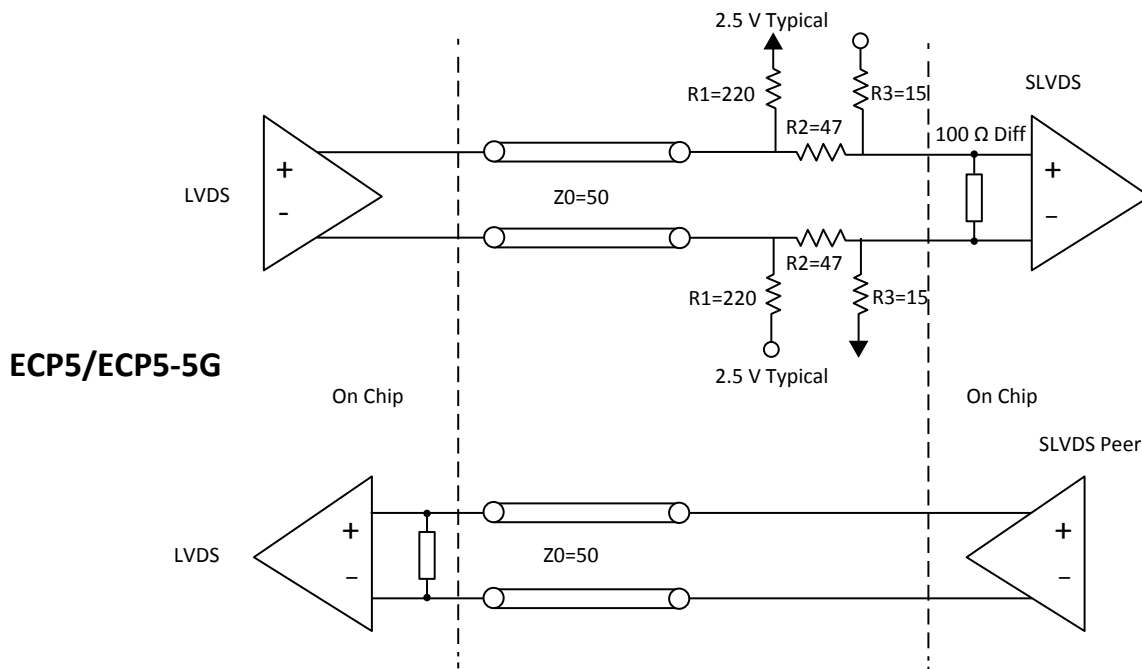
Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

**Table 3.18. Input to SLVS**

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.



**Figure 3.5. SLVS Interface**

### 3.18. External Switching Characteristics

Over recommended commercial operating conditions.

**Table 3.22. ECP5/ECP5-5G External Switching Characteristics**

Parameter	Description	Device	-8		-7		-6		Unit
			Min	Max	Min	Max	Min	Max	
<b>Clocks</b>									
<b>Primary Clock</b>									
$f_{MAX\_PRI}$	Frequency for Primary Clock Tree	—	—	370	—	303	—	257	MHz
$t_{W\_PRI}$	Clock Pulse Width for Primary Clock	—	0.8	—	0.9	—	1.0	—	ns
$t_{SKEW\_PRI}$	Primary Clock Skew within a Device	—	—	420	—	462	—	505	ps
<b>Edge Clock</b>									
$f_{MAX\_EDGE}$	Frequency for Edge Clock Tree	—	—	400	—	350	—	312	MHz
$t_{W\_EDGE}$	Clock Pulse Width for Edge Clock	—	1.175	—	1.344	—	1.50	—	ns
$t_{SKEW\_EDGE}$	Edge Clock Skew within a Bank	—	—	160	—	180	—	200	ps
<b>Generic SDR Input</b>									
<b>General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL</b>									
$t_{CO}$	Clock to Output - PIO Output Register	All Devices	—	5.4	—	6.1	—	6.8	ns
$t_{SU}$	Clock to Data Setup - PIO Input Register	All Devices	0	—	0	—	0	—	ns
$t_H$	Clock to Data Hold - PIO Input Register	All Devices	2.7	—	3	—	3.3	—	ns
$t_{SU\_DEL}$	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	—	1.33	—	1.46	—	ns
$t_{H\_DEL}$	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
$f_{MAX\_IO}$	Clock Frequency of I/O and PFU Register	All Devices	—	400	—	350	—	312	MHz
<b>General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL</b>									
$t_{COPLL}$	Clock to Output - PIO Output Register	All Devices	—	3.5	—	3.8	—	4.1	ns
$t_{SUPLL}$	Clock to Data Setup - PIO Input Register	All Devices	0.7	—	0.78	—	0.85	—	ns
$t_{HPLL}$	Clock to Data Hold - PIO Input Register	All Devices	0.8	—	0.89	—	0.98	—	ns
$t_{SU\_DEPLL}$	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	—	1.78	—	1.95	—	ns

### 3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

**Table 3.23. sysCLOCK PLL Timing**

Parameter	Descriptions	Conditions	Min	Max	Units
$f_{IN}$	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
$f_{OUT}$	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
$f_{VCO}$	PLL VCO Frequency	—	400	800	MHz
$f_{PFD}^3$	Phase Detector Input Frequency	—	10	400	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle	—	45	55	%
$t_{PH4}$	Output Phase Accuracy	—	-5	5	%
$t_{OPJIT}^1$	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
$t_{SPO}$	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
$t_W$	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
$t_{LOCK}^2$	PLL Lock-in Time	—	—	15	ms
$t_{UNLOCK}$	PLL Unlock Time	—	—	50	ns
$t_{IPJIT}$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{HI}$	Input Clock High Time	90% to 90%	0.5	—	ns
$t_{LO}$	Input Clock Low Time	10% to 10%	0.5	—	ns
$t_{RST}$	RST/ Pulse Width	—	1	—	ms
$t_{RSTREC}$	RST Recovery Time	—	1	—	ns
$t_{LOAD\_REG}$	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain "0" or	—	4	—	VCO cycles

**Notes:**

- Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
- Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
- Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PFD} > 10$  MHz. For  $f_{PFD} < 10$  MHz, the jitter numbers may not be met in certain conditions.



**Table 3.36. Receive and Jitter Tolerance**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z <sub>RX_DIFF</sub>	Differential termination resistance	—	80	100	120	Ω
J <sub>RX_DJ</sub> <sup>2, 3, 4</sup>	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J <sub>RX_RJ</sub> <sup>2, 3, 4</sup>	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J <sub>RX_SJ</sub> <sup>2, 3, 4</sup>	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3, 4</sup>	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T <sub>RX_EYE</sub>	Receiver eye opening	—	0.35	—	—	UI

**Notes:**

- Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
- Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
- Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
- Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

## 3.29. Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics

### 3.29.1. AC and DC Characteristics

**Table 3.37. Transmit**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T <sub>RF</sub>	Differential rise/fall time	20% to 80%	—	80	—	ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance	—	80	100	120	Ω
J <sub>TX_DDJ</sub> <sup>2, 3</sup>	Output data deterministic jitter	—	—	—	0.10	UI
J <sub>TX_TJ</sub> <sup>1, 2, 3</sup>	Total output data jitter	—	—	—	0.24	UI

**Notes:**

- Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
- Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
- Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

**Table 3.38. Receive and Jitter Tolerance**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z <sub>RX_DIFF</sub>	Differential termination resistance	—	80	100	120	Ω
J <sub>RX_DJ</sub> <sup>1, 2, 3, 4</sup>	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.34	UI
J <sub>RX_RJ</sub> <sup>1, 2, 3, 4</sup>	Random jitter tolerance (peak-to-peak)	—	—	—	0.26	UI
J <sub>RX_SJ</sub> <sup>1, 2, 3, 4</sup>	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.11	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3, 4</sup>	Total jitter tolerance (peak-to-peak)	—	—	—	0.71	UI
T <sub>RX_EYE</sub>	Receiver eye opening	—	0.29	—	—	UI

**Notes:**

- Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
- Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
- Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
- Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

### 3.31. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

**Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications**

Symbol	Parameter		Min	Max	Unit
<b>POR, Configuration Initialization, and Wakeup</b>					
$t_{ICFG}$	Time from the Application of $V_{CC}$ , $V_{CCAUX}$ or $V_{CCIO8}$ (whichever is the last) to the rising edge of INITN	—	—	33	ms
$t_{VMC}$	Time from $t_{ICFG}$ to the valid Master CCLK	—	—	5	us
$t_{CZ}$	CCLK from Active to High-Z	—	—	300	ns
<b>Master CCLK</b>					
$f_{MCLK}$	Frequency	All selected frequencies	-20	20	%
$t_{MCLK-DC}$	Duty Cycle	All selected frequencies	40	60	%
<b>All Configuration Modes</b>					
$t_{PRGM}$	PROGRAMN LOW pulse accepted	—	110	—	ns
$t_{PRGMRJ}$	PROGRAMN LOW pulse rejected	—	—	50	ns
$t_{INITL}$	INITN LOW time	—	—	55	ns
$t_{DPPINT}$	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
$t_{IODISS}$	PROGRAMN LOW to I/O Disabled	—	—	150	ns
<b>Slave SPI</b>					
$f_{CCLK}$	CCLK input clock frequency	—	—	60	MHz
$t_{CCLKH}$	CCLK input clock pulsewidth HIGH	—	6	—	ns
$t_{CCLKL}$	CCLK input clock pulsewidth LOW	—	6	—	ns
$t_{STSU}$	CCLK setup time	—	1	—	ns
$t_{STH}$	CCLK hold time	—	1	—	ns
$t_{STCO}$	CCLK falling edge to valid output	—	—	10	ns
$t_{STOZ}$	CCLK falling edge to valid disable	—	—	10	ns
$t_{STOV}$	CCLK falling edge to valid enable	—	—	10	ns
$t_{SCS}$	Chip Select HIGH time	—	25	—	ns
$t_{SCSS}$	Chip Select setup time	—	3	—	ns
$t_{SCSH}$	Chip Select hold time	—	3	—	ns
<b>Master SPI</b>					
$f_{CCLK}$	Max selected CCLK output frequency	—	—	62	MHz
$t_{CCLKH}$	CCLK output clock pulse width HIGH	—	3.5	—	ns
$t_{CCLKL}$	CCLK output clock pulse width LOW	—	3.5	—	ns
$t_{STSU}$	CCLK setup time	—	5	—	ns
$t_{STH}$	CCLK hold time	—	1	—	ns
$t_{CSSPI}$	INITN HIGH to Chip Select LOW	—	100	200	ns
$t_{CFGX}$	INITN HIGH to first CCLK edge	—	—	150	ns
<b>Slave Serial</b>					
$f_{CCLK}$	CCLK input clock frequency	—	—	66	MHz
$t_{SSCH}$	CCLK input clock pulse width HIGH	—	5	—	ns
$t_{SSCL}$	CCLK input clock pulse width LOW	—	5	—	ns
$t_{SUSCDI}$	CCLK setup time	—	0.5	—	ns
$t_{HS CDI}$	CCLK hold time	—	1.5	—	ns

**Table 3.44. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>	Timing Ref.	V <sub>T</sub>
LVTTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V <sub>CCIO</sub> /2	V <sub>CCIO</sub>
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V <sub>OH</sub> - 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V <sub>OL</sub> + 0.10	V <sub>CCIO</sub>

**Note:** Output test conditions for all other interfaces are determined by the respective standards.

Signal Name	I/O	Description
<b>Configuration Pads (Used during sysCONFIG) (Continued)</b>		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
<b>SERDES Function</b>		
VCCA <sub>x</sub>	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All VCCA supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect VCCA to VCC. VCCA <sub>x</sub> = 1.1 V for ECP5, VCCA <sub>x</sub> = 1.2 V for ECP5-5G.
VCCAUX <sub>Ax</sub>	—	SERDES Aux Power Supply pin for SERDES Dual x. VCCAUX <sub>Ax</sub> = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5, or 1.2 V on ECP5-5G.

**Notes:**

- When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
- These pins are dedicated inputs or can be used as general purpose I/O.
- m defines the associated channel in the quad.



7<sup>th</sup> Floor, 111 SW 5<sup>th</sup> Avenue  
Portland, OR 97204, USA  
T 503.268.8000  
[www.latticesemi.com](http://www.latticesemi.com)