Lattice Semiconductor Corporation - LFE5UM-85F-7BG554I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	259
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-7bg554i

Figures

2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - P Œ rššZ Œ Œ‹µ r}
  - v }r‹µ r}
  - o r Z rŒ‹µ r}

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90° phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90° shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL, DLLDEL, that takes a clock input and generates a 90° shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90° clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delay code.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. The code is the DCNTL[7:0] outputs. These outputs are updated when the UDDCNTLN signal is LOW.
FREEZE	Input	FREEZE goes high and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes low, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are four identical DDRDLLs, one in each of the four corners in LFE5-85 and LFE5-45 devices, and two DDRDLLs in both LFE5-25 & LFE5-12 devices in the upper two corners. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL (DQSBUF and DLLDEL) use the code to delay the signal, to create the phase shifted signal used for either DDR memory, to create 90° shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

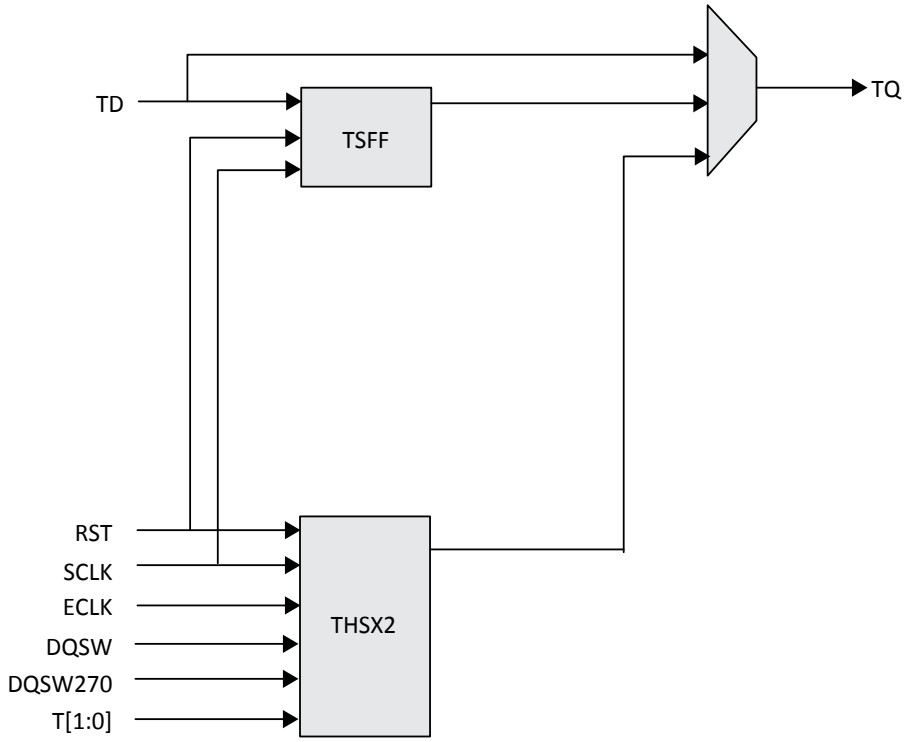


Figure 2.22. Tristate Register Block on Left and Right Sides

Table 2.10. Tristate Block Port Description

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR Register
RST	Input	Reset to the Tristate Block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.13. DDR Memory Support

2.13.1. DQS Grouping for DDR Memory

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in Figure 2.23 on page 36. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. In DQS groups with more than 11 pins bonded out, up to two pre-defined pins are assigned to be used as "virtual" VCCIO, by driving these pins to HIGH, with the user connecting these pins to VCCIO power supply. These connections create "soft" connections to V_{CCIO} thru these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

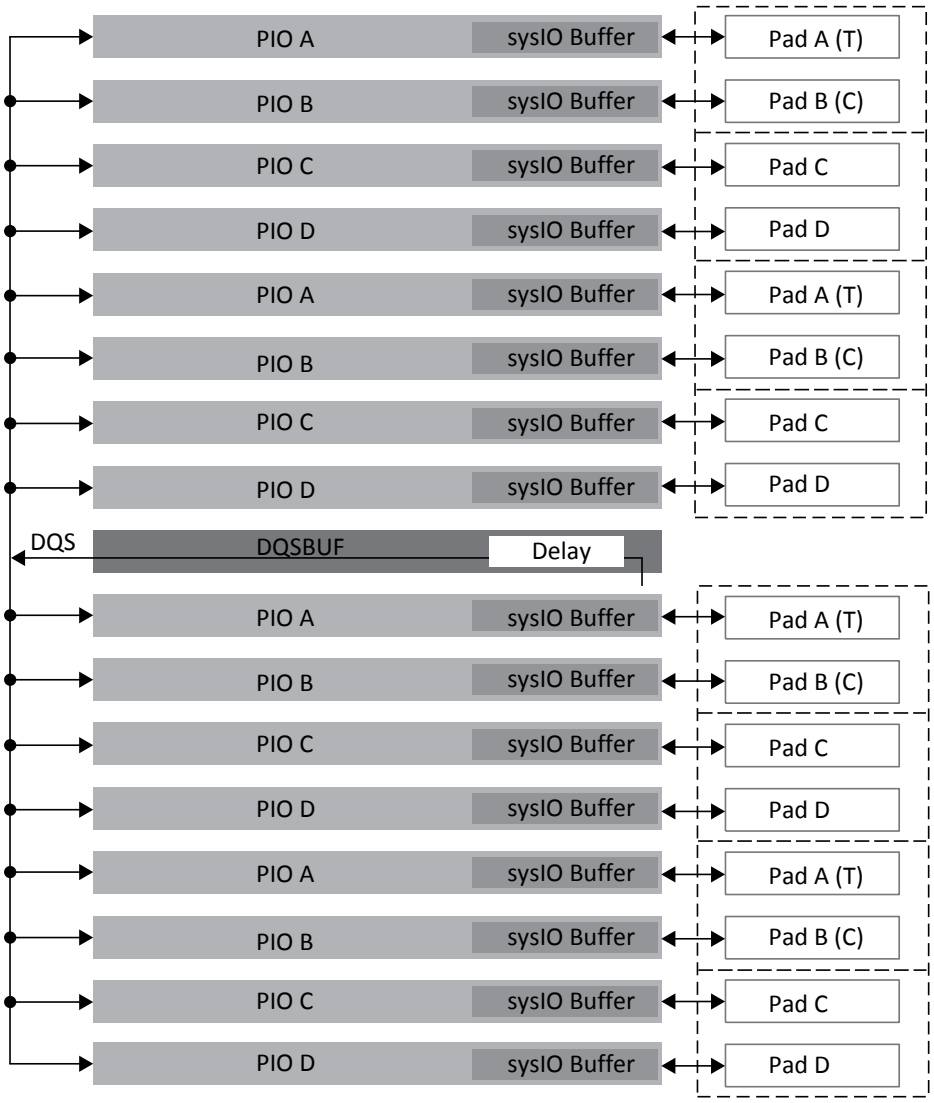


Figure 2.23. DQS Grouping on the Left and Right Edges

2.13.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR2/3, LPDDR2/3), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifted is achieved by using DQSDEL programmable delay line in the DQS Delay Block (DQS read circuit). The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block shown in Figure 2.24 generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. Figure 2.27 shows the position of the dual blocks for the LFE5-85. Table 2.13 shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE t 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B t ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

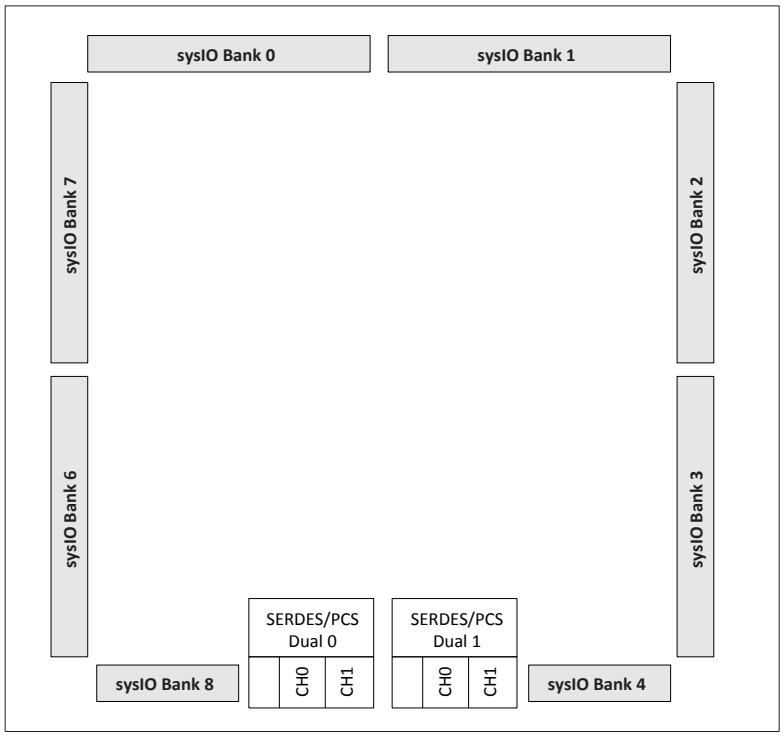


Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 [2]	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 [2]	x1	8b10b
SD-SDI (259M, 344M) [1]	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	v	v
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	t0.5	1.32	V
V_{CCA}	Supply Voltage	t0.5	1.32	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	t0.5	2.75	V
V_{CCIO}	Supply Voltage	t0.5	3.63	V
v	Input or I/O Transient Voltage Applied	t0.5	3.63	V
V_{CCHRX}, V_{CCHTX}	SERDES RX/TX Buffer Supply Voltages	t0.5	1.32	V
v	Voltage Applied on SERDES Pins	t0.5	1.80	V
T_A	Storage Temperature (Ambient)	t65	150	°C
T_J	Junction Temperature	v	+125	°C

Notes:

1. Stress above those listed µ v Œ š Z ^ •} o µ š D Æ] u µ u Z š] v P • _ u Ç µ • ‰ Œ u v v š u P š } operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[2]	Core Supply Voltage	ECP5	1.045	1.155	V
		ECP5-5G	1.14	1.26	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage	v	2.375	2.625	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	v	1.14	3.465	V
V_{REF}[1]	Input Reference Voltage	v	0.5	1.0	V
t_{JCOM}	Junction Temperature, Commercial Operation	v	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	v	t40	100	°C
SERDES External Power Supply[5]					
V_{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.164	1.236	V
V_{CCAUXA}	SERDES Auxiliary Supply Voltage	v	2.374	2.625	V
V_{CCHRX}[6]	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
		ECP5-5G	0.30	1.26	V
V_{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V
		ECP5-5G	1.14	1.26	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 on page 48.
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
5. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the Rx section of this Data Sheet.

3.7. Hot Socketing Requirements

Table 3.6. Hot Socketing Requirements

Description	Min	Typ	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	v	v	8	mA
Input current per HDIN pin when device power supply is off, inputs driven[1, 2]	v	v	15	mA
Current per HDIN pin when device power ramps up, input driven[3]	v	v	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up[4]	v	v	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, no external AC coupling.
2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.
3. Device power supplies are ramping up (V_{CCA} and V_{CCAUX}), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, internal AC coupling.
4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to V_{CCHTX} by the far end receiver termination of 50 Ωsingle ended.

3.8. ESD Performance

Refer to the ECP5 and ECP5-5G Product Family Qualification Summary for complete qualification data, including ESD performance.

3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4]	Input or I/O Low Leakage	0 dV$_{IN}$ dV$_{CCIO}$	v	v	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	V$_{CCIO}$ < V$_{IN}$ dV$_{IH(MAX)}$	v	v	100	µA
I_{PU}	I/O Active Pull-up Current, sustaining logic HIGH state	0.7 V$_{CCIO}$ dV$_{IN}$ dV$_{CCIO}$	t30	v	v	µA
	I/O Active Pull-up Current, pulling down from logic HIGH state	0 dV$_{IN}$ d0.7 V$_{CCIO}$	v	v	t150	µA
I_{PD}	I/O Active Pull-down Current, sustaining logic LOW state	0 dV$_{IN}$ d V$_{IL}$ (MAX)	30	v	v	µA
	I/O Active Pull-down Current, pulling up from logic LOW state	0 dV$_{IN}$ dV$_{CCIO}$	v	v	150	µA
C1	I/O Capacitance[2]	V$_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V$_{CC}$ = 1.2 V, V$_{IO}$ = 0 to V$_{IH(MAX)}$	v	5	8	pf
C2	Dedicated Input Capacitance[2]	V$_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V$_{CC}$ = 1.2 V, V$_{IO}$ = 0 to V$_{IH(MAX)}$	v	5	7	pf
V_{HYST}	Hysteresis for Single-Ended Inputs	V$_{CCIO}$ = 3.3 V	v	300	v	mV
		V$_{CCIO}$ = 2.5 V	v	250	v	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as V_{REF}, maximum leakage= 25 µA.

3.17. Maximum I/O Buffer Speed

Over recommended operating conditions.

Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
MIPI D-PHY (HS Mode)	MIPI Video	400	MHz
SLVS	SLVS similar to MIPI	400	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL_12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	200	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	200	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	200	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	200	MHz
LVCMOS15	LVCMOS 1.5, V_{CCIO} = 1.5 V	200	MHz
LVCMOS12	LVCMOS 1.2, V_{CCIO} = 1.2 V	200	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	150	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, VCCIO = 3.3 V	150	MHz
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	150	MHz
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	150	MHz
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	150	MHz
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	150	MHz
LVCMOS12 (For all drives)	LVCMOS, 1.2 V	150	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Switching Test Conditions, Table 3.44 on page 90.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.26. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	v	4	v	1	byte clk
	FPGA Bridge - Gearing enabled	5	v	7	v	v	word clk
T2	8b10b Encoder	v	v	v	2	1	byte clk
T3	SERDES Bridge transmit	v	v	v	2	1	byte clk
T4	Serializer: 8-bit mode	v	v	v	15 + '1	v	UI + ps
	Serializer: 10-bit mode	v	v	v	18 + '1	v	UI + ps
T5	Pre-emphasis ON	v	v	v	1 + '2	v	UI + ps
	Pre-emphasis OFF	v	v	v	0 + '3	v	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	v	v	v	'1	v	UI + ps
	Equalization OFF	v	v	v	'2	v	UI + ps
R2	Deserializer: 8-bit mode	v	v	v	10 + '3	v	UI + ps
	Deserializer: 10-bit mode	v	v	v	12 + '3	v	UI + ps
R3	SERDES Bridge receive	v	v	v	2	v	byte clk
R4	Word alignment	3.1	v	4	v	1	byte clk
R5	8b10b decoder	v	v	v	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	v	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	v	5	v	1	byte clk
	FPGA Bridge - Gearing enabled	7	v	9	v	v	word clk

Notes:

1. '1 = t245 ps, '2 = +88 ps, '3 = +112 ps.
2. '1 = +118 ps, '2 = +132 ps, '3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

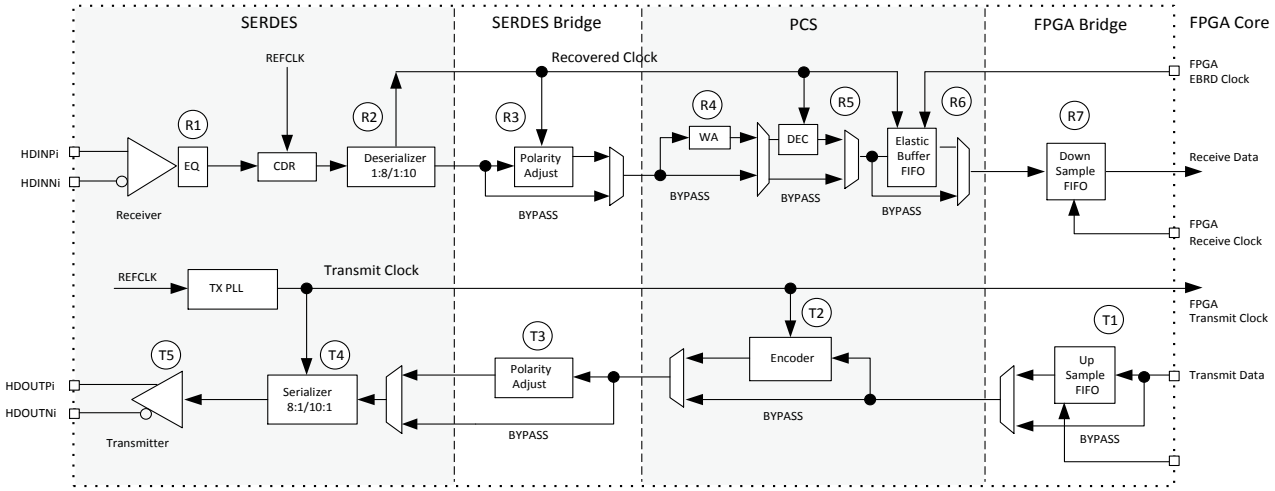


Figure 3.13. Transmitter and Receiver Latency Block Diagram

3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.39. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDO}	Serial data rate	v	270	v	2975	Mb/s
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	270 Mb/s[6]	v	v	0.2	UI
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	1485 Mb/s	v	v	0.2	UI
$T_{JALIGNMENT}$[1, 2]	Serial output jitter, alignment	2970 Mb/s	v	v	0.3	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mb/s[6]	v	v	0.2	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mb/s	v	v	1	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mb/s	v	v	2	UI

Notes:
1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice SERDES device configured to ñ ì Q output impedance connecting to the external cable driver with differential signaling.
4. The cable driver drives: RL=75 QAC-coupled at 270, 1485, or 2970 Mb/s.
5. All LFE5UM/LFE5UM5G devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.
6. 270 Mb/s is supported with Rate Divider only.

Table 3.40. Receive

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDI}	Serial input data rate	v	270	v	2970	Mb/s

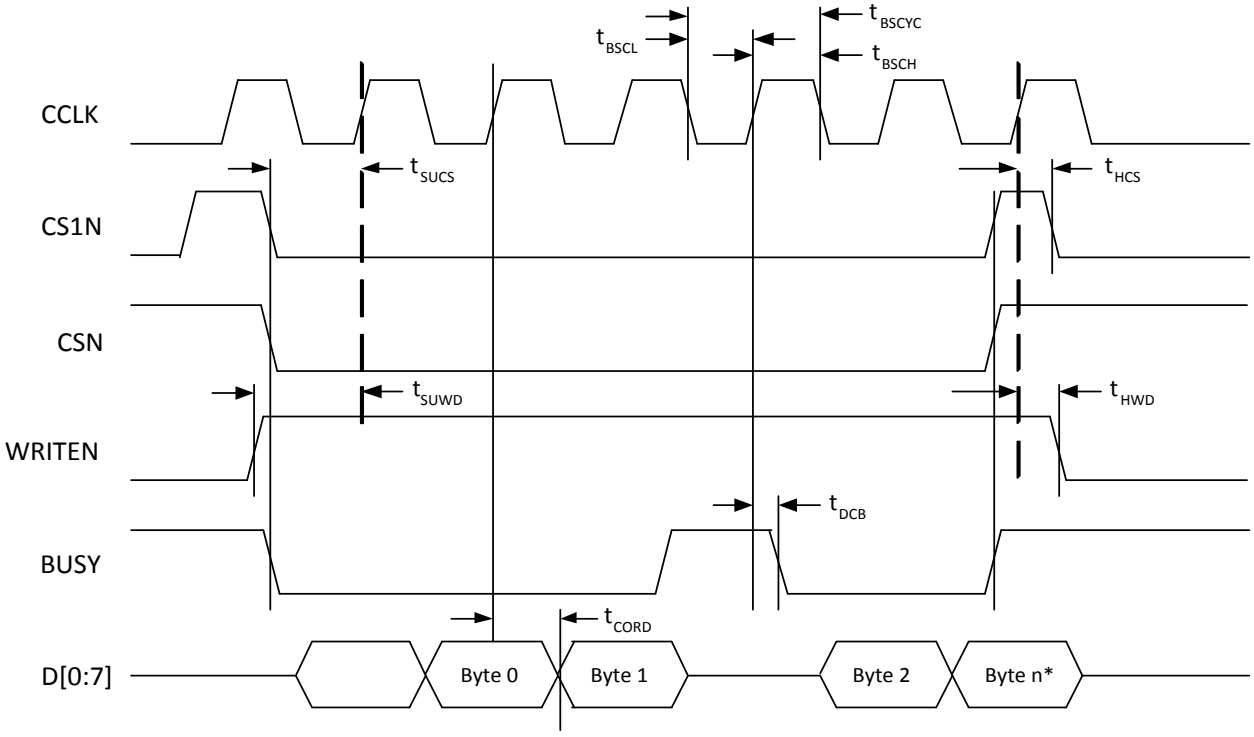
Table 3.41. Reference Clock

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F_{VCLK}	Video output clock frequency	v	54	v	148.5	MHz
DC_V	Duty cycle, video clock	v	45	50	55	%

Note: SD-SDI (270 Mb/s) is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications *(Continued)*

Symbol	Parameter		Min	Max	Unit
Slave Parallel					
f_{CCLK}	CCLK input clock frequency	v	v	50	MHz
t_{BSCH}	CCLK input clock pulsewidth HIGH	v	6	v	ns
t_{BSCL}	CCLK input clock pulsewidth LOW	v	6	v	ns
t_{CORD}	CCLK to DOUT for Read Data	v	v	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	v	1.5	v	ns
t_{HCBDI}	Data Hold Time to CCLK	v	1.5	v	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	v	2.5	v	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	v	1.5	v	ns
t_{SUWD}	WRITEN Setup Time to CCLK	v	45	v	ns
t_{HCWD}	WRITEN Hold Time to CCLK	v	2	v	ns
t_{DCB}	CCLK to BUSY Delay Time	v	v	12	ns



*n = last byte of read cycle.

Figure 3.15. sysCONFIG Parallel Port Read Cycle

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-45F-8BG554C	t8	Lead free caBGA	554	Commercial	44	No
LFE5U-85F-6MG285C	t6	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-7MG285C	t7	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-8MG285C	t8	Lead free csfBGA	285	Commercial	84	No
LFE5U-85F-6BG381C	t6	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-7BG381C	t7	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-8BG381C	t8	Lead free caBGA	381	Commercial	84	No
LFE5U-85F-6BG554C	t6	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-7BG554C	t7	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-8BG554C	t8	Lead free caBGA	554	Commercial	84	No
LFE5U-85F-6BG756C	t6	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-7BG756C	t7	Lead free caBGA	756	Commercial	84	No
LFE5U-85F-8BG756C	t8	Lead free caBGA	756	Commercial	84	No
LFE5UM-25F-6MG285C	t6	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-7MG285C	t7	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-8MG285C	t8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM-25F-6BG381C	t6	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-7BG381C	t7	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-25F-8BG381C	t8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM-45F-6MG285C	t6	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-7MG285C	t7	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-8MG285C	t8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM-45F-6BG381C	t6	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-7BG381C	t7	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-8BG381C	t8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM-45F-6BG554C	t6	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-7BG554C	t7	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-45F-8BG554C	t8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM-85F-6MG285C	t6	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-7MG285C	t7	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-8MG285C	t8	Lead free csfBGA	285	Commercial	84	Yes
LFE5UM-85F-6BG381C	t6	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-7BG381C	t7	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-8BG381C	t8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM-85F-6BG554C	t6	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-7BG554C	t7	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-8BG554C	t8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM-85F-6BG756C	t6	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-7BG756C	t7	Lead free caBGA	756	Commercial	84	Yes
LFE5UM-85F-8BG756C	t8	Lead free caBGA	756	Commercial	84	Yes
LFE5UM5G-25F-8MG285C	t8	Lead free csfBGA	285	Commercial	24	Yes
LFE5UM5G-25F-8BG381C	t8	Lead free caBGA	381	Commercial	24	Yes
LFE5UM5G-45F-8MG285C	t8	Lead free csfBGA	285	Commercial	44	Yes
LFE5UM5G-45F-8BG381C	t8	Lead free caBGA	381	Commercial	44	Yes
LFE5UM5G-45F-8BG554C	t8	Lead free caBGA	554	Commercial	44	Yes
LFE5UM5G-85F-8MG285C	t8	Lead free csfBGA	285	Commercial	84	Yes

Supplemental Information

For Further Information

A variety of technical notes for the ECP5/ECP5-5G family are available.

- High-Speed PCB Design Considerations (TN1033)
- Transmission of High-Speed Serial Signals Over Common Cable Media (TN1066)
- PCB Layout Recommendations for BGA Packages (TN1074)
- Minimizing System Interruption During Configuration Using TransFR Technology (TN1087)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- LatticeECP3, ECP-5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184)
- Using TraceID (TN1207)
- Sub-LVDS Signaling Using Lattice Devices (TN1210)
- Advanced Security Encryption Key Programming Guide for ECP5, ECP5-5G, LatticeECP3, and LatticeECP2/MS Devices (TN1215)
- LatticeECP3, LatticeECP2/M, ECP5 and ECP5-5G Dual Boot and Multiple Boot Feature (TN1216)
- ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260)
- ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261)
- ECP5 and ECP5-5G sysIO Usage Guide (TN1262)
- ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263)
- ECP5 and ECP5-5G Memory Usage Guide (TN1264)
- ECP5 and ECP5-5G High-Speed I/O Interface (TN1265)
- Power Consumption and Management for ECP5 and ECP5-5G Devices (TN1266)
- ECP5 and ECP5-5G sysDSP Usage Guide (TN1267)
- ECP5 and ECP5-5G Hardware Checklist (FPGA-TN-02038)
- Solder Reflow Guide for Surface Mount Devices (FPGA-TN-02041)
- ECP5 and ECP5-5G PCI Express Soft IP Ease of Use Guidelines (FPGA-TN-02045)
- Programming External SPI Flash through JTAG for ECP5/ECP5-5G (FPGA-TN-02050)
- Adding Scalable Power and Thermal Management to ECP5 Using L-ASC10 (AN6095)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL): www.jedec.org
- PCI: www.pcisig.com

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Date	Version	Section	Change Summary
November 2015	1.5	All	Added ECP5-5G device family.
			Changed document title to ECP5 and ECP5-5G Family Data Sheet.
	1.4	General Description	Updated Features section. Added support for eDP in RDR and HDR.
		Architecture	Updated Overview section. Revised Figure 2.1. Simplified Block Diagram, LFE5UM/LFE5UM5G-85 Device (Top Level). Modified Flexible sysIO description and Note.
			Updated SERDES and Physical Coding Sublayer section. x Changed E.24.V in CPRI protocol to E.24.LV. x Z u } À ^ í X í s _ (Œ } u ‰ Œ P Œ ‰ Z } v µ v
		DC and Switching Characteristics	Updated Hot Socketing Requirements section. Revised V_{CCHTX} in table notes 1 and 3. Indicated V_{CCHTX} in table note 4.
			Updated SERDES High-Speed Data Transmitter section. Revised V_{CCHTX} in table note 1.
		Ordering Information	Updated ECP5/ECP5-5G Part Number Description section. Changed ^ > & ñ & W ' _ µ v Œ À] & u] o Ç š } ^ W ñ
August 2015	1.3	General Description	Updated Features section. x Removed SMPTE3G under Embedded SERDES. x Added Single Event Upset (SEU) Mitigation Support. Removed SMPTE protocol in fifth paragraph.
		Architecture	General update.
		DC and Switching Characteristics	General update.
		Pinout Information	Updated Signal Descriptions section. Revised the descriptions of the following signals: x P[L/R] [Group Number]_[A/B/C/D] x P[T/B][Group Number]_[A/B] x D4/IO4 (Previously named D4/MOSI2/IO4) x D5/IO5 (Previously named D5/MISO/IO5) x VCCHRX_D[dual_num]CH[chan_num] x VCCHTX_D[dual_num]CH[chan_num]
		Supplemental Information	Added TN1184 reference.

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Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section. x Deleted Serial RapidIO protocol under Embedded SERDES. x Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3. Mentioned transmit de- u ‰ Z •] • - and % œ - µ Œ • } Œ • _ X
		Architecture	Updated Overview section. x Revised description of PFU blocks. x Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section. x Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. x Deleted Serial RapidIO protocol. x Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section. x o š ^ í ï ì ± Ð ñ Ò D K ^ _ } •] o o š } Œ X x Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA}.
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to t_{SKEW_PR} V_{CCA} and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.

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Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.