Lattice Semiconductor Corporation - LFE5UM-85F-7MG285I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-7mg285i

Tables

1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 84K LUTs
  - 197 to 365 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 3.744 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs

  - Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 18/15 I, II
  - HSUL12
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
  - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
  - Shared bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
  - Soft Error Detect – Embedded hard macro
  - Soft Error Correction – Without stopping user operation
  - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - On-chip oscillator for initialization and general use
  - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U-12	LFE5U-25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels / IO Count)							
256 caBGA (14 x 14 mm², 0.8 mm)	—	—	—	0/197	0/197	0/197	—
285 csfBGA (10 x 10 mm², 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm², 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm², 0.8 mm)	—	4/245	4/259	—	—	0/245	0/259
756 caBGA (27 x 27 mm², 0.8 mm)	—	—	4/365	—	—	—	0/365

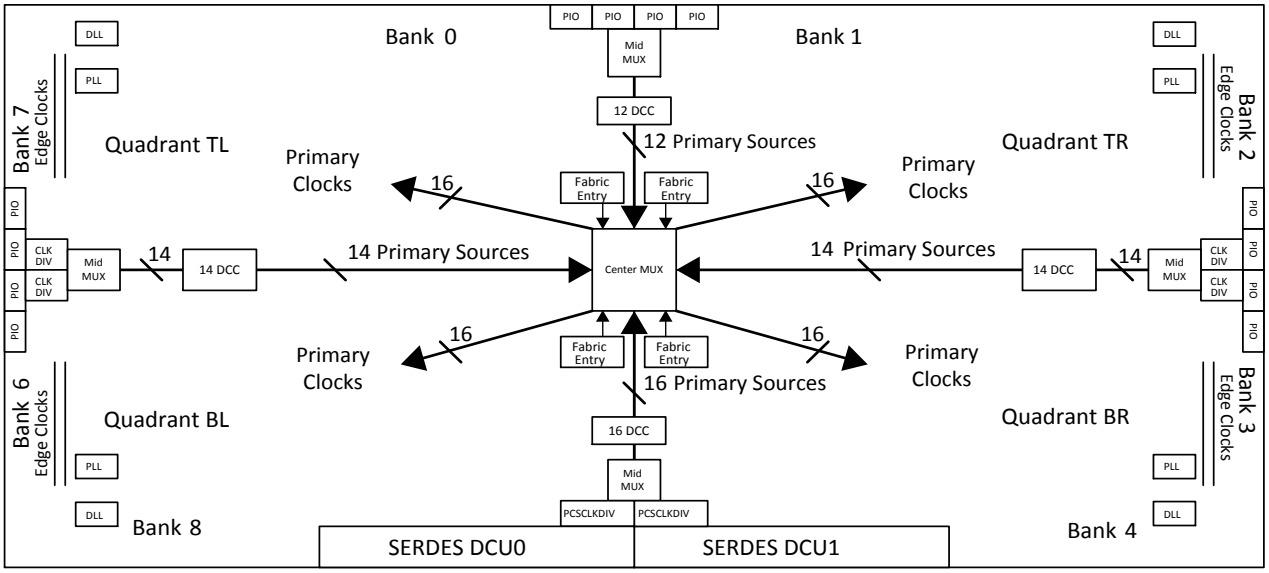


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

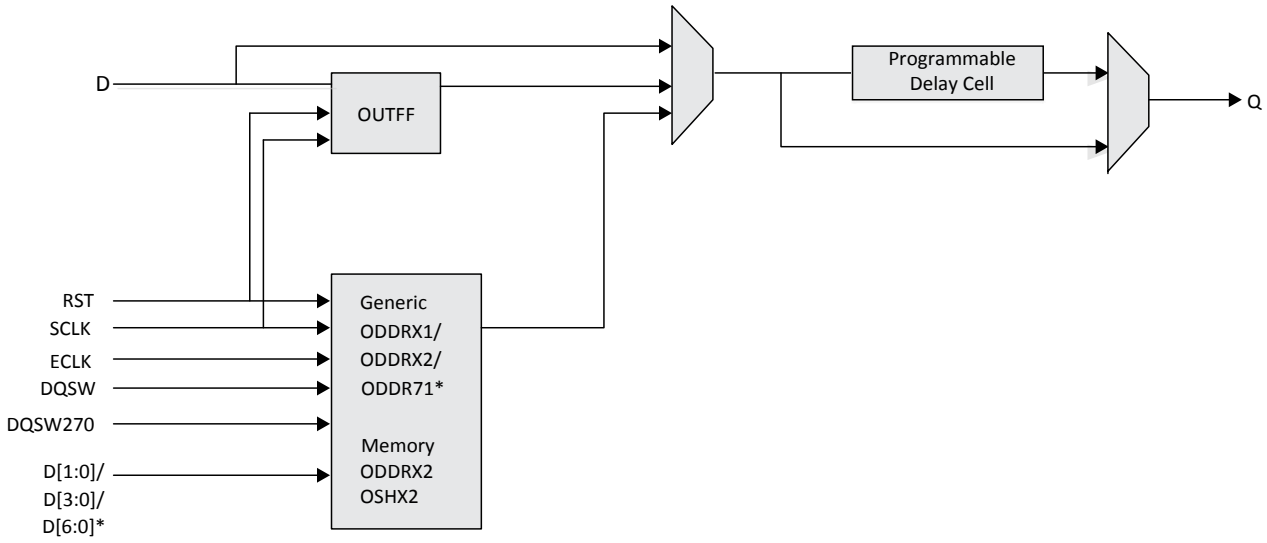
- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

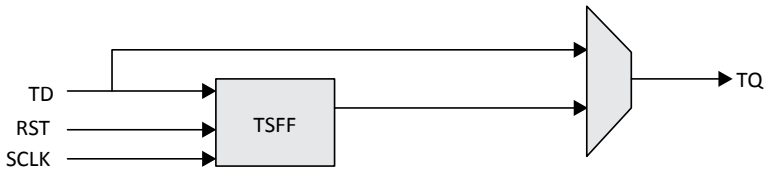


Figure 2.21. Tristate Register Block on Top Side

2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTL, LVPECL, and MIPI.

2.14.1. sysI/O Buffer Banks

ECP5/ECP5-5G devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank (Bank 8) is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O. For LFE5-85 devices, there is an additional I/O bank (Bank 4) that is not available in other device in the family.

In ECP5/ECP5-5G devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, the banks on the Left and Right sides of the device, have voltage reference input (shared I/O pin), VREF1 per bank, which allow it to be completely independent of each other. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5/ECP5-5G devices, single-ended output buffers and ratioed input buffers (LVTTL, and LVCMOS) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

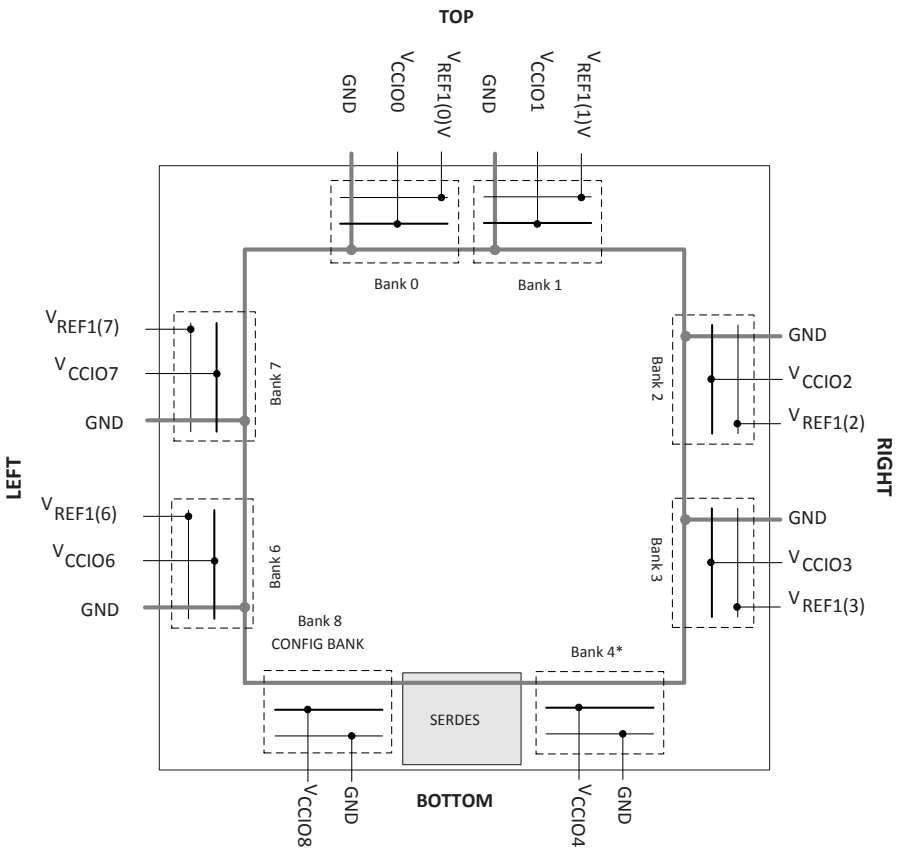


Figure 2.25. ECP5/ECP5-5G Device Family Banks

ECP5/ECP5-5G devices contain two types of sysI/O buffer pairs:

- Top (Bank 0 and Bank 1) and Bottom (Bank 8 and Bank 4) sysIO Buffer Pairs (Single-Ended Only)

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and be configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top and bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for used as emulated differential signaling.

  Bank 4 I/O only exists in the LFE5-85 device.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Diamond tool.

- Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers (both ratioed and referenced) and half of the sysI/O buffer pairs (PIOA/B pairs) also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5/ECP5-5G devices, see the list of technical documentation in Supplemental Information section on page 102.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The ECP5/ECP5-5G sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).

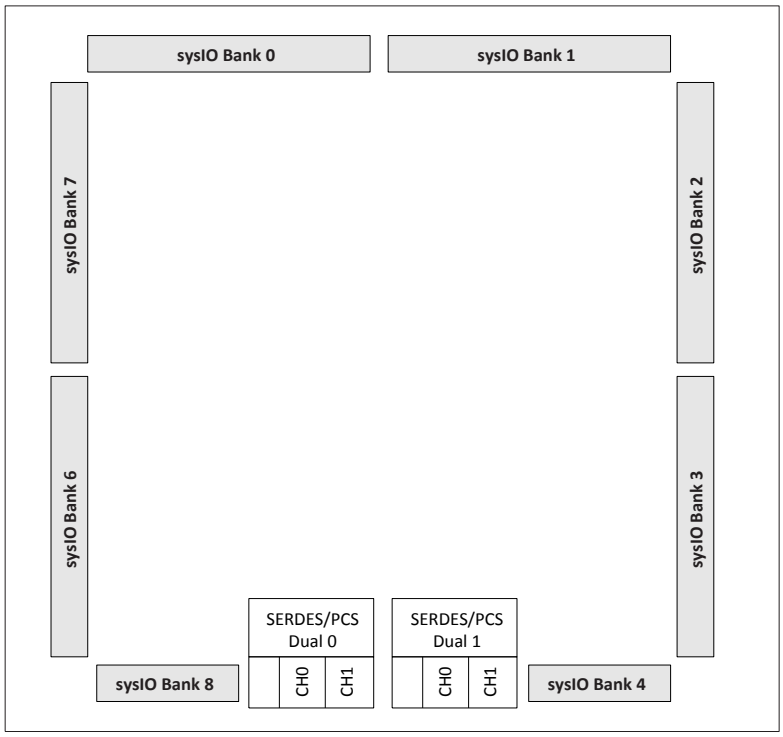


Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 [2]	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 [2]	x1	8b10b
SD-SDI (259M, 344M) [1]	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	—	—
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide (TN1184).

2.18.3. On-Chip Oscillator

Every ECP5/ECP5-5G device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) and ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.19. Density Shifting

The ECP5/ECP5-5G family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5/ECP5-5G Pin Migration Tables and Diamond software for specific restrictions and limitations.

3.11. SERDES Power Supply Requirements[1,2,3]

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I_{CCA-SB}	V_{CCA} Power Supply Current (Per Channel)	4	9.5	mA
$I_{CCHRX-SB}$[4]	V_{CCHRX}, Input Buffer Current (Per Channel)	—	0.1	mA
$I_{CCHTX-SB}$	V_{CCHTX}, Output Buffer Current (Per Channel)	—	0.9	mA
Operating (Data Rate = 3.125 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	43	54	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 2.5 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	40	50	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 1.25 Gb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	34	43	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	10	13	mA
Operating (Data Rate = 270 Mb/s)				
I_{CCA-OP}	V_{CCA} Power Supply Current (Per Channel)	28	38	mA
$I_{CCHRX-OP}$[5]	V_{CCHRX}, Input Buffer Current (Per Channel)	0.4	0.5	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current (Per Channel)	8	10	mA

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled
2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.
3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.
4. For $I_{CCHRX-SB}$, during Standby, input termination on Rx are disabled.
5. For $I_{CCHRX-OP}$, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

3.14.5. **BLVDS25**

The ECP5/ECP5-5G devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

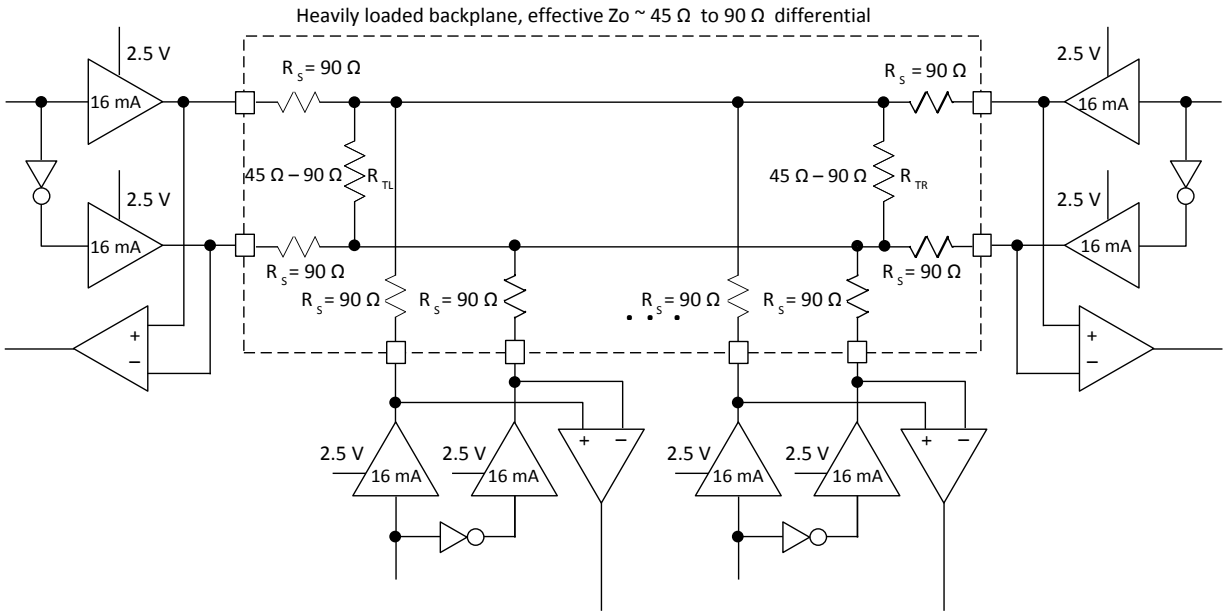


Figure 3.2. BLVDS25 Multi-point Output Example

Over recommended operating conditions.

Table 3.15. BLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo = 45 Ω	Zo = 90 Ω	
V_{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (±1%)	90.00	90.00	Ω
R_{TL}	Driver Parallel Resistor (±1%)	45.00	90.00	Ω
R_{TR}	Receiver Termination (±1%)	45.00	90.00	Ω
V_{OH}	Output High Voltage	1.38	1.48	V
V_{OL}	Output Low Voltage	1.12	1.02	V
V_{OD}	Output Differential Voltage	0.25	0.46	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	11.24	10.20	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.15. Typical Building Block Function Performance

Table 3.19. Pin-to-Pin Performance

Function	–8 Timing	Unit
Basic Functions		
16-Bit Decoder	5.06	ns
32-Bit Decoder	6.08	ns
64-Bit Decoder	5.06	ns
4:1 Mux	4.45	ns
8:1 Mux	4.63	ns
16:1 Mux	4.81	ns
32:1 Mux	4.85	ns

Notes:

1. I/Os are configured with LVCMOS25 with V_{CCIO}=2.5, 12 mA drive.
2. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
3. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss (without package)	—	—	–10	dB

Notes:
1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

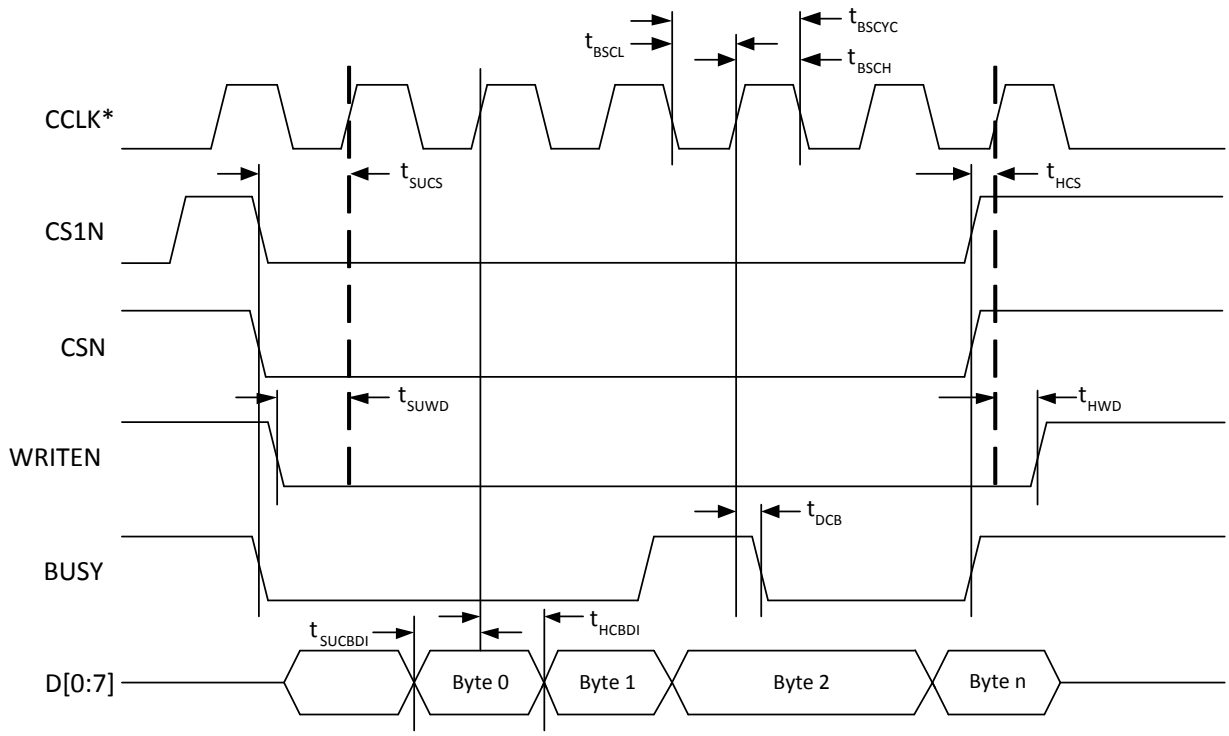
Notes:
1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

Table 3.31. PCIe (5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit[1]						
UI	Unit Interval	—	199.94	200	200.06	ps
$B_{WTX-PKG-PLL2}$	Tx PLL bandwidth corresponding to PKGTX-PLL2	—	5	—	16	MHz
$P_{KGTX-PLL2}$	Tx PLL Peaking	—	—	—	1	dB
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width	—		—	—	UI
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—		—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T_{TX-DJ}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T_{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
$T_{RF-MISMATCH}$	Tx rise/fall time mismatch	—	—	—		UI
$R_{LTX-DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX-CM-AC-PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—		mV, p-p
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Output peak voltage	—	—	—		mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—		ps



*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3.16. sysCONFIG Parallel Port Write Cycle

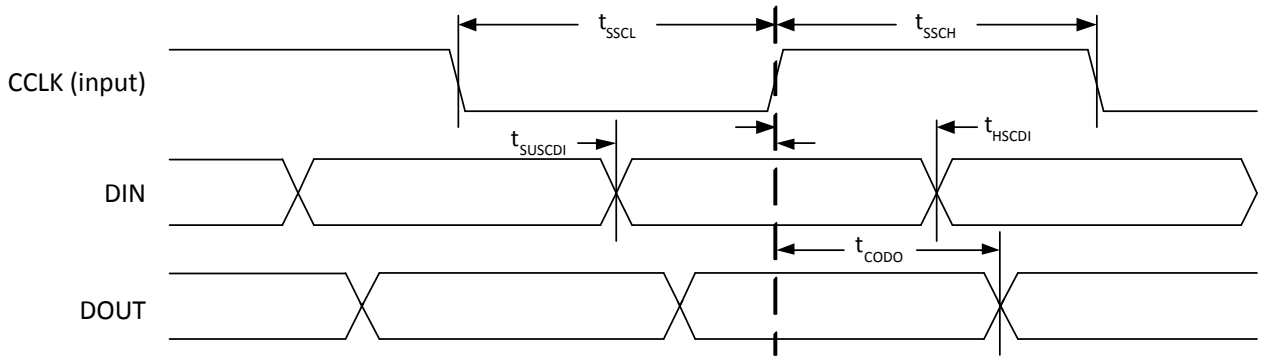


Figure 3.17. sysCONFIG Slave Serial Port Timing

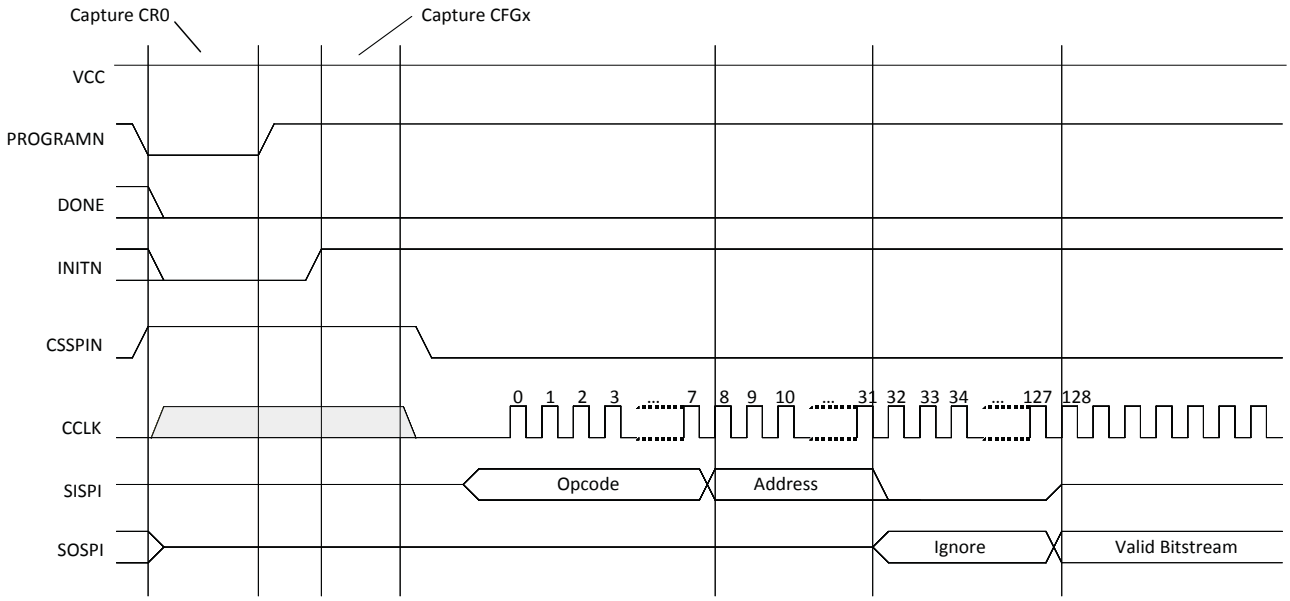


Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

(Continued)

Date	Version	Section	Change Summary
April 2017	1.7	All	Changed document number from DS1044 to FPGA-DS-02012.
		General Description	Updated Features section. Changed “1.1 V core power supply” to “1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G”.
		Architecture	Updated Overview section. Change “The ECP5/ECP5-5G devices use 1.1 V as their core voltage” to “The ECP5 devices use 1.1V, ECP5UM5G devices use 1.2V as their core voltage”
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions Added ECP5-5G on VCC to be 1.2V +/- 5% Added ECP5-5G on VCCA to be 1.2V +/- 3% Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) Changed “Core Power Supply Current” for ICC on LFE5UM5G devices Changed “SERDES Power Supply Current (Per Dual)” for ICCA on LFE5UM5G devices Updated Table 3.20. Register-to-Register Performance. Remove “(DDR/SDR)” from DSP Function Changed DSP functions to 225 MHz
		Pinout Information	Update Section 4.1 Signal Description. Revised Vcc Description to “Power supply pins for core logic. Dedicated pins. VCC = 1.1 V (ECP5), 1.2 V (ECP5UM5G)”
February 2016	1.6	All	Changed document status from Preliminary to Final.
		General Description	Updated Features section. Changed “24K to 84K LUTs” to “12K to 84K LUTs”. Added LFE5U-12 column to Table 1.1. ECP5 and ECP5-5G Family Selection Guide.
		DC and Switching Characteristics	Updated Power up Sequence section. Identified typical ICC current for specific devices in Table 3.8. ECP5/ECP5-5G Supply Current (Standby). Updated values in Table 3.9. ECP5. Updated values in Table 3.10. ECP5-5G. Added values to –8 Timing column of Table 3.19. Pin-to-Pin Performance. Added values to –8 Timing column of Table 3.20. Register-to-Register Performance. Changed LFE5-45 to All Devices in Table 3.22. ECP5/ECP5-5G External Switching Characteristics. Added table notes to Table 3.31. PCIe (5 Gb/s). Added table note to Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics.
		Pinout Information	Added LFE5U-12 column to the table in LFE5U section.
		Ordering Information	Updated LFE5U in ECP5/ECP5-5G Part Number Description section: added 12 F = 12K LUTs to Logic Capacity. Added LFE5U-12F information to Ordering Part Numbers section.

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Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section. • Deleted Serial RapidIO protocol under Embedded SERDES. • Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3. Mentioned transmit de-emphasis “pre- and post-cursors”.
		Architecture	Updated Overview section. • Revised description of PFU blocks. • Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section. • Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. • Deleted Serial RapidIO protocol. • Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section. • Deleted “130 MHz ±15% CMOS” oscillator. • Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA}.
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to t_{SKEW_PR} V_{CCA} and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.