Lattice Semiconductor Corporation - LFE5UM-85F-8BG756C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	365
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	756-FBGA
Supplier Device Package	756-CABGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-8bg756c

1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 84K LUTs
  - 197 to 365 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 3.744 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs

Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.

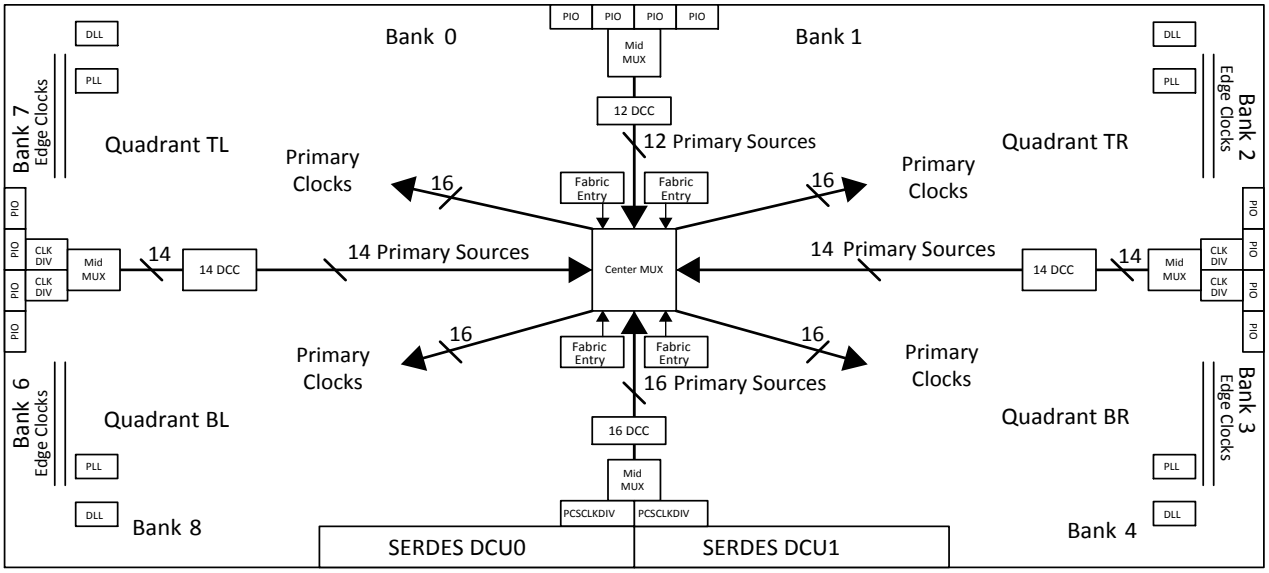

Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

- 5*5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5/ ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.

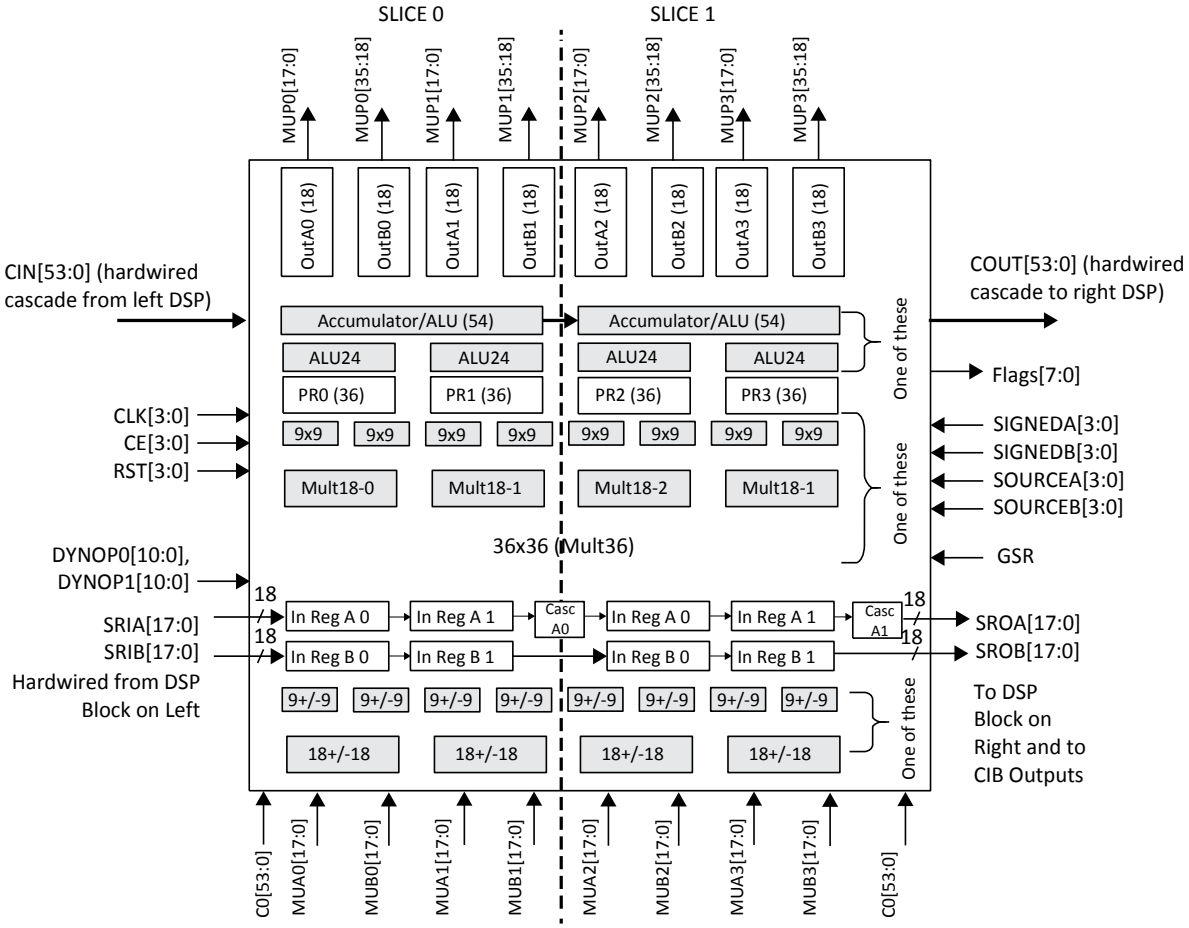

Figure 2.14. Simplified sysDSP Slice Block Diagram

2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTL, LVPECL, and MIPI.

2.14.1. sysI/O Buffer Banks

ECP5/ECP5-5G devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank (Bank 8) is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O. For LFE5-85 devices, there is an additional I/O bank (Bank 4) that is not available in other device in the family.

In ECP5/ECP5-5G devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, the banks on the Left and Right sides of the device, have voltage reference input (shared I/O pin), VREF1 per bank, which allow it to be completely independent of each other. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5/ECP5-5G devices, single-ended output buffers and ratioed input buffers (LVTTL, and LVCMOS) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

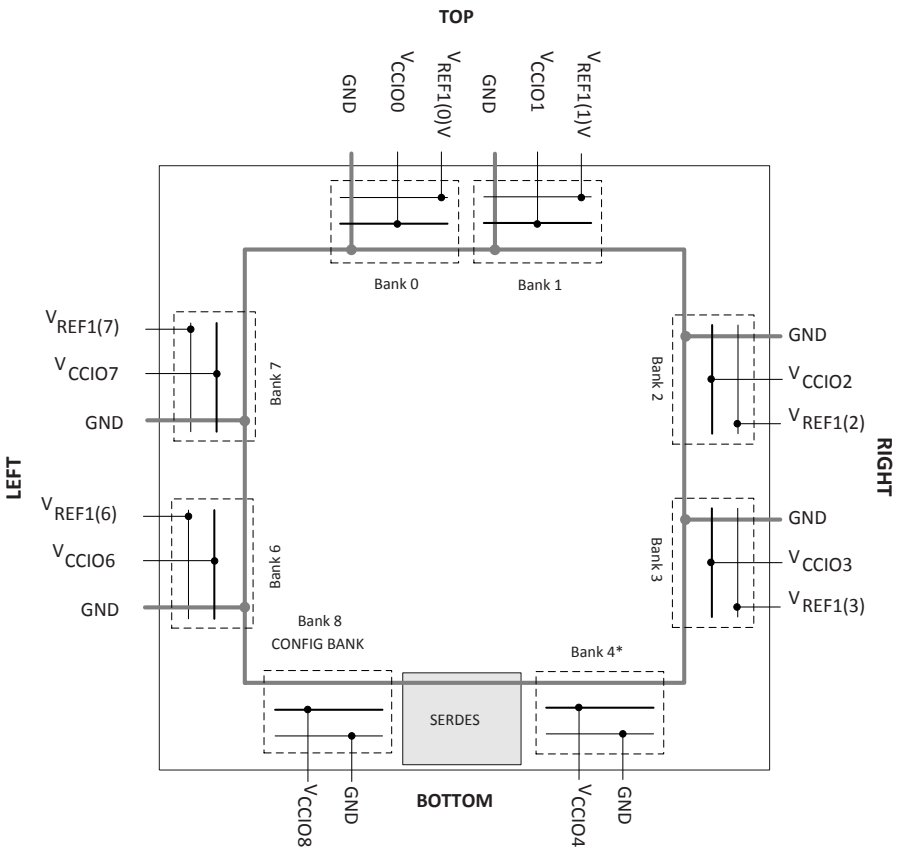

Figure 2.25. ECP5/ECP5-5G Device Family Banks

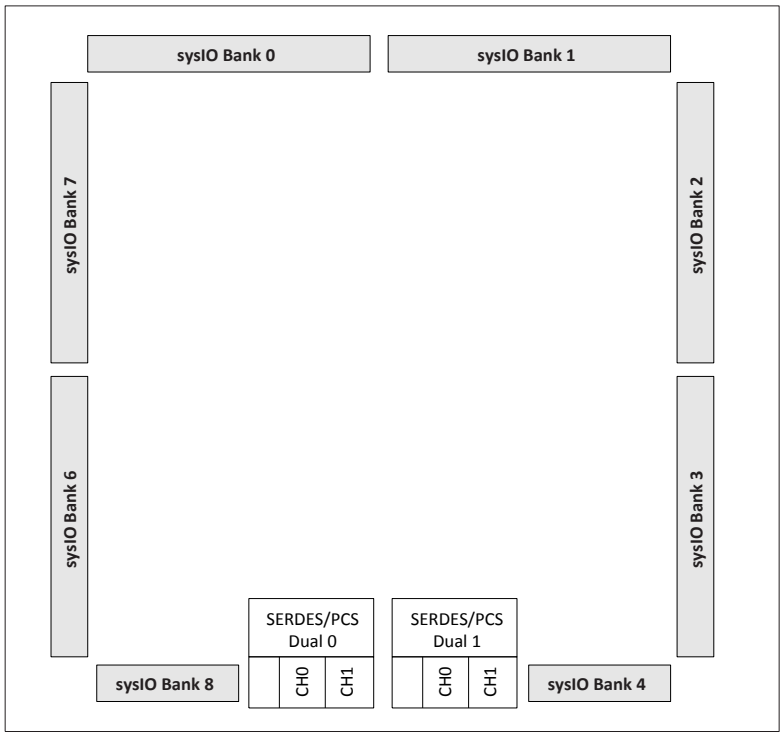

Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 [2]	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 [2]	x1	8b10b
SD-SDI (259M, 344M) [1]	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	—	—
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.

Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	—	2	2
756 caBGA	—	—	2

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).

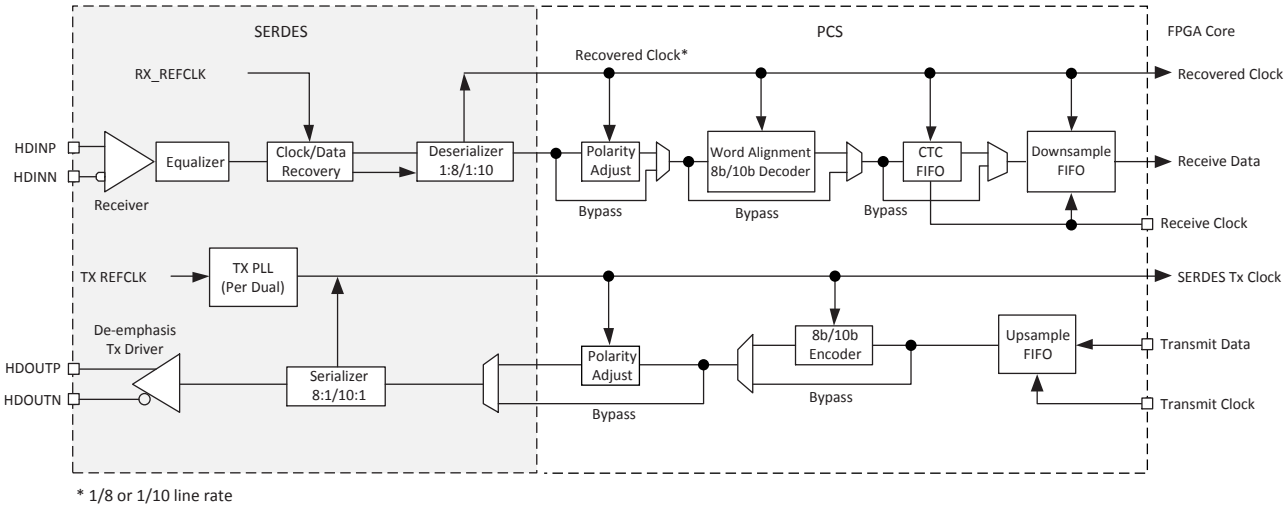

Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

3.7. Hot Socketing Requirements

Table 3.6. Hot Socketing Requirements

Description	Min	Typ	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA
Input current per HDIN pin when device power supply is off, inputs driven[1, 2]	—	—	15	mA
Current per HDIN pin when device power ramps up, input driven[3]	—	—	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up[4]	—	—	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, no external AC coupling.
2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.
3. Device power supplies are ramping up (V_{CCA} and V_{CCAUX}), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, internal AC coupling.
4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to V_{CCHTX} by the far end receiver termination of 50 Ω single ended.

3.8. ESD Performance

Refer to the ECP5 and ECP5-5G Product Family Qualification Summary for complete qualification data, including ESD performance.

3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4]	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	$V_{CCIO} < V_{IN} \le V_{IH(MAX)}$	—	—	100	µA
I_{PU}	I/O Active Pull-up Current, sustaining logic HIGH state	$0.7\ V_{CCIO} \le V_{IN} \le V_{CCIO}$	–30	—	—	µA
	I/O Active Pull-up Current, pulling down from logic HIGH state	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	—	—	–150	µA
I_{PD}	I/O Active Pull-down Current, sustaining logic LOW state	$0 \le V_{IN} \le V_{IL}$ (MAX)	30	—	—	µA
	I/O Active Pull-down Current, pulling up from logic LOW state	$0 \le V_{IN} \le V_{CCIO}$	—	—	150	µA
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to $V_{IH(MAX)}$	—	5	8	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to $V_{IH(MAX)}$	—	5	7	pf
V_{HYST}	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V	—	300	—	mV
		V_{CCIO} = 2.5 V	—	250	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as V_{REF}, maximum leakage= 25 µA.

3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

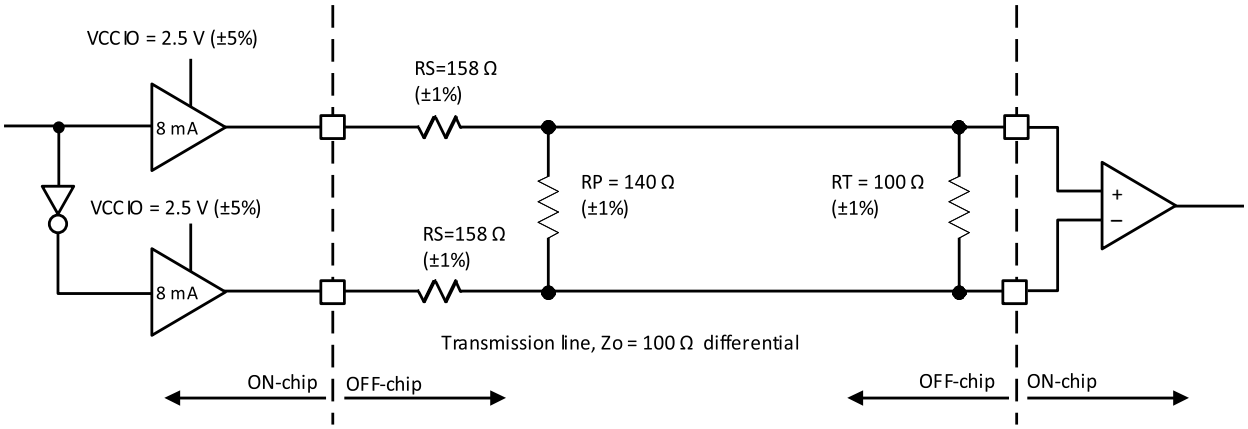

Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (±1%)	158	Ω
R_P	Driver Parallel Resistor (±1%)	140	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

3.14.6. **LVPECL33**

The ECP5/ECP5-5G devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.3 is one possible solution for point-to-point signals.

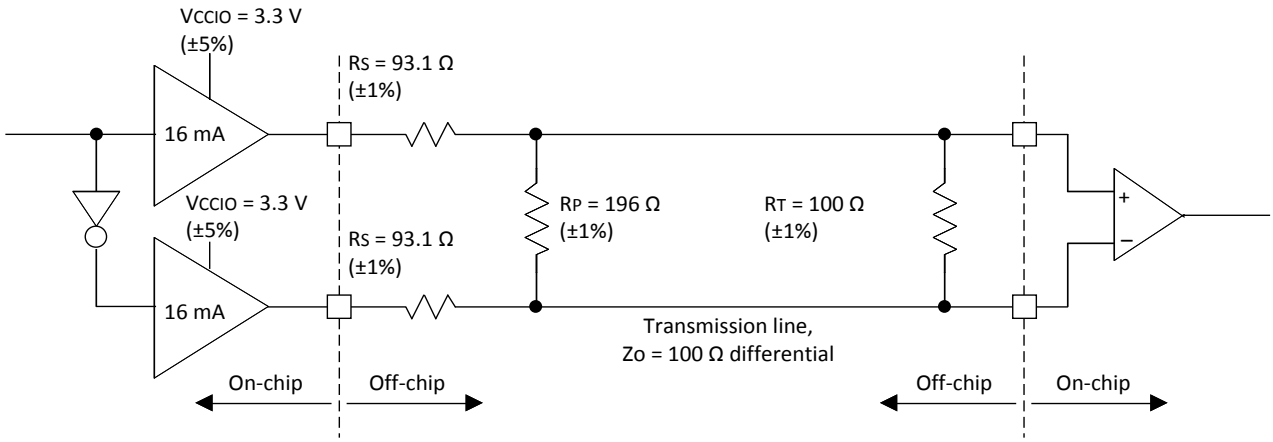

Figure 3.3. Differential LVPECL33

Over recommended operating conditions.

Table 3.16. LVPECL33 DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (±1%)	93	Ω
R_P	Driver Parallel Resistor (±1%)	196	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	0	—	0	—	ns
Generic DDR Input									
Generic DDRX1 Inputs With Clock and Data Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{SU\_GDDRX1\_centered}$	Data Setup Before CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$t_{HD\_GDDRX1\_centered}$	Data Hold After CLK Input	All Devices	0.52	—	0.52	—	0.52	—	ns
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs With Clock and Data Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.7									
$t_{SU\_GDDRX1\_aligned}$	Data Setup from CLK Input	All Devices	—	–0.55	—	–0.55	—	–0.55	ns + 1/2 UI
$t_{HD\_GDDRX1\_aligned}$	Data Hold from CLK Input	All Devices	0.55	—	0.55	—	0.55	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Inputs With Clock and Data Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.6									
$t_{SU\_GDDRX2\_centered}$	Data Setup before CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$t_{HD\_GDDRX2\_centered}$	Data Hold after CLK Input	All Devices	0.321	—	0.403	—	0.471	—	ns
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Inputs With Clock and Data Aligned at Pin (GDDRX2_RX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.7									
$t_{SU\_GDDRX2\_aligned}$	Data Setup from CLK Input	All Devices	—	–0.344	—	–0.42	—	-0.495	ns + 1/2 UI
$t_{HD\_GDDRX2\_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	—	0.495	—	ns + 1/2 UI
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Inputs With Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) Using PLL Clock Input, Left and Right sides Only Figure 3.11									
$t_{SU\_LVDS71\_i}$	Data Setup from CLK Input (bit i)	All Devices	—	–0.271	—	–0.39	—	–0.41	ns+(1/2+i) * UI
$t_{HD\_LVDS71\_i}$	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	—	0.41	—	ns+(1/2+i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
Generic DDR Output									
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDRX1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6									
$t_{DVB\_GDDRX1\_centered}$	Data Output Valid before CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$t_{DVA\_GDDRX1\_centered}$	Data Output Valid after CLK Output	All Devices	–0.67	—	–0.67	—	–0.67	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9									
$t_{DIB\_GDDRX1\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.3	—	–0.3	—	–0.3	—	ns
$t_{DIA\_GDDRX1\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.3	—	0.3	—	0.3	ns
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	—	500	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8									
$t_{DVB\_GDDRX2\_centered}$	Data Output Valid Before CLK Output	All Devices	–0.442	—	–0.56	—	–0.676	—	ns + 1/2 UI
$t_{DVA\_GDDRX2\_centered}$	Data Output Valid After CLK Output	All Devices	—	0.442	—	0.56	—	0.676	ns + 1/2 UI
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9									
$t_{DIB\_GDDRX2\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns
$t_{DIA\_GDDRX2\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	800	—	700	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDRX71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12									
$t_{DIB\_LVDS71\_i}$	Data Output Invalid before CLK Output	All Devices	–0.16	—	–0.18	—	–0.2	—	ns + (i) * UI
$t_{DIA\_LVDS71\_i}$	Data Output Invalid after CLK Output	All Devices	—	0.16	—	0.18	—	0.2	ns + (i) * UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	756	—	620	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	378	—	310	—	262.5	MHz
Memory Interface									
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)									
t_{DVBDQ_DDR2} t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	–0.26	—	–0.317	—	–0.374	ns + 1/2 UI
t_{DVADQ_DDR2} t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.26	—	0.317	—	0.374	—	ns + 1/2 UI

Table 3.22. ECP5/ECP5-5G External Switching Characteristics *(Continued)*

Parameter	Description	Device	–8		–7		–6		Unit
			Min	Max	Min	Max	Min	Max	
f_{DATA_DDR2} f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	800	—	700	—	624	Mb/s
f_{MAX_DDR2} f_{MAX_DDR3} f_{MAX_DDR3L} f_{MAX_LPDDR2} f_{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS)									
t_{DQVBS_DDR2} t_{DQVBS_DDR3} t_{DQVBS_DDR3L} t_{DQVBS_LPDDR2} t_{DQVBS_LPDDR3}	Data Output Valid before DQS Output	All Devices	—	–0.25	—	–0.25	—	-0.25	UI
t_{DQVAS_DDR2} t_{DQVAS_DDR3} t_{DQVAS_DDR3L} t_{DQVAS_LPDDR2} t_{DQVAS_LPDDR3}	Data Output Valid after DQS Output	All Devices	0.25	—	0.25	—	0.25	—	UI
f_{DATA_DDR2} f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	800	—	700	—	624	Mb/s
f_{MAX_DDR2} f_{MAX_DDR3} f_{MAX_DDR3L} f_{MAX_LPDDR2} f_{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	400	—	350	—	312	MHz

Notes:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.
2. General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load.
   Generic DDR timing are numbers based on LVDS I/O.
   DDR2 timing numbers are based on SSTL18.
   DDR3 timing numbers are based on SSTL15.
   LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
3. Uses LVDS I/O standard for measurements.
4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
5. All numbers are generated with the Diamond software.

3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

Table 3.31. PCIe (5 Gb/s)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit[1]						
UI	Unit Interval	—	199.94	200	200.06	ps
$B_{WTX-PKG-PLL2}$	Tx PLL bandwidth corresponding to PKGTX-PLL2	—	5	—	16	MHz
$P_{KGTX-PLL2}$	Tx PLL Peaking	—	—	—	1	dB
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width	—		—	—	UI
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—		—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T_{TX-DJ}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T_{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
$T_{RF-MISMATCH}$	Tx rise/fall time mismatch	—	—	—		UI
$R_{LTX-DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX-CM-AC-PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—		mV, p-p
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Output peak voltage	—	—	—		mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—		ps

3.31. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 3.42. ECP5/ECP5-5G sysCONFIG Port Timing Specifications

Symbol	Parameter		Min	Max	Unit
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC}, V_{CCAUX} or V_{CCIO8} (whichever is the last) to the rising edge of INITN	—	—	33	ms
t_{VMC}	Time from t_{ICFG} to the valid Master CCLK	—	—	5	us
t_{CZ}	CCLK from Active to High-Z	—	—	300	ns
Master CCLK					
f_{MCLK}	Frequency	All selected frequencies	–20	20	%
$t_{MCLK-DC}$	Duty Cycle	All selected frequencies	40	60	%
All Configuration Modes					
t_{PRGM}	PROGRAMN LOW pulse accepted	—	110	—	ns
t_{PRGMRJ}	PROGRAMN LOW pulse rejected	—	—	50	ns
t_{INITL}	INITN LOW time	—	—	55	ns
t_{DPPINT}	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	150	ns
Slave SPI					
f_{CCLK}	CCLK input clock frequency	—	—	60	MHz
t_{CCLKH}	CCLK input clock pulsewidth HIGH	—	6	—	ns
t_{CCLKL}	CCLK input clock pulsewidth LOW	—	6	—	ns
t_{STSU}	CCLK setup time	—	1	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{STCO}	CCLK falling edge to valid output	—	—	10	ns
t_{STOZ}	CCLK falling edge to valid disable	—	—	10	ns
t_{STOV}	CCLK falling edge to valid enable	—	—	10	ns
t_{SCS}	Chip Select HIGH time	—	25	—	ns
t_{SCSS}	Chip Select setup time	—	3	—	ns
t_{SCSH}	Chip Select hold time	—	3	—	ns
Master SPI					
f_{CCLK}	Max selected CCLK output frequency	—	—	62	MHz
t_{CCLKH}	CCLK output clock pulse width HIGH	—	3.5	—	ns
t_{CCLKL}	CCLK output clock pulse width LOW	—	3.5	—	ns
t_{STSU}	CCLK setup time	—	5	—	ns
t_{STH}	CCLK hold time	—	1	—	ns
t_{CSSPI}	INITN HIGH to Chip Select LOW	—	100	200	ns
t_{CFGX}	INITN HIGH to first CCLK edge	—	—	150	ns
Slave Serial					
f_{CCLK}	CCLK input clock frequency	—	—	66	MHz
t_{SSCH}	CCLK input clock pulse width HIGH	—	5	—	ns
t_{SSCL}	CCLK input clock pulse width LOW	—	5	—	ns
t_{SUSCDI}	CCLK setup time	—	0.5	—	ns
t_{HSCDI}	CCLK hold time	—	1.5	—	ns

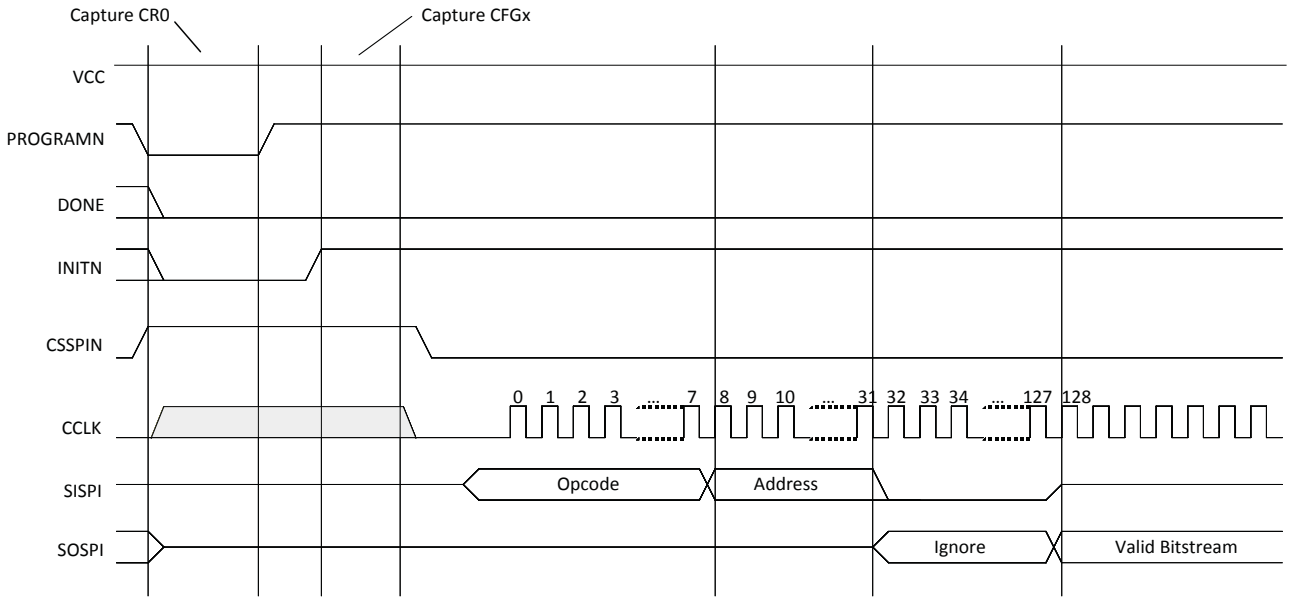

Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device Only		
P[L/R] [n–6]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n–3]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n]	A	DQS (P)
	B	DQS (N)
	C	DQ
	D	DQ
P[L/R] [n+3]	A	DQ
	B	DQ
	C	DQ
	D	DQ

Note: "n" is a row PIC number.

4.3. Pin Information Summary

4.3.1. LFE5UM/LFE5UM5G

Pin Information Summary		LFE5UM/ LFE5UM5G-25		LFE5UM/LFE5UM5G-45			LFE5UM/LFE5UM5G-85			
Pin Type		285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA
General Purpose Inputs/Outputs per Bank	Bank 0	6	24	6	27	32	6	27	32	56
	Bank 1	6	32	6	33	40	6	33	40	48
	Bank 2	21	32	21	32	32	21	34	32	48
	Bank 3	28	32	28	33	48	28	33	48	64
	Bank 4	0	0	0	0	0	0	0	14	24
	Bank 6	26	32	26	33	48	26	33	48	64
	Bank 7	18	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13
Total Single-Ended User I/O		118	197	118	203	245	118	205	259	365
VCC		13	20	13	20	24	13	20	24	36
VCCAUX (Core)		3	4	3	4	9	3	4	9	8
VCCIO	Bank 0	1	2	1	2	3	1	2	3	4
	Bank 1	1	2	1	2	3	1	2	3	4
	Bank 2	2	3	2	3	4	2	3	4	4
	Bank 3	2	3	2	3	3	2	3	3	4
	Bank 4	0	0	0	0	0	0	0	2	2
	Bank 6	2	3	2	3	4	2	3	4	4
	Bank 7	2	3	2	3	3	2	3	3	4
	Bank 8	2	2	2	2	2	2	2	2	2

Pin Information Summary		LFE5UM/ LFE5UM5G-25		LFE5UM/LFE5UM5G-45			LFE5UM/LFE5UM5G-85			
Pin Type		285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA
TAP		4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated Pins		7	7	7	7	7	7	7	7	7
GND		83	59	83	59	113	83	59	113	166
NC		1	8	1	2	33	1	0	17	29
Reserved		0	2	0	2	4	0	2	4	4
SERDES		14	28	14	28	28	14	28	28	28
VCCA (SERDES)	VCCA0	2	2	2	2	6	2	2	6	8
	VCCA1	0	2	0	2	6	0	2	6	9
VCCAUX (SERDES)	VCCAUXA0	2	2	2	2	2	2	2	2	2
	VCCAUXA1	0	2	0	2	2	0	2	2	2
GNDA (SERDES)		26	26	26	26	49	26	26	49	60
Total Balls		285	381	285	381	554	285	381	554	756
High Speed Differential Input / Output Pairs	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	10/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8	24/12
	Bank 3	14/7	16/8	14/7	16/8	24/12	14/7	16/8	24/12	32/16
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	13/6	16/8	13/6	16/8	24/12	13/6	16/8	24/12	32/16
	Bank 7	8/6	16/8	8/6	16/8	16/8	8/6	16/8	16/8	24/12
	Bank 8	0	0	0	0	0	0	0	0	0
Total High Speed Differential I/O Pairs		45/2	64/32	45/27	64/3	80/40	45/27	65/3	80/40	112/5
DQS Groups (> 11 pins in group)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	1	2	1	2	2	1	2	2	3
	Bank 3	2	2	2	2	3	2	2	3	4
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	2	2	2	2	3	2	2	3	4
	Bank 7	1	2	1	2	2	1	2	2	3
	Bank 8	0	0	0	0	0	0	0	0	0
Total DQS Groups		6	8	6	8	10	6	8	10	14

(Continued)

Date	Version	Section	Change Summary
April 2017	1.7	All	Changed document number from DS1044 to FPGA-DS-02012.
		General Description	Updated Features section. Changed “1.1 V core power supply” to “1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G”.
		Architecture	Updated Overview section. Change “The ECP5/ECP5-5G devices use 1.1 V as their core voltage” to “The ECP5 devices use 1.1V, ECP5UM5G devices use 1.2V as their core voltage”
		DC and Switching Characteristics	Updated Table 3.2. Recommended Operating Conditions Added ECP5-5G on VCC to be 1.2V +/- 5% Added ECP5-5G on VCCA to be 1.2V +/- 3% Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby) Changed “Core Power Supply Current” for ICC on LFE5UM5G devices Changed “SERDES Power Supply Current (Per Dual)” for ICCA on LFE5UM5G devices Updated Table 3.20. Register-to-Register Performance. Remove “(DDR/SDR)” from DSP Function Changed DSP functions to 225 MHz
		Pinout Information	Update Section 4.1 Signal Description. Revised Vcc Description to “Power supply pins for core logic. Dedicated pins. VCC = 1.1 V (ECP5), 1.2 V (ECP5UM5G)”
February 2016	1.6	All	Changed document status from Preliminary to Final.
		General Description	Updated Features section. Changed “24K to 84K LUTs” to “12K to 84K LUTs”. Added LFE5U-12 column to Table 1.1. ECP5 and ECP5-5G Family Selection Guide.
		DC and Switching Characteristics	Updated Power up Sequence section. Identified typical ICC current for specific devices in Table 3.8. ECP5/ECP5-5G Supply Current (Standby). Updated values in Table 3.9. ECP5. Updated values in Table 3.10. ECP5-5G. Added values to –8 Timing column of Table 3.19. Pin-to-Pin Performance. Added values to –8 Timing column of Table 3.20. Register-to-Register Performance. Changed LFE5-45 to All Devices in Table 3.22. ECP5/ECP5-5G External Switching Characteristics. Added table notes to Table 3.31. PCIe (5 Gb/s). Added table note to Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics.
		Pinout Information	Added LFE5U-12 column to the table in LFE5U section.
		Ordering Information	Updated LFE5U in ECP5/ECP5-5G Part Number Description section: added 12 F = 12K LUTs to Logic Capacity. Added LFE5U-12F information to Ordering Part Numbers section.

7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com