# E. Lattice Semiconductor Corporation - <u>LFE5UM-85F-8BG756I Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	365
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	756-FBGA
Supplier Device Package	756-CABGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um-85f-8bg756i

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- Four DLLs and four PLLs in LFE5-45 and LFE5-85; two DLLs and two PLLs in LFE5-25 and LFE5-12
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O<sup>™</sup> Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 18/15 I, II
  - HSUL12
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

- subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
  - Shared bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR<sup>™</sup> I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
  - Soft Error Detect Embedded hard macro
  - Soft Error Correction Without stopping user operation
  - Soft Error Injection Emulate SEU event to debug system error handling
- System Level Support
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - On-chip oscillator for initialization and general use
  - 1.1 V core power supply for ECP5, 1.2 V core power supply for ECP5UM5G

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U- 12	LFE5U- 25	LFE5U- 45	LFE5U- 85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages (SERDES Channels /	IO Count)						
256 caBGA (14 x 14 mm <sup>2</sup> , 0.8 mm)	-	—	-	0/197	0/197	0/197	-
285 csfBGA (10 x 10 mm <sup>2</sup> , 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm², 0.8 mm)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm <sup>2</sup> , 0.8 mm)	_	4/245	4/259	_	_	0/245	0/259
756 caBGA (27 x 27 mm², 0.8 mm)	_	_	4/365	_	_	_	0/365

#### Table 1.1. ECP5 and ECP5-5G Family Selection Guide

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Figure 2.2. PFU Diagram

#### 2.2.1. Slice

Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Clico	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
Slice	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Table 2.1. Resources and Modes Available per Slice

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals, 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are five outputs, four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/ PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7 and LUT8. Table 2.2 and Figure 2.3 list the signals associated with all the slices. Figure 2.4 on page 16 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7 and LUT8.





Figure 2.4. Conned	tivity Supporting L	LUT5, LUT6,	LUT7, and LUT8
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Table 2.2	. Slice	Signal	Descri	ptions
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Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in <sup>1</sup>
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8 <sup>2</sup>
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8 <sup>2</sup>
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output <sup>1</sup>

Notes:

2. Requires two adjacent PFUs.

<sup>1.</sup> See Figure 2.3 on page 15 for connection details.



### 2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.



Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

## 2.9. sysDSP<sup>™</sup> Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

## 2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.



In Figure 2.15, note that A\_ALU, B\_ALU and C\_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

#### Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	Ι

\*Note: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

## 2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.





Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13.	LFE5UM	/LFE5UM5G S	ERDES Standa	ard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0	2500	x1, x2, x4	8b10b
2.02	5000 <sup>2</sup>	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SCMI	1250	x1	8b10b
SGIVIII	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 <sup>2</sup>	x1	8b10b
SD-SDI (259M, 344M) <sup>1</sup>	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	_	_
JESD204A/B	3125	x1	8b/10b

#### Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.

2. For ECP5-5G family devices only.



## 2.18. Device Configuration

All ECP5/ECP5-5G devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are 11 dedicated pins for TAP and sysConfig supports (TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN and CCLK). The remaining sysCONFIG pins are used as dual function pins. Refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5/ECP5-5G device:

- JTAG
- Standard Serial Peripheral Interface (SPI) Interface to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port SPCM mode
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Slave Serial model (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5/ECP5-5G devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

#### 2.18.1. Enhanced Configuration Options

ECP5/ECP5-5G devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O and dual-boot and multi-boot image support.

#### TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to Minimizing System Interruption During Configuration Using TransFR Technology (TN1087) for details.

#### **Dual-Boot and Multi-Boot Image Support**

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the ECP5/ECP5-5G devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5/ECP5-5G device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

## 2.18.2. Single Event Upset (SEU) Support

ECP5/ECP5-5G devices support SEU mitigation with three supporting functions:

- SED Soft Error Detect
- SEC Soft Error Correction
- SEI Soft Error Injection

ECP5/ECP5-5G devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5/ECP5-5G device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

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## 3.10. Supply Current (Standby)

Over recommended operating conditions.

#### Table 3.8. ECP5/ECP5-5G Supply Current (Standby)

Symbol	Parameter	Device	Typical	Unit
		LFE5U-12F/ LFE5U-25F/ LFE5UM-25F	77	mA
		LFE5UM5G-25F	77	mA
Icc Iccaux	Come Devices Commission Commission	LFE5U-45F/ LFE5UM-45F	116	mA
ICC	Core Power Supply Current	LFE5UM5G-45F	116	mA
		LFE5U-85F/ LFE5UM-85F	212	mA
		LFE5UM5G-85F	212	mA
Iccaux		LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	16	mA
	Auxiliary Power Supply Current	LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	17	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	26	mA
		LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	0.5	mA
I <sub>CCIO</sub>	Bank Power Supply Current (Per Bank)	LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	0.5	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	0.5	mA
		LFE5UM-25F	11	mA
		LFE5UM5G-25F	12	mA
	SERDES Power Supply Current (Per	LFE5UM-45F	9.5	mA
I <sub>CCA</sub>	Dual)	LFE5UM5G-45F	11	mA
		LFE5UM-85F	9.5	mA
		LFE5UM5G-85F	11	mA

Notes:

- For further information on supply current, see the list of technical documentation in Supplemental Information section on page 102.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V<sub>CCIO</sub> or GND.

• Frequency 0 Hz.

- Pattern represents a "blank" configuration data file.
- T<sub>J</sub> = 85 °C, power supplies at nominal voltage.
- To determine the ECP5/ECP5-5G peak start-up current, use the Power Calculator tool in the Lattice Diamond Design Software.



## 3.11. SERDES Power Supply Requirements<sup>1,2,3</sup>

Over recommended operating conditions.

#### Table 3.9. ECP5UM

Symbol	Description	Тур	Max	Unit		
Standby (Power	Down)					
I <sub>CCA-SB</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	4	9.5	mA		
I <sub>CCHRX-SB</sub> <sup>4</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	—	0.1	mA		
I <sub>CCHTX-SB</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	—	0.9	mA		
<b>Operating</b> (Data	Rate = 3.125 Gb/s)					
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	43	54	mA		
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA		
І <sub>сснтх-ор</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA		
Operating (Data Rate = 2.5 Gb/s)						
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	40	50	mA		
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA		
І <sub>сснтх-ор</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA		
Operating (Data	Rate = 1.25 Gb/s)					
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	34	43	mA		
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA		
I <sub>CCHTX-OP</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	10	13	mA		
<b>Operating</b> (Data	Rate = 270 Mb/s)					
I <sub>CCA-OP</sub>	V <sub>CCA</sub> Power Supply Current (Per Channel)	28	38	mA		
I <sub>CCHRX-OP</sub> <sup>5</sup>	V <sub>CCHRX</sub> , Input Buffer Current (Per Channel)	0.4	0.5	mA		
I <sub>ССНТХ-ОР</sub>	V <sub>CCHTX</sub> , Output Buffer Current (Per Channel)	8	10	mA		

Notes:

1. Rx Equalization enabled, Tx De-emphasis (pre-cursor and post-cursor) disabled

2. Per Channel current is calculated with both channels on in a Dual, and divide current by two. If only one channel is on, current will be higher.

3. To calculate with Tx De-emphasis enabled, use the Diamond Power Calculator tool.

4. For ICCHRX-SB, during Standby, input termination on Rx are disabled.

5. For ICCHRX-OP, during operational, the max specified when external AC coupling is used. If externally DC coupled, the power is based on current pulled down by external driver when the input is driven to LOW.

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## 3.13. sysI/O Single-Ended DC Electrical Characteristics

Input/Output	VIL		VIH		V <sub>oL</sub> Max	V <sub>он</sub> Min	L 1/m A)	1 1 (m A)
Standard	Min (V)	Max (V)	Min (V)	Max (V)	(V)	(V)	1 <sub>0L</sub> - (mA)	<sub>ЮН</sub> - (тпА)
LVCMOS33	-0.3	0.8	2.0	3.465	0.4	V <sub>CCIO</sub> – 0.4	16, 12, 8, 4	-16, -12, -8, -4
LVCMOS25	-0.3	0.7	1.7	3.465	0.4	$V_{CCIO} - 0.4$	12, 8, 4	-12, -8, -4
LVCMOS18	-0.3	0.35 V <sub>CCIO</sub>	0.65 V <sub>CCIO</sub>	3.465	0.4	V <sub>CCIO</sub> – 0.4	12, 8, 4	-12, -8, -4
LVCMOS15	-0.3	0.35 V <sub>CCIO</sub>	0.65 V <sub>CCIO</sub>	3.465	0.4	V <sub>CCIO</sub> – 0.4	8, 4	-8, -4
LVCMOS12	-0.3	0.35 V <sub>CCIO</sub>	0.65 V <sub>CCIO</sub>	3.465	0.4	V <sub>CCIO</sub> – 0.4	8, 4	-8, -4
LVTTL33	-0.3	0.8	2.0	3.465	0.4	V <sub>CCIO</sub> – 0.4	16, 12, 8, 4	-16, -12, -8, -4
SSTL18_I (DDR2 Memory)	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	3.465	0.4	V <sub>CCIO</sub> – 0.4	6.7	-6.7
SSTL18_II	-0.3	V <sub>REF</sub> -	V <sub>REF</sub> + 0.125	3.465	0.28	V <sub>CCIO</sub> -0.28	13.4	-13.4
SSTL15 _I (DDR3 Memory)	-0.3	$V_{REF} - 0.1$	V <sub>REF</sub> + 0.1	3.465	0.31	V <sub>CCIO</sub> -0.31	7.5	-7.5
SSTL15_II (DDR3 Memory)	-0.3	$V_{REF} - 0.1$	V <sub>REF</sub> + 0.1	3.465	0.31	V <sub>CCIO</sub> -0.31	8.8	-8.8
SSTL135_I (DDR3L Memory)	-0.3	V <sub>REF</sub> -0.09	V <sub>REF</sub> + 0.09	3.465	0.27	V <sub>CCIO</sub> – 0.27	7	-7
SSTL135_II (DDR3L Memory)	-0.3	V <sub>REF</sub> -0.09	V <sub>REF</sub> + 0.09	3.465	0.27	V <sub>CCIO</sub> – 0.27	8	-8
MIPI D-PHY (LP) <sup>3</sup>	-0.3	0.55	0.88	3.465	—	_	—	—
HSUL12 (LPDDR2/3 Memory)	-0.3	V <sub>REF</sub> -0.1	V <sub>REF</sub> + 0.1	3.465	0.3	V <sub>CCIO</sub> – 0.3	4	-4

#### Table 3.12. Single-Ended DC Characteristics

Notes:

1. For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O (All I/Os used in the same V<sub>CCIO</sub>).

2. Not all IO types are supported in all banks. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.

3. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V<sub>IH</sub> and V<sub>IL</sub>. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V<sub>IH</sub>/V<sub>IL</sub> spec on LVCOM12.





## 3.14.7. MLVDS25

The ECP5/ECP5-5G devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.



Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Parameter	Description	Тур	l la it	
	Description	Zo=50 Ω	Zo=70 Ω	Onit
V <sub>CCIO</sub>	Output Driver Supply (±5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
Rs	Driver Series Resistor (±1%)	35.00	35.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
R <sub>TR</sub>	Receiver Termination (±1%)	50.00	70.00	Ω
V <sub>OH</sub>	Output High Voltage	1.52	1.60	V
V <sub>OL</sub>	Output Low Voltage	0.98	0.90	V
V <sub>OD</sub>	Output Differential Voltage	0.54	0.70	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	21.74	20.00	mA

#### Table 3.17. MLVDS25 DC Conditions

**Note**: For input buffer, see LVDS Table 3.13 on page 55.

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## 3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

#### Table 3.18. Input to SLVS

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.



Figure 3.5. SLVS Interface

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Deveryoten	Description	Davias	-8		-	7	-	11	
Parameter	Description	Device	Min	Мах	Min	Max	Min	Max	Unit
fdata_ddr2 fdata_ddr3 fdata_ddr3l fdata_ddr3l fdata_lpddr2 fdata_lpddr3	DDR Memory Data Rate	All Devices	_	800	_	700	_	624	Mb/s
fmax_ddr2 fmax_ddr3 fmax_ddr3l fmax_lpddr2 fmax_lpddr3	DDR Memory CLK Frequency (ECLK)	All Devices	_	400	_	350	_	312	MHz
DDR2/DDR3/DDR	3L/LPDDR2/LPDDR3 WRITE (DO	Q Output Data	are Cente	ered to DC	QS)				
toqvbs_ddr2 toqvbs_ddr3 toqvbs_ddr3 toqvbs_lpdr2 toqvbs_lpdr2 toqvbs_lpdr3 toqvas_ddr2	Data Output Valid before DQS Output	All Devices	_	-0.25	_	-0.25	_	-0.25	UI
tdqvas_ddr3 tdqvas_ddr3l tdqvas_lpddr2 tdqvas_lpddr3	Data Output Valid after DQS Output	All Devices	0.25	_	0.25	_	0.25	_	UI
fdata_ddr2 fdata_ddr3 fdata_ddr3l fdata_upddr2 fdata_upddr2 fdata_upddr3	DDR Memory Data Rate	All Devices	_	800	_	700	_	624	Mb/s
fmax_ddr2 fmax_ddr3 fmax_ddr3 fmax_ddr3l fmax_lpddr2 fmax_lpddr3	DDR Memory CLK Frequency (ECLK)	All Devices	_	400	_	350	_	312	MHz

Notes:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.

 General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load. Generic DDR timing are numbers based on LVDS I/O. DDR2 timing numbers are based on SSTL18. DDR3 timing numbers are based on SSTL15. LPDDR2 and LPDDR3 timing numbers are based on HSUL12.

- 3. Uses LVDS I/O standard for measurements.
- 4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- 5. All numbers are generated with the Diamond software.

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## 3.25. PCI Express Electrical and Timing Characteristics

### 3.25.1. PCIe (2.5 Gb/s) AC and DC Characteristics

Over recommended operating conditions.

#### Table 3.30. PCIe (2.5 Gb/s)

Symbol	Description	<b>Test Conditions</b>	Min	Тур	Max	Unit
Transmit <sup>1</sup>						
UI	Unit interval	_	399.88	400	400.12	ps
V <sub>TX-DIFF_P-P</sub>	Differential peak-to-peak output	-	0.8	1.0	1.2	V
V <sub>TX-DE-RATIO</sub>	De-emphasis differential output voltage ratio	_	-3	-3.5	-4	dB
V <sub>TX-CM-AC_P</sub>	RMS AC peak common-mode output voltage	_	_	_	20	mV
V <sub>TX-RCV-DETECT</sub>	Amount of voltage change allowed during receiver detection	_	_	_	600	mV
V <sub>TX-CM-DC</sub>	Tx DC common mode voltage	_	0	—	V <sub>CCHTX</sub>	V
I <sub>TX-SHORT</sub>	Output short circuit current	V <sub>TX-D+</sub> =0.0 V V <sub>TX-D-</sub> =0.0 V	_	_	90	mA
Z <sub>TX-DIFF-DC</sub>	Differential output impedance	_	80	100	120	Ω
RL <sub>TX-DIFF</sub>	Differential return loss	_	10	_	—	dB
RL <sub>TX-CM</sub>	Common mode return loss	_	6.0	_	—	dB
T <sub>TX-RISE</sub>	Tx output rise time	20% to 80%	0.125	_	—	UI
T <sub>TX-FALL</sub>	Tx output fall time	20% to 80%	0.125	_	—	UI
L <sub>TX-SKEW</sub>	Lane-to-lane static output skew for all lanes in port/link	_	_	_	1.3	ns
T <sub>TX-EYE</sub>	Transmitter eye width	—	0.75	_	—	UI
T <sub>TX-EYE-MEDIAN-TO-MAX-</sub> JITTER	Maximum time between jitter median and maximum deviation from median	-	-	-	0.125	UI
Receive <sup>1, 2</sup>						
UI	Unit Interval	_	399.88	400	400.12	ps
V <sub>RX-DIFF_P-P</sub>	Differential peak-to-peak input voltage	_	0.34 <sup>3</sup>	_	1.2	v
V <sub>RX-IDLE-DET-DIFF_P-P</sub>	Idle detect threshold voltage	_	65	—	340 <sup>3</sup>	mV
V <sub>RX-CM-AC_P</sub>	RMS AC peak common-mode input voltage	_	_	_	150	mV
Z <sub>RX-DIFF-DC</sub>	DC differential input impedance	_	80	100	120	Ω
Z <sub>RX-DC</sub>	DC input impedance	_	40	50	60	Ω
Z <sub>RX-HIGH-IMP-DC</sub>	Power-down DC input impedance	_	200K	—	-	Ω
RL <sub>RX-DIFF</sub>	Differential return loss	-	10	—	-	dB
RL <sub>RX-CM</sub>	Common mode return loss	—	6.0	—	_	dB

#### Notes:

- 1. Values are measured at 2.5 Gb/s.
- 2. Measured with external AC-coupling on the receiver.
- 3. Not in compliance with PCI Express 1.1 standard.

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## 3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

Symbol	Description	Test Conditions	Min	Тур	Max	Unit
Transmit			L	1	I	1
UI	Unit Interval	_	203.43	203.45	203.47	ps
T <sub>DCD</sub>	Duty Cycle Distortion	-	_	—	0.05	UI
J <sub>UBHPJ</sub>	Uncorrelated Bounded High Probability Jitter	-	_	-	0.15	UI
J <sub>TOTAL</sub>	Total Jitter	-	_	_	0.3	UI
Z <sub>RX-DIFF-DC</sub>	DC differential Impedance	-	80	_	120	Ω
T <sub>SKEW</sub>	Skew between differential signals	-	_	-	9	ps
D	Tx Differential Return Loss (S22),	100 MHz < freq < 3.6864 GHz	_	_	-8	dB
LTX-DIFF	including package and silicon	3.6864 GHz < freq < 4.9152 GHz	—	_	-8 + 16.6 *log (freq/3.6864)	dB
R <sub>LTX-CM</sub>	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	-	-	dB
I <sub>TX-SHORT</sub>	Transmitter short-circuit current	_	_	—	100	mA
T <sub>RISE_FALL</sub> -DIFF	Differential Rise and Fall Time	_		—	_	ps
L <sub>TX-SKEW</sub>	Lane-to-lane output skew	_	_	—		ps
Receive		·				
UI	Unit Interval	_	203.43	203.45	203.47	ps
V <sub>RX-DIFF-PP</sub>	Differential Rx peak-peak voltage	-	_	—	1.2	V, p-p
V <sub>RX-EYE_Y1_Y2</sub>	Receiver eye opening mask, Y1 and Y2	_	62.5	_	375	mV, diff
V <sub>RX-EYE_X1</sub>	Receiver eye opening mask, X1	-	_	—	0.3	UI
T <sub>RX-TJ</sub>	Receiver total jitter tolerance (not including sinusoidal)	_	_	_	0.6	UI
D	Receiver differential Return Loss,	100 MHz < freq < 3.6864 GHz	_	_	-8	dB
nLRX-DIFF	package plus silicon	3.6864 GHz < freq < 4.9152 GHz	-	-	-8 + 16.6 *log (freq/3.6864)	dB
R <sub>LRX-CM</sub>	Receiver common mode Return Loss, package plus silicon	_	6	_	_	dB
Z <sub>RX-DIFF-DC</sub>	Receiver DC differential impedance	_	80	100	120	Ω

#### Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics

**Note**: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

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Figure 3.23. JTAG Port Timing Waveforms

## 3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.



\*CL Includes Test Fixture and Probe Capacitance

#### Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards



## 4.3.2. LFE5U

Pin Information Summary		LFE5U-12		LFE5U-25		LFE5U-45				LFE5U-85					
Pin Type		256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	554 caBGA	285 csfBG	381 caBGA	554 caBGA	756 caBG
	Bank 0	24	6	24	24	6	24	24	6	27	32	6	27	32	56
General Purpose	Bank 1	32	6	32	32	6	32	32	6	33	40	6	33	40	48
	Bank 2	32	21	32	32	21	32	32	21	32	32	21	34	32	48
	Bank 3	32	28	32	32	28	32	32	28	33	48	28	33	48	64
Inputs/Outputs	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	14	24
per Bank	Bank 6	32	26	32	32	26	32	32	26	33	48	26	33	48	64
	Bank 7	32	18	32	32	18	32	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13	13	13	13	13	13
Total Single-Ende	d User	197	118	197	197	118	197	197	118	203	245	118	205	259	365
VCC		6	13	20	6	13	20	6	13	20	24	13	20	24	36
VCCAUX (Core)		2	3	4	2	3	4	2	3	4	9	3	4	9	8
	Bank 0	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 1	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 2	2	2	3	2	2	3	2	2	3	4	2	3	4	4
VCCIO	Bank 3	2	2	3	2	2	3	2	2	3	3	2	3	3	4
VCCIO	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	2	2
	Bank 6	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 7	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 8	1	2	2	1	2	2	1	2	2	2	2	2	2	2
ТАР		4	4	4	4	4	4	4	4	4	4	4	4	4	4
Miscellaneous De	dicated	7	7	7	7	7	7	7	7	7	7	7	7	7	7
GND		27	123	99	27	123	99	27	123	99	198	123	99	198	267
NC		0	1	26	0	1	26	0	1	26	33	1	26	33	29
Reserved		0	4	6	0	4	6	0	4	6	12	4	6	12	12
Total Balls		256	285	381	256	285	381	256	285	381	554	285	381	554	756
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8
High Speed Differ	ential	Bank	16/8	14/7	16/8	16/8	14/7	16/8	16/8	14/7	16/8	24/12	14/7	16/8	24/1
Input / Output Pa	irs	Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	16/8	13/6	16/8	16/8	13/6	16/8	16/8	13/6	16/8	24/12	13/6	16/8	24/1
		Bank	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
Total High Speed		64/32	45/27	64/32	64/32	45/27	64/32	64/32	45/27	64/32	80/40	45/27	65/33	80/40	112/
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	2	1	2	2	1	2	2	1	2	2	1	2	2
DQS Groups	,	Bank	2	2	2	2	2	2	2	2	2	3	2	2	3
(> 11 pins in grou	p)	Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	2	2	2	2	2	2	2	2	2	3	2	2	3
		Bank	2	1	2	2	1	2	2	1	2	2	1	2	2
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
Total DQS Groups	5	8	6	8	8	6	8	8	6	8	10	6	8	10	14