Lattice Semiconductor Corporation - LFE5UM5G-25F-8MG285C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	118
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	285-LFBGA, CSPBGA
Supplier Device Package	285-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um5g-25f-8mg285c

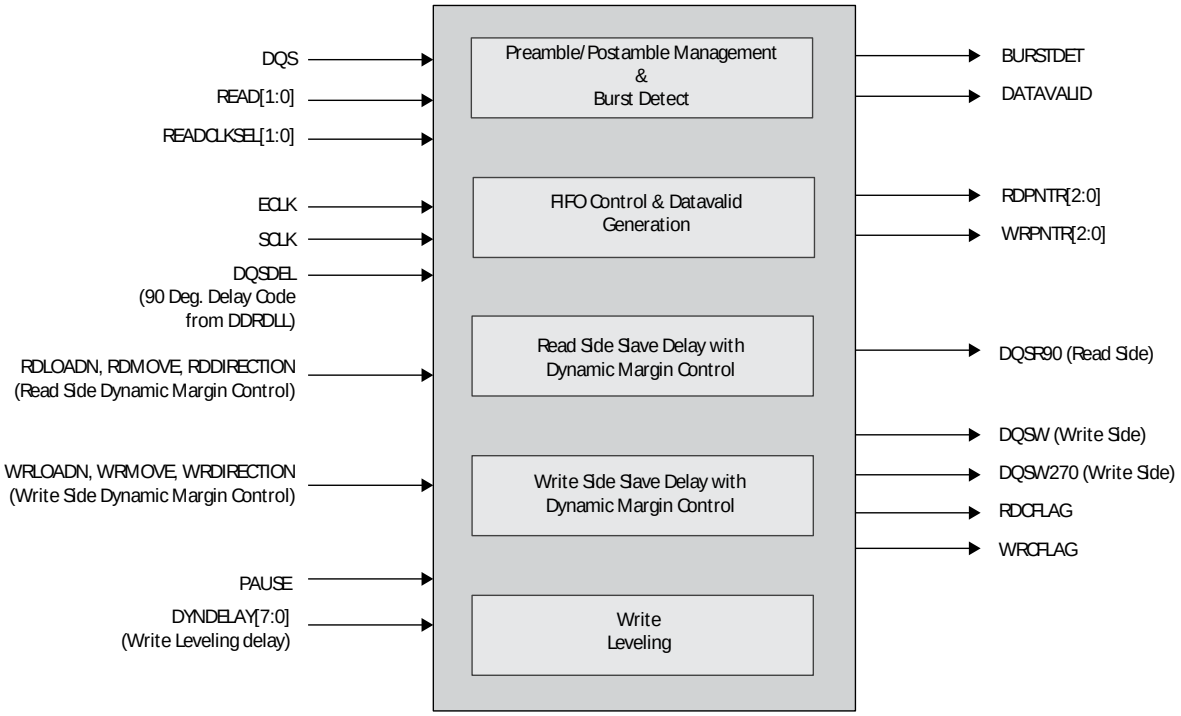

Figure 2.24. DQS Control and Delay Block (DQSBUF)

Table 2.11. DQSBUF Pin List Description

Name	Type	Description
DQS	Input	DDR memory DQS strobe
READ[1:0]	Input	Read Input from DDR Controller
READCLKSEL[1:0]	Input	Read pulse selection
SCLK	Input	Slow System Clock
ECLK	Input	High Speed Edge Clock (same frequency as DDR memory)
DQSDEL	Input	90° Delay Code from DDRDLL
RDLOADN, RDMOVE, RDDIRECTION	Input	Dynamic Margin Control ports for Read delay
WRLOADN, WRMOVE, WRDIRECTION	Input	Dynamic Margin Control ports for Write delay
PAUSE	Input	Used by DDR Controller to Pause write side signals during DDRDLL Code update or Write Leveling
DYNDELAY[7:0]	Input	Dynamic Write Leveling Delay Control
DQSR90	Output	90° delay DQS used for Read
DQSW270	Output	90° delay clock used for DQ Write
DQSW	Output	Clock used for DQS Write
RDPNTR[2:0]	Output	Read Pointer for IFIFO module
WRPNTR[2:0]	Output	Write Pointer for IFIFO module
DATAVALID	Output	Signal indicating start of valid data
BURSTDET	Output	Burst Detect indicator
RDFLAG	Output	Read Dynamic Margin Control output to indicate max value
WRFLAG	Output	Write Dynamic Margin Control output to indicate max value

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