# Lattice Semiconductor Corporation - LFE5UM5G-45F-8BG381C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 11000 |
| Number of Logic Elements/Cells | 44000 |
| Total RAM Bits | 1990656 |
| Number of I/O | 203 |
| Number of Gates | - |
| Voltage - Supply | 1.045V ~ 1.155V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 381-FBGA |
| Supplier Device Package | 381-CABGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um5g-45f-8bg381c |

# Contents

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# 2. Architecture

## 2.1. Overview

Each ECP5/ECP5-5G device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2.1 on page 13. The LFE5-85 devices have three rows of DSP slices, the LFE5-45 devices have two rows, and both LFE5-25 and LFE5-12 devices have one. In addition, the LFE5UM/LFE5UM5G devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5/ECP5-5G devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5/ECP5-5G devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 devices feature up to four embedded 3.2 Gb/s SERDES channels, and the ECP5-5G devices feature up to four embedded 5 Gb/s SERDES channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the ECP5/ECP5-5G devices are arranged in seven banks (eight banks for LFE5-85 devices in caBGA756 and caBGA554 packages), allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. Half of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5/ECP5-5G registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The ECP5/ECP5-5G architecture provides up to four Delay-Locked Loops (DLLs) and up to four Phase-Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5/ECP5-5G family supports a sysCONFIG™ ports located in that same corner, powered by Vccio8, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 devices use 1.1 V and ECP5UM5G devices use 1.2 V as their core voltage.

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## 2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
    - A greater-than-or-equal-to B
    - A not-equal-to B
    - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

### RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.
A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

**Table 2.3. Number of Slices Required to Implement Distributed RAM**

| | SPR 16 X 4 | PDPR 16 X 4 |
|---|---|---|
| Number of slices | 3 | 6 |

**Note**: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

### ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

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### 2.8.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

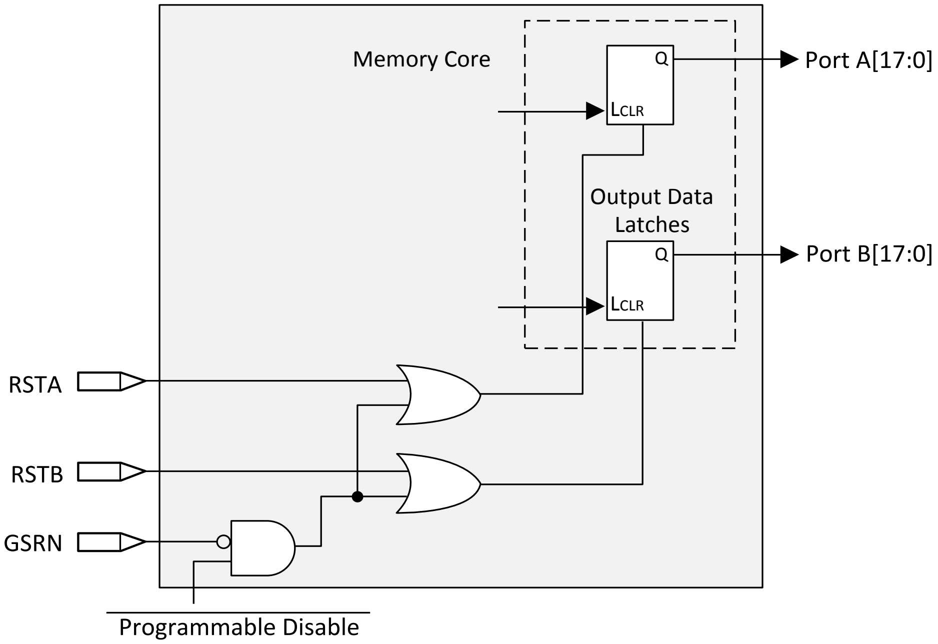

**Figure 2.12. Memory Core Reset**

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 102.

## 2.9. sysDSP™ Slice

The ECP5/ECP5-5G family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### 2.9.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5/ECP5-5G device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

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  - 5*5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5/ ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.

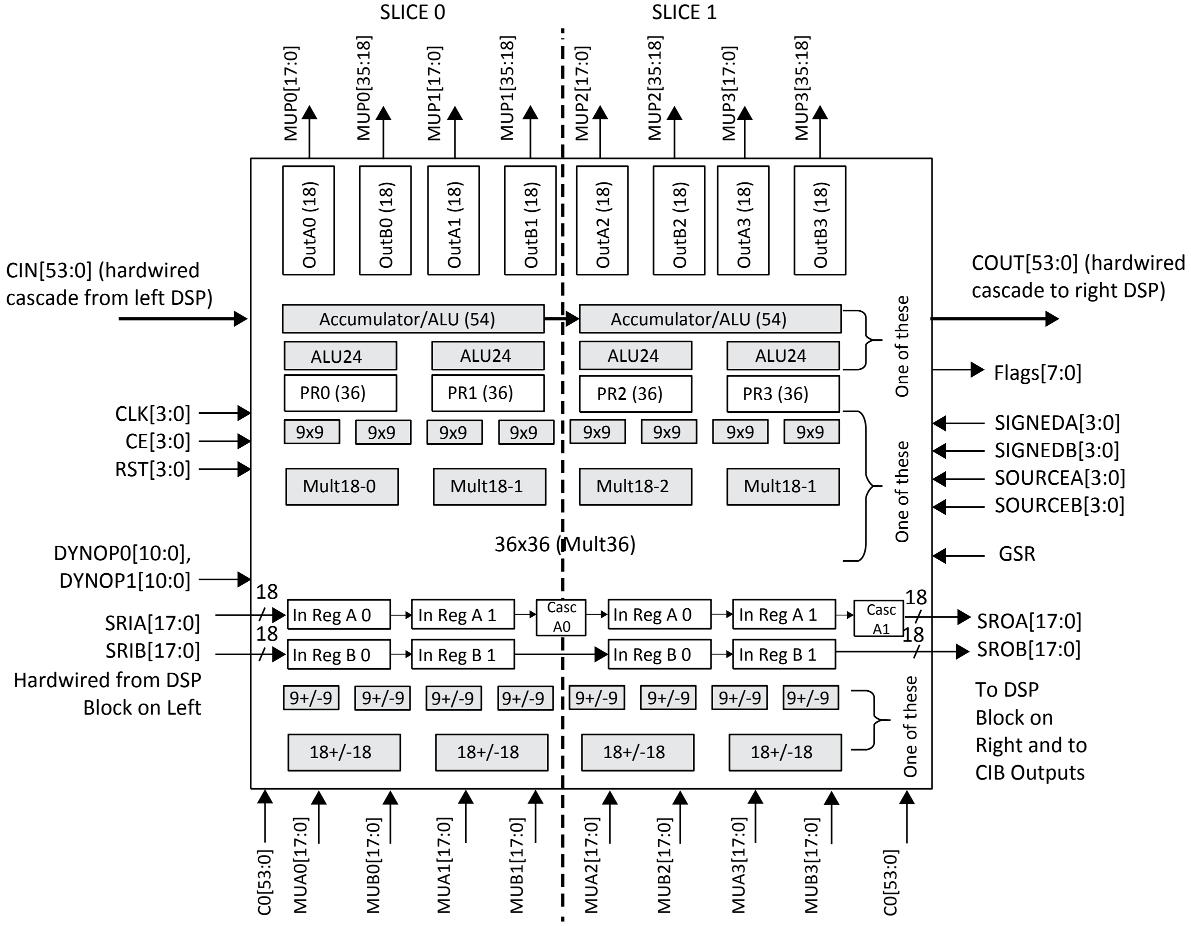

**Figure 2.14. Simplified sysDSP Slice Block Diagram**

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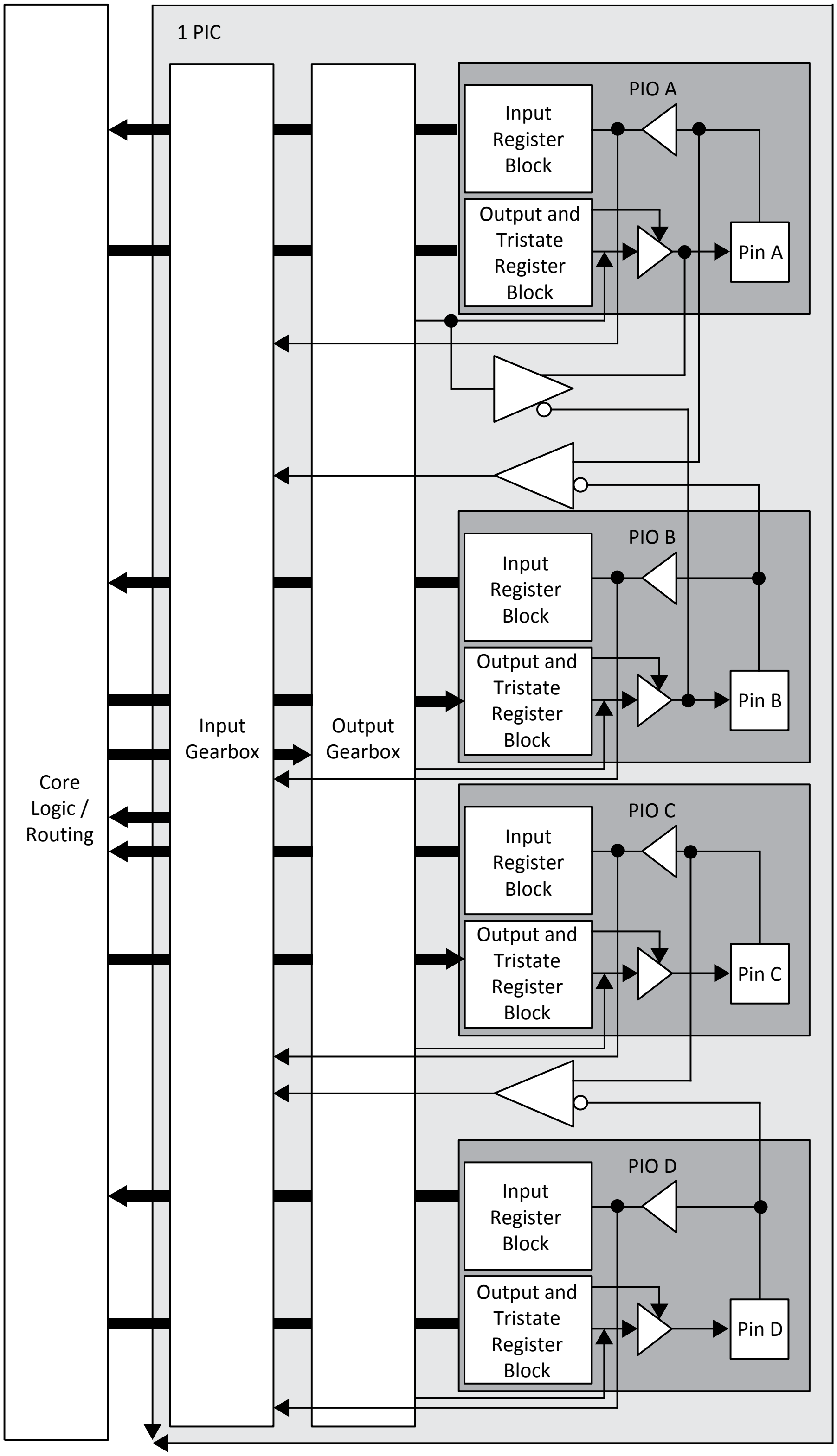

Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Sides

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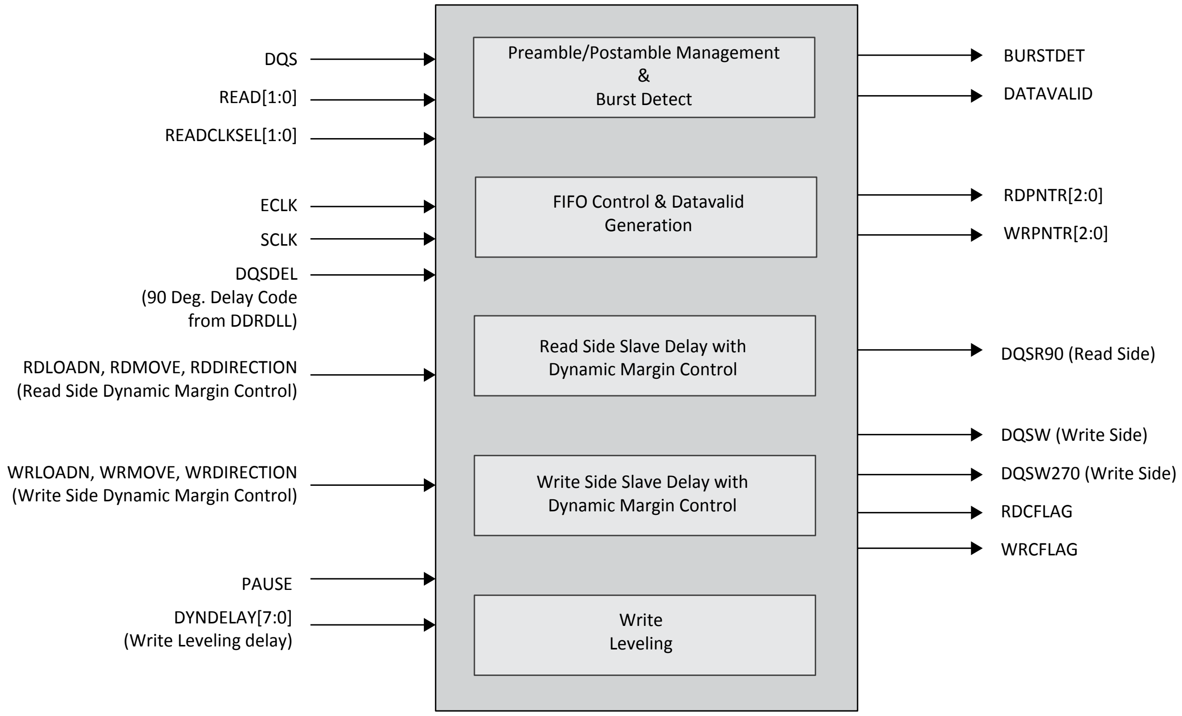

**Figure 2.24. DQS Control and Delay Block (DQSBUF)**

### Table 2.11. DQSBUF Port List Description

| Name | Type | Description |
|---|---|---|
| DQS | Input | DDR memory DQS strobe |
| READ[1:0] | Input | Read Input from DDR Controller |
| READCLKSEL[1:0] | Input | Read pulse selection |
| SCLK | Input | Slow System Clock |
| ECLK | Input | High Speed Edge Clock (same frequency as DDR memory) |
| DQSDEL | Input | 90° Delay Code from DDRDLL |
| RDLOADN, RDMOVE, RDDIRECTION | Input | Dynamic Margin Control ports for Read delay |
| WRLOADN, WRMOVE, WRDIRECTION | Input | Dynamic Margin Control ports for Write delay |
| PAUSE | Input | Used by DDR Controller to Pause write side signals during DDRDLL Code update or Write Leveling |
| DYNDELAY[7:0] | Input | Dynamic Write Leveling Delay Control |
| DQSR90 | Output | 90° delay DQS used for Read |
| DQSW270 | Output | 90° delay clock used for DQ Write |
| DQSW | Output | Clock used for DQS Write |
| RDPNTR[2:0] | Output | Read Pointer for IFIFO module |
| WRPNTR[2:0] | Output | Write Pointer for IFIFO module |
| DATAVALID | Output | Signal indicating start of valid data |
| BURSTDET | Output | Burst Detect indicator |
| RDFLAG | Output | Read Dynamic Margin Control output to indicate max value |
| WRFLAG | Output | Write Dynamic Margin Control output to indicate max value |

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## 2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. Figure 2.27 shows the position of the dual blocks for the LFE5-85. Table 2.13 shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

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## 3.14. sysI/O Differential Electrical Characteristics

### 3.14.1. LVDS

Over recommended operating conditions.

**Table 3.13. LVDS**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | — | 0 | — | 2.4 | V |
| $V_{CM}$ | Input Common Mode Voltage | Half the sum of the two Inputs | 0.05 | — | 2.35 | V |
| $V_{THD}$ | Differential Input Threshold | Difference between the two Inputs | ±100 | — | — | mV |
| $I_{IN}$ | Input Current | Power On or Power Off | — | — | ±10 | µA |
| $V_{OH}$ | Output High Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ω | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output Low Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ω | 0.9 V | 1.03 | — | V |
| $V_{OD}$ | Output Voltage Differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ω | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Between High and Low | — | — | — | 50 | mV |
| $V_{OS}$ | Output Voltage Offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100 Ω | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between H and L | — | — | — | 50 | mV |
| $I_{SAB}$ | Output Short Circuit Current | $V_{OD}$ = 0 V Driver outputs shorted to each other | — | — | 12 | mA |

**Note**: On the left and right sides of the device, this specification is valid only for $V_{CCIO}$ = 2.5 V or 3.3 V.

### 3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

### 3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V $V_{CCIO}$. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

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### 3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

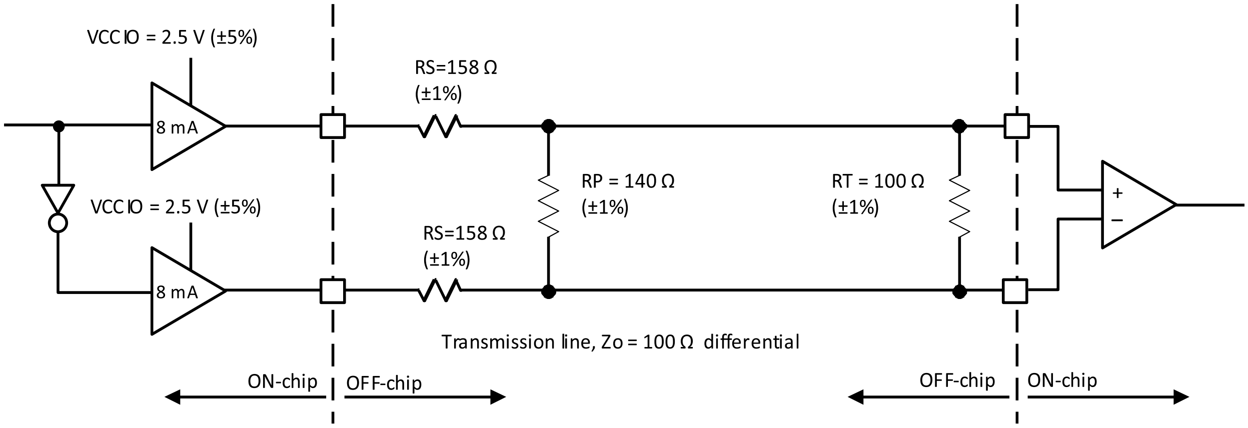

**Figure 3.1. LVDS25E Output Termination Example**

**Table 3.14. LVDS25E DC Conditions**

| Parameter | Description | Typical | Unit |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (±5%) | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 20 | Ω |
| $R_S$ | Driver Series Resistor (±1%) | 158 | Ω |
| $R_P$ | Driver Parallel Resistor (±1%) | 140 | Ω |
| $R_T$ | Receiver Termination (±1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage | 1.43 | V |
| $V_{OL}$ | Output Low Voltage | 1.07 | V |
| $V_{OD}$ | Output Differential Voltage | 0.35 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 6.03 | mA |

**Note**: For input buffer, see LVDS Table 3.13 on page 55.

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**Table 3.20. Register-to-Register Performance**

| Function | –8 Timing | Unit |
|---|---|---|
| **Basic Functions** | | |
| 16-Bit Decoder | 441 | MHz |
| 32-Bit Decoder | 441 | MHz |
| 64-Bit Decoder | 332 | MHz |
| 4:1 Mux | 441 | MHz |
| 8:1 Mux | 441 | MHz |
| 16:1 Mux | 441 | MHz |
| 32:1 Mux | 441 | MHz |
| 8-Bit Adder | 441 | MHz |
| 16-Bit Adder | 441 | MHz |
| 64-Bit Adder | 441 | MHz |
| 16-Bit Counter | 384 | MHz |
| 32-Bit Counter | 317 | MHz |
| 64-Bit Counter | 263 | MHz |
| 64-Bit Accumulator | 288 | MHz |
| **Embedded Memory Functions** | | |
| 1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers | 272 | MHz |
| 1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers | 214 | MHz |
| **Distributed Memory Functions** | | |
| 16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU) | 441 | MHz |
| 16 x 4 Pseudo-Dual Port (Two PFUs) | 441 | MHz |
| **DSP Functions** | | |
| 9 x 9 Multiplier (All Registers) | 225 | MHz |
| 18 x 18 Multiplier (All Registers) | 225 | MHz |
| 36 x 36 Multiplier (All Registers) | 225 | MHz |
| 18 x 18 Multiply-Add/Sub (All Registers) | 225 | MHz |
| 18 x 18 Multiply/Accumulate (Input and Output Registers) | 225 | MHz |

**Notes**:

1. These functions were generated using Lattice Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Diamond design software tool.

## 3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

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## 3.17. Maximum I/O Buffer Speed

Over recommended operating conditions.

**Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed**

| Buffer | Description | Max | Unit |
|---|---|---|---|
| **Maximum Input Frequency** | | | |
| LVDS25 | LVDS, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| MLVDS25 | MLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| BLVDS25 | BLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| MIPI D-PHY (HS Mode) | MIPI Video | 400 | MHz |
| SLVS | SLVS similar to MIPI | 400 | MHz |
| Mini LVDS | Mini LVDS | 400 | MHz |
| LVPECL33 | LVPECL, Emulated, $V_{CCIO}$ = 3.3 V | 400 | MHz |
| SSTL18 (all supported classes) | SSTL_18 class I, II, $V_{CCIO}$ = 1.8 V | 400 | MHz |
| SSTL15 (all supported classes) | SSTL_15 class I, II, $V_{CCIO}$ = 1.5 V | 400 | MHz |
| SSTL135 (all supported classes) | SSTL_135 class I, II, $V_{CCIO}$ = 1.35 V | 400 | MHz |
| HSUL12 (all supported classes) | HSUL_12 class I, II, $V_{CCIO}$ = 1.2 V | 400 | MHz |
| LVTTL33 | LVTTL, $V_{CCIO}$ = 3.3 V | 200 | MHz |
| LVCMOS33 | LVCMOS, $V_{CCIO}$ = 3.3 V | 200 | MHz |
| LVCMOS25 | LVCMOS, $V_{CCIO}$ = 2.5 V | 200 | MHz |
| LVCMOS18 | LVCMOS, $V_{CCIO}$ = 1.8 V | 200 | MHz |
| LVCMOS15 | LVCMOS 1.5, $V_{CCIO}$ = 1.5 V | 200 | MHz |
| LVCMOS12 | LVCMOS 1.2, $V_{CCIO}$ = 1.2 V | 200 | MHz |
| **Maximum Output Frequency** | | | |
| LVDS25E | LVDS, Emulated, $V_{CCIO}$ = 2.5 V | 150 | MHz |
| LVDS25 | LVDS, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| MLVDS25 | MLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 150 | MHz |
| BLVDS25 | BLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 150 | MHz |
| LVPECL33 | LVPECL, Emulated, $V_{CCIO}$ = 3.3 V | 150 | MHz |
| SSTL18 (all supported classes) | SSTL_18 class I, II, $V_{CCIO}$ = 1.8 V | 400 | MHz |
| SSTL15 (all supported classes) | SSTL_15 class I, II, $V_{CCIO}$ = 1.5 V | 400 | MHz |
| SSTL135 (all supported classes) | SSTL_135 class I, II, $V_{CCIO}$ = 1.35 V | 400 | MHz |
| HSUL12 (all supported classes) | HSUL12 class I, II, $V_{CCIO}$ = 1.2 V | 400 | MHz |
| LVTTL33 | LVTTL, VCCIO = 3.3 V | 150 | MHz |
| LVCMOS33 (For all drives) | LVCMOS, 3.3 V | 150 | MHz |
| LVCMOS25 (For all drives) | LVCMOS, 2.5 V | 150 | MHz |
| LVCMOS18 (For all drives) | LVCMOS, 1.8 V | 150 | MHz |
| LVCMOS15 (For all drives) | LVCMOS, 1.5 V | 150 | MHz |
| LVCMOS12 (For all drives) | LVCMOS, 1.2 V | 150 | MHz |

**Notes**:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Switching Test Conditions, Table 3.44 on page 90.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

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| Parameter | Description | Device | –8 |  | –7 |  | –6 |  | Unit |
|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Min | Max | Min | Max | Min | Max |  |
| $f_{DATA\_DDR2}$<br>$f_{DATA\_DDR3}$<br>$f_{DATA\_DDR3L}$<br>$f_{DATA\_LPDDR2}$<br>$f_{DATA\_LPDDR3}$ | DDR Memory Data Rate | All Devices | — | 800 | — | 700 | — | 624 | Mb/s |
| $f_{MAX\_DDR2}$<br>$f_{MAX\_DDR3}$<br>$f_{MAX\_DDR3L}$<br>$f_{MAX\_LPDDR2}$<br>$f_{MAX\_LPDDR3}$ | DDR Memory CLK Frequency (ECLK) | All Devices | — | 400 | — | 350 | — | 312 | MHz |
| **DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS)** |  |  |  |  |  |  |  |  |  |
| $t_{DQVBS\_DDR2}$<br>$t_{DQVBS\_DDR3}$<br>$t_{DQVBS\_DDR3L}$<br>$t_{DQVBS\_LPDDR2}$<br>$t_{DQVBS\_LPDDR3}$ | Data Output Valid before DQS Output | All Devices | — | –0.25 | — | –0.25 | — | -0.25 | UI |
| $t_{DQVAS\_DDR2}$<br>$t_{DQVAS\_DDR3}$<br>$t_{DQVAS\_DDR3L}$<br>$t_{DQVAS\_LPDDR2}$<br>$t_{DQVAS\_LPDDR3}$ | Data Output Valid after DQS Output | All Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA\_DDR2}$<br>$f_{DATA\_DDR3}$<br>$f_{DATA\_DDR3L}$<br>$f_{DATA\_LPDDR2}$<br>$f_{DATA\_LPDDR3}$ | DDR Memory Data Rate | All Devices | — | 800 | — | 700 | — | 624 | Mb/s |
| $f_{MAX\_DDR2}$<br>$f_{MAX\_DDR3}$<br>$f_{MAX\_DDR3L}$<br>$f_{MAX\_LPDDR2}$<br>$f_{MAX\_LPDDR3}$ | DDR Memory CLK Frequency (ECLK) | All Devices | — | 400 | — | 350 | — | 312 | MHz |

**Notes**:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.
2. General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load.
   Generic DDR timing are numbers based on LVDS I/O.
   DDR2 timing numbers are based on SSTL18.
   DDR3 timing numbers are based on SSTL15.
   LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
3. Uses LVDS I/O standard for measurements.
4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
5. All numbers are generated with the Diamond software.

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## 3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

**Table 3.32. CPRI LV2 E.48 Electrical and Timing Characteristics**

| Symbol | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Transmit** | | | | | | |
| UI | Unit Interval | — | 203.43 | 203.45 | 203.47 | ps |
| $T_{DCD}$ | Duty Cycle Distortion | — | — | — | 0.05 | UI |
| $J_{UBHPJ}$ | Uncorrelated Bounded High Probability Jitter | — | — | — | 0.15 | UI |
| $J_{TOTAL}$ | Total Jitter | — | — | — | 0.3 | UI |
| $Z_{RX\text{-}DIFF\text{-}DC}$ | DC differential Impedance | — | 80 | — | 120 | Ω |
| $T_{SKEW}$ | Skew between differential signals | — | — | — | 9 | ps |
| $R_{LTX\text{-}DIFF}$ | Tx Differential Return Loss (S22), including package and silicon | 100 MHz < freq < 3.6864 GHz | — | — | –8 | dB |
| | | 3.6864 GHz < freq < 4.9152 GHz | — | — | –8 + 16.6 *log (freq/3.6864) | dB |
| $R_{LTX\text{-}CM}$ | Tx Common Mode Return Loss, including package and silicon | 100 MHz < freq < 3.6864 GHz | 6 | — | — | dB |
| $I_{TX\text{-}SHORT}$ | Transmitter short-circuit current | — | — | — | 100 | mA |
| $T_{RISE\_FALL\text{-}DIFF}$ | Differential Rise and Fall Time | — | | — | — | ps |
| $L_{TX\text{-}SKEW}$ | Lane-to-lane output skew | — | — | — | | ps |
| **Receive** | | | | | | |
| UI | Unit Interval | — | 203.43 | 203.45 | 203.47 | ps |
| $V_{RX\text{-}DIFF\text{-}PP}$ | Differential Rx peak-peak voltage | — | — | — | 1.2 | V, p-p |
| $V_{RX\text{-}EYE\_Y1\_Y2}$ | Receiver eye opening mask, Y1 and Y2 | — | 62.5 | — | 375 | mV, diff |
| $V_{RX\text{-}EYE\_X1}$ | Receiver eye opening mask, X1 | — | — | — | 0.3 | UI |
| $T_{RX\text{-}TJ}$ | Receiver total jitter tolerance (not including sinusoidal) | — | — | — | 0.6 | UI |
| $R_{LRX\text{-}DIFF}$ | Receiver differential Return Loss, package plus silicon | 100 MHz < freq < 3.6864 GHz | — | — | –8 | dB |
| | | 3.6864 GHz < freq < 4.9152 GHz | — | — | –8 + 16.6 *log (freq/3.6864) | dB |
| $R_{LRX\text{-}CM}$ | Receiver common mode Return Loss, package plus silicon | — | 6 | — | — | dB |
| $Z_{RX\text{-}DIFF\text{-}DC}$ | Receiver DC differential impedance | — | 80 | 100 | 120 | Ω |

**Note**: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

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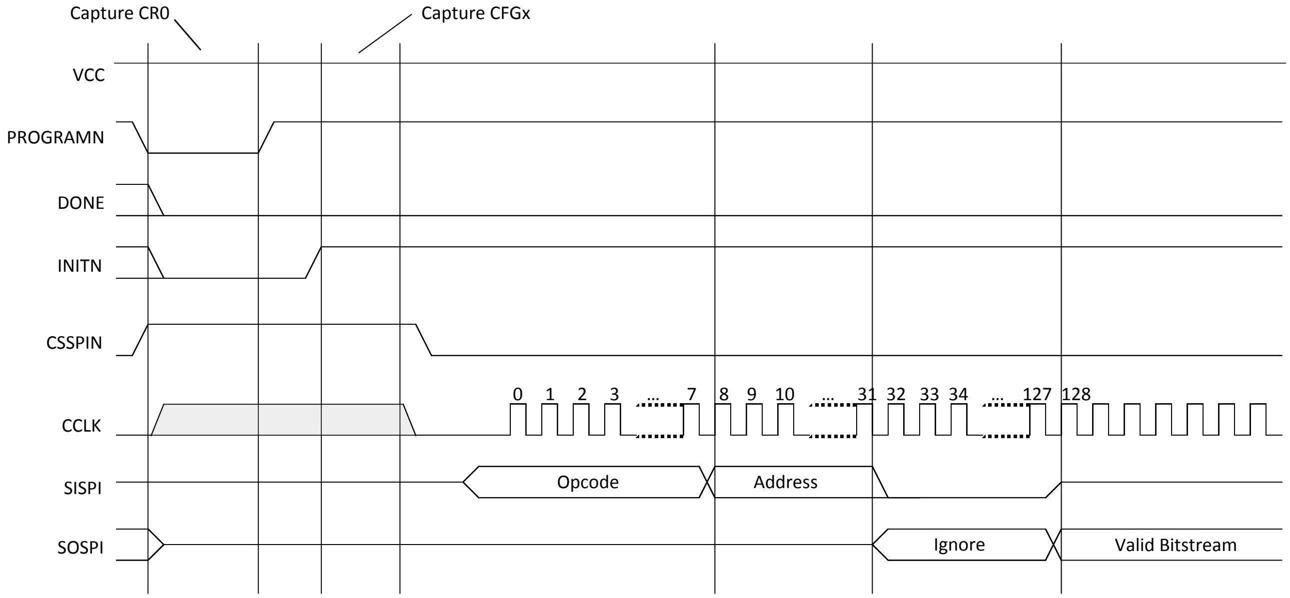

Figure 3.22. Master SPI Configuration Waveforms

## 3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | 25 | MHz |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 10 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 8 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

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# 4. Pinout Information

## 4.1. Signal Descriptions

| Signal Name | I/O | Description |
|---|---|---|
| **General Purpose** | | |
| P[L/R] [Group Number]_[A/B/C/D] | I/O | [L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group.<br>[A/B/C/D] indicates the PIO within the PIC to which the pad is connected.<br>Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration.<br>PIO A and B are grouped as a pair, and PIO C and D are group as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer.<br>Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω. |
| P[T/B][Group Number]_[A/B] | I/O | [T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group.<br>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration.<br>PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer.<br>PIO A/B forms a pair of emulated differential output buffer. |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| RESERVED | — | This pin is reserved and should not be connected to anything on the board. |
| GND | — | Ground. Dedicated pins. |
| $V_{CC}$ | — | Power supply pins for core logic. Dedicated pins. $V_{CC}$ = 1.1 V (ECP5), 1.2 V (ECP5UM5G) |
| $V_{CCAUX}$ | — | Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. $V_{CCAUX}$ = 2.5 V. |
| $V_{CCIOx}$ | — | Dedicated power supply pins for I/O bank x. $V_{CCIO8}$ is used for configuration and JTAG. |
| VREF1_x | — | Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as VREF1 input. When not used, they may be used as I/O pins. |
| **PLL, DLL and Clock Functions** | | |
| [LOC][_GPLL[T, C]_IN | I | General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not configured as GPLL input pads, they can be used as general purpose I/O pins. |
| GR_PCLK[Bank][num] | I | General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to ECP5 sysClock PLL/DLL Design and Usage Guide (TN1263). These pins are shared I/O pins. When not configured as GR pins, they can be used as general purpose I/O pins. |
| PCLK[T/C][Bank]_[num] | I/O | General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/ O pins. When not configured as PCLK pins, they can be used as general purpose I/O pins. |

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| Part number | Grade | Package | Pins | Temp. | LUTs (K) | SERDES |
|---|---|---|---|---|---|---|
| LFE5UM5G-85F-8BG381C | –8 | Lead free caBGA | 381 | Commercial | 84 | Yes |
| LFE5UM5G-85F-8BG554C | –8 | Lead free caBGA | 554 | Commercial | 84 | Yes |
| LFE5UM5G-85F-8BG756C | –8 | Lead free caBGA | 756 | Commercial | 84 | Yes |

### 5.2.2. Industrial

| Part number | Grade | Package | Pins | Temp. | LUTs (K) | SERDES |
|---|---|---|---|---|---|---|
| LFE5U-12F-6BG256I | –6 | Lead free caBGA | 256 | Industrial | 12 | No |
| LFE5U-12F-7BG256I | –7 | Lead free caBGA | 256 | Industrial | 12 | No |
| LFE5U-12F-8BG256I | –8 | Lead free caBGA | 256 | Industrial | 12 | No |
| LFE5U-12F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 12 | No |
| LFE5U-12F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 12 | No |
| LFE5U-12F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 12 | No |
| LFE5U-12F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 12 | No |
| LFE5U-12F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 12 | No |
| LFE5U-12F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 12 | No |
| LFE5U-25F-6BG256I | –6 | Lead free caBGA | 256 | Industrial | 24 | No |
| LFE5U-25F-7BG256I | –7 | Lead free caBGA | 256 | Industrial | 24 | No |
| LFE5U-25F-8BG256I | –8 | Lead free caBGA | 256 | Industrial | 24 | No |
| LFE5U-25F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 24 | No |
| LFE5U-25F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 24 | No |
| LFE5U-25F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 24 | No |
| LFE5U-25F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 24 | No |
| LFE5U-25F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 24 | No |
| LFE5U-25F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 24 | No |
| LFE5U-45F-6BG256I | –6 | Lead free caBGA | 256 | Industrial | 44 | No |
| LFE5U-45F-7BG256I | –7 | Lead free caBGA | 256 | Industrial | 44 | No |
| LFE5U-45F-8BG256I | –8 | Lead free caBGA | 256 | Industrial | 44 | No |
| LFE5U-45F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 44 | No |
| LFE5U-45F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 44 | No |
| LFE5U-45F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 44 | No |
| LFE5U-45F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 44 | No |
| LFE5U-45F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 44 | No |
| LFE5U-45F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 44 | No |
| LFE5U-45F-6BG554I | –6 | Lead free caBGA | 554 | Industrial | 44 | No |
| LFE5U-45F-7BG554I | –7 | Lead free caBGA | 554 | Industrial | 44 | No |
| LFE5U-45F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 44 | No |
| LFE5U-85F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 84 | No |
| LFE5U-85F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 84 | No |
| LFE5U-85F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 84 | No |
| LFE5U-85F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 84 | No |
| LFE5U-85F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 84 | No |
| LFE5U-85F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 84 | No |
| LFE5U-85F-6BG554I | –6 | Lead free caBGA | 554 | Industrial | 84 | No |
| LFE5U-85F-7BG554I | –7 | Lead free caBGA | 554 | Industrial | 84 | No |
| LFE5U-85F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 84 | No |

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| Part number | Grade | Package | Pins | Temp. | LUTs (K) | SERDES |
|---|---|---|---|---|---|---|
| LFE5U-85F-6BG756I | –6 | Lead free caBGA | 756 | Industrial | 84 | No |
| LFE5U-85F-7BG756I | –7 | Lead free caBGA | 756 | Industrial | 84 | No |
| LFE5U-85F-8BG756I | –8 | Lead free caBGA | 756 | Industrial | 84 | No |
| LFE5UM-25F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 24 | Yes |
| LFE5UM-25F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 24 | Yes |
| LFE5UM-25F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 24 | Yes |
| LFE5UM-25F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 24 | Yes |
| LFE5UM-25F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 24 | Yes |
| LFE5UM-25F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 24 | Yes |
| LFE5UM-45F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 44 | Yes |
| LFE5UM-45F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 44 | Yes |
| LFE5UM-45F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 44 | Yes |
| LFE5UM-45F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 44 | Yes |
| LFE5UM-45F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 44 | Yes |
| LFE5UM-45F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 44 | Yes |
| LFE5UM-45F-6BG554I | –6 | Lead free caBGA | 554 | Industrial | 44 | Yes |
| LFE5UM-45F-7BG554I | –7 | Lead free caBGA | 554 | Industrial | 44 | Yes |
| LFE5UM-45F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 44 | Yes |
| LFE5UM-85F-6MG285I | –6 | Lead free csfBGA | 285 | Industrial | 84 | Yes |
| LFE5UM-85F-7MG285I | –7 | Lead free csfBGA | 285 | Industrial | 84 | Yes |
| LFE5UM-85F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 84 | Yes |
| LFE5UM-85F-6BG381I | –6 | Lead free caBGA | 381 | Industrial | 84 | Yes |
| LFE5UM-85F-7BG381I | –7 | Lead free caBGA | 381 | Industrial | 84 | Yes |
| LFE5UM-85F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 84 | Yes |
| LFE5UM-85F-6BG554I | –6 | Lead free caBGA | 554 | Industrial | 84 | Yes |
| LFE5UM-85F-7BG554I | –7 | Lead free caBGA | 554 | Industrial | 84 | Yes |
| LFE5UM-85F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 84 | Yes |
| LFE5UM-85F-6BG756I | –6 | Lead free caBGA | 756 | Industrial | 84 | Yes |
| LFE5UM-85F-7BG756I | –7 | Lead free caBGA | 756 | Industrial | 84 | Yes |
| LFE5UM-85F-8BG756I | –8 | Lead free caBGA | 756 | Industrial | 84 | Yes |
| LFE5UM5G-25F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 24 | Yes |
| LFE5UM5G-25F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 24 | Yes |
| LFE5UM5G-45F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 44 | Yes |
| LFE5UM5G-45F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 44 | Yes |
| LFE5UM5G-45F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 44 | Yes |
| LFE5UM5G-85F-8MG285I | –8 | Lead free csfBGA | 285 | Industrial | 84 | Yes |
| LFE5UM5G-85F-8BG381I | –8 | Lead free caBGA | 381 | Industrial | 84 | Yes |
| LFE5UM5G-85F-8BG554I | –8 | Lead free caBGA | 554 | Industrial | 84 | Yes |
| LFE5UM5G-85F-8BG756I | –8 | Lead free caBGA | 756 | Industrial | 84 | Yes |

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# Revision History

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2018 | 1.9 | All | Updated formatting and page referencing. |
| | | General Description | Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-45. |
| | | Architecture | Added a row for SGMII in Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support. Updated footnote #1. |
| | | DC and Switching Characteristics | Updated Table 3.2. Recommended Operating Conditions. |
| | | | Added 2 rows and updated values in Table 3.7. DC Electrical Characteristics. |
| | | | Updated Table 3.8. ECP5/ECP5-5G Supply Current (Standby). |
| | | | Updated Table 3.11. sysI/O Recommended Operating Conditions. |
| | | | Updated Table 3.12. Single-Ended DC Characteristics. |
| | | | Updated Table 3.13. LVDS. |
| | | | Updated Table 3.14. LVDS25E DC Conditions. |
| | | | Updated Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed. |
| | | | Updated Table 3.28. Receiver Total Jitter Tolerance Specification. |
| | | | Updated header name of section 3.28 CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics. |
| | | | Updated header name of section 3.29 Gigabit Ethernet/SGMII(1.25Gbps)/CPRI LV E.12 Electrical and Timing Characteristics |
| | | Pinout Information | Updated table in section 4.3.2 LFE5U. |
| | | Ordering Information | Added table rows in 5.2.1 Commercial. |
| | | | Added table rows in 5.2.2 Industrial. |
| | | Supplemental Information | Updated For Further Information section. |
| November 2017 | 1.8 | General Description | Updated Table 1.1. ECP5 and ECP5-5G Family Selection Guide. Added caBGA256 package in LFE5U-12 and LFE5U-25. |

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