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## Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	259
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um5g-85f-8bg554c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um5g-85f-8bg554c</a>

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## Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay-Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVC MOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLL	Phase-Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SERDES	Serializer/Deserializer
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing

# 1. General Description

The ECP5/ECP5-5G family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES (Serializer/Deserializer), and high speed source synchronous interfaces, in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5/ECP5-5G device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5/ECP5-5G device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5/ECP5-5G FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5/ECP5-5G devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase-Locked Loops (PLLs), Delay-Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5/ECP5-5G device family supports a broad range of interface standards including DDR2/3, LPDDR2/3, XGMII, and 7:1 LVDS.

The ECP5/ECP5-5G device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5/ECP5-5G devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

ECP5-5G family devices have made some enhancement in the SERDES compared to ECP5UM devices. These enhancements increase the performance of the SERDES to up to 5 Gb/s data rate.

The ECP5-5G family devices are pin-to-pin compatible with the ECP5UM devices. These allows a migration path for users to port designs from ECP5UM to ECP5-5G devices to get higher performance.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5/ECP5-5G FPGA family. Synthesis library support for ECP5/ECP5-5G devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5/ECP5-5G device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5/ECP5-5G family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

## 1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 84K LUTs
  - 197 to 365 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - 270 Mb/s, up to 5.0 Gb/s, SERDES interface (ECP5-5G)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, SGMII, XAUI), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 3.744 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 669K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs

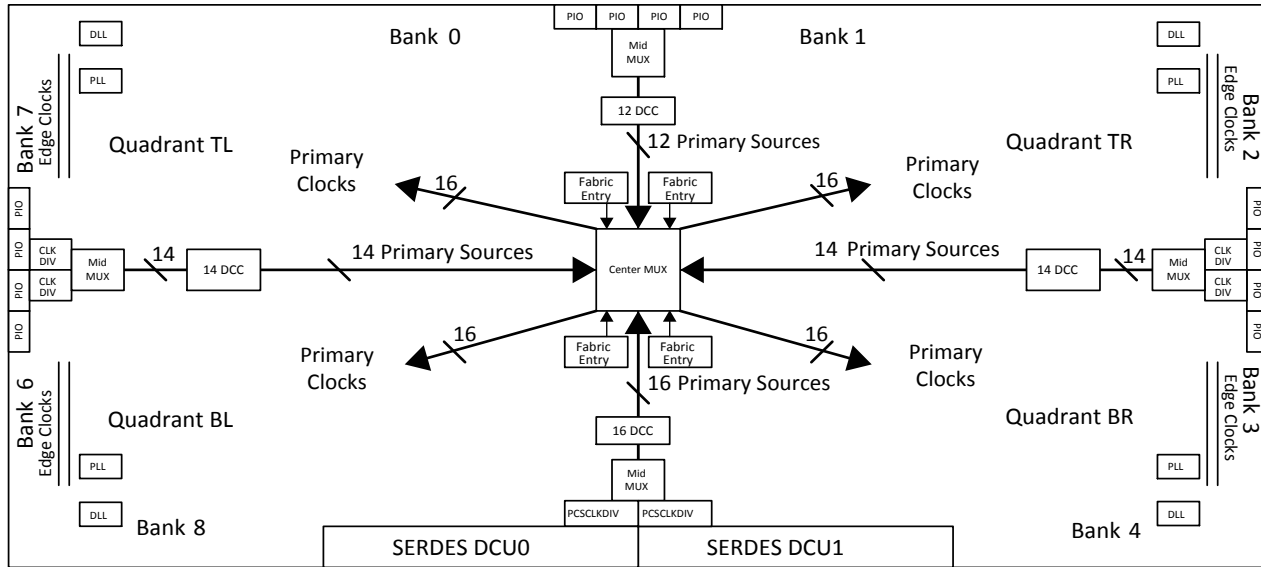


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

### 2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

#### 2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide \(TN1263\)](#).

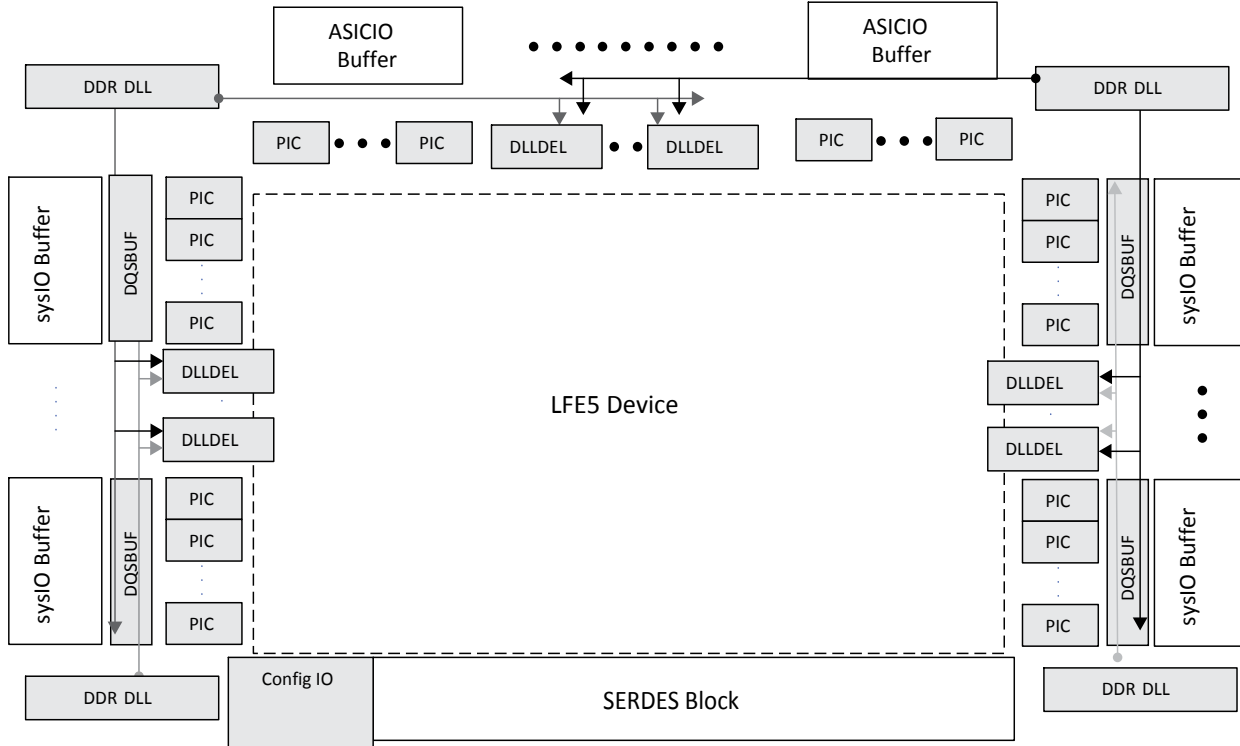


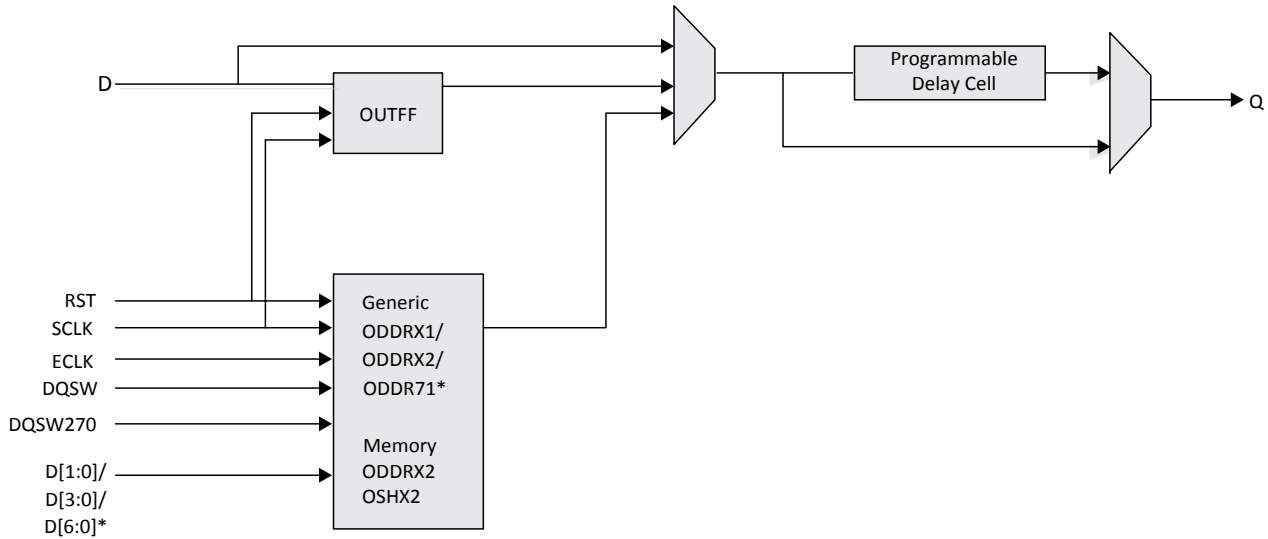
Figure 2.11. ECP5/ECP5-5G DLL Top Level View (For LFE-45 and LFE-85)

## 2.8. sysMEM Memory

ECP5/ECP5-5G devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

### 2.8.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.6 on page 25. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to [ECP5 and ECP5-5G Memory Usage Guide \(TN1264\)](#).



\*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

**Figure 2.20. Output Register Block on Left and Right Sides**

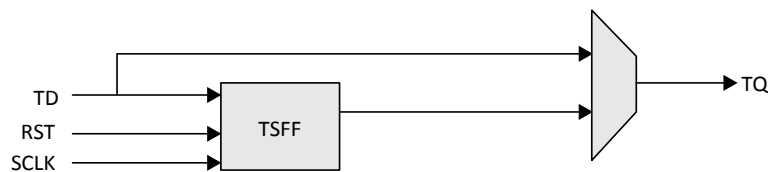
**Table 2.9. Output Block Port Description**

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

## 2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to [ECP5 and ECP5-5G High-Speed I/O Interface \(TN1265\)](#).



**Figure 2.21. Tristate Register Block on Top Side**

## 2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today’s systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTTL, LVPECL, and MIPI.

### 2.14.1. sysI/O Buffer Banks

ECP5/ECP5-5G devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank (Bank 8) is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O. For LFE5-85 devices, there is an additional I/O bank (Bank 4) that is not available in other device in the family.

In ECP5/ECP5-5G devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysI/O bank has its own I/O supply voltage ( $V_{CCIO}$ ). In addition, the banks on the Left and Right sides of the device, have voltage reference input (shared I/O pin),  $V_{REF1}$  per bank, which allow it to be completely independent of each other. The  $V_{REF}$  voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5/ECP5-5G devices, single-ended output buffers and ratioed input buffers (LVTTTL, and LVCMOS) are powered using  $V_{CCIO}$ . LVTTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of  $V_{CCIO}$ .

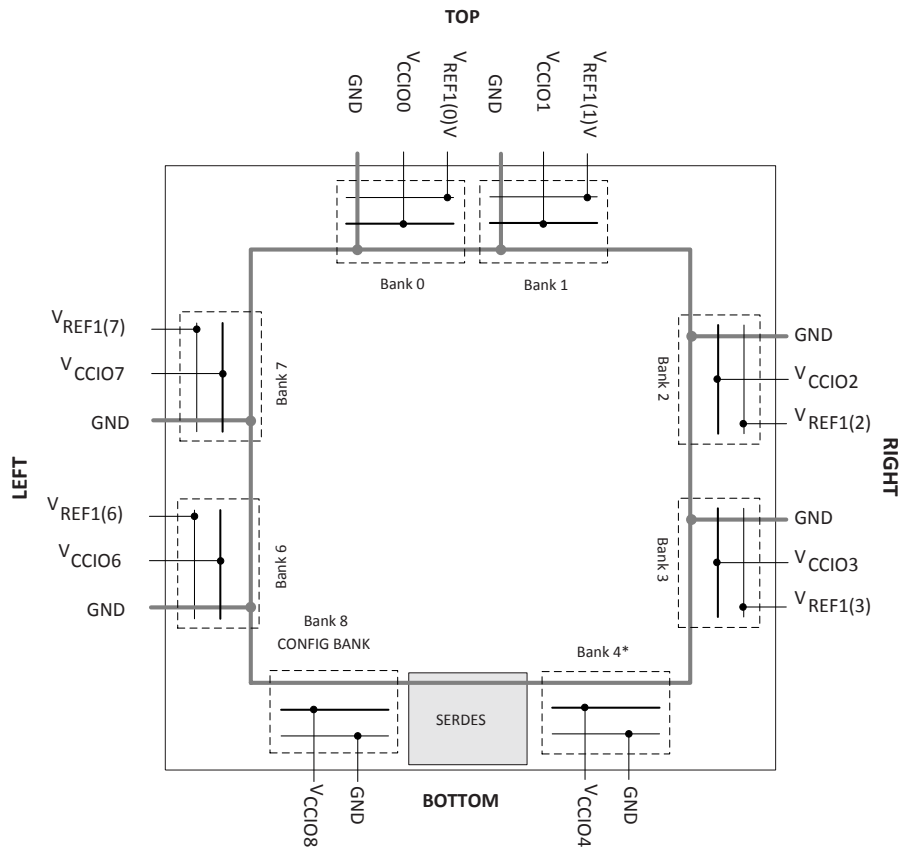


Figure 2.25. ECP5/ECP5-5G Device Family Banks



### 2.14.4. On-Chip Programmable Termination

The ECP5/ECP5-5G devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.

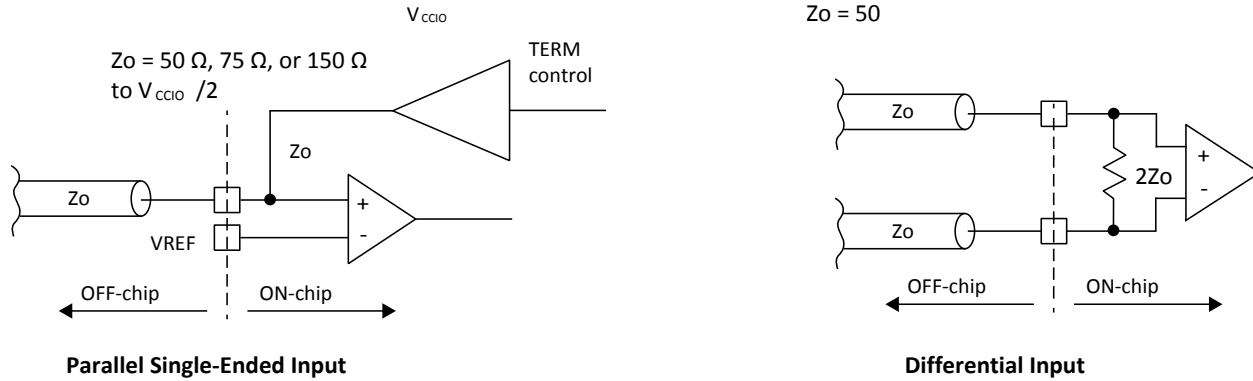


Figure 2.26. On-Chip Termination

See [Table 2.12](#) for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2^*$	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

**\*Notes:**

TERMINATE to  $V_{CCIO}/2$  (Single-Ended) and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to  $V_{CCIO}/2$  and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance  $\pm 20\%$ .

Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for on-chip termination usage and value ranges.

### 2.14.5. Hot Socketing

ECP5/ECP5-5G devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the [Hot Socketing Specifications](#) section on page 48.

### 2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. [Table 2.15](#) lists the allowable combination of primary and secondary protocol combinations.

### 2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

[Table 2.15](#) lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

**Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support**

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to [ECP5 and ECP5-5G SERDES/PCS Usage Guide \(TN1261\)](#).

### 2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to [ECP5 and ECP5-5G sysCONFIG Usage Guide \(TN1260\)](#).

### 3.10. Supply Current (Standby)

Over recommended operating conditions.

**Table 3.8. ECP5/ECP5-5G Supply Current (Standby)**

Symbol	Parameter	Device	Typical	Unit
I <sub>CC</sub>	Core Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F	77	mA
		LFE5UM5G-25F	77	mA
		LFE5U-45F/ LFE5UM-45F	116	mA
		LFE5UM5G-45F	116	mA
		LFE5U-85F/ LFE5UM-85F	212	mA
		LFE5UM5G-85F	212	mA
I <sub>CCAUX</sub>	Auxiliary Power Supply Current	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	16	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	17	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	26	mA
I <sub>CCIO</sub>	Bank Power Supply Current (Per Bank)	LFE5U-12F/ LFE5U-25F/ LFE5UM-25F/ LFE5UM5G-25F	0.5	mA
		LFE5U-45F/ LFE5UM-45F/ LFE5UM5G-45F	0.5	mA
		LFE5U-85F/ LFE5UM-85F/ LFE5UM5G-85F	0.5	mA
I <sub>CCA</sub>	SERDES Power Supply Current (Per Dual)	LFE5UM-25F	11	mA
		LFE5UM5G-25F	12	mA
		LFE5UM-45F	9.5	mA
		LFE5UM5G-45F	11	mA
		LFE5UM-85F	9.5	mA
		LFE5UM5G-85F	11	mA

**Notes:**

- For further information on supply current, see the list of technical documentation in [Supplemental Information](#) section on page 102.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V<sub>CCIO</sub> or GND.
- Frequency 0 Hz.
- Pattern represents a “blank” configuration data file.
- T<sub>j</sub> = 85 °C, power supplies at nominal voltage.
- To determine the ECP5/ECP5-5G peak start-up current, use the Power Calculator tool in the Lattice Diamond Design Software.

3.12. **sysI/O Recommended Operating Conditions**
**Table 3.11. sysI/O Recommended Operating Conditions**

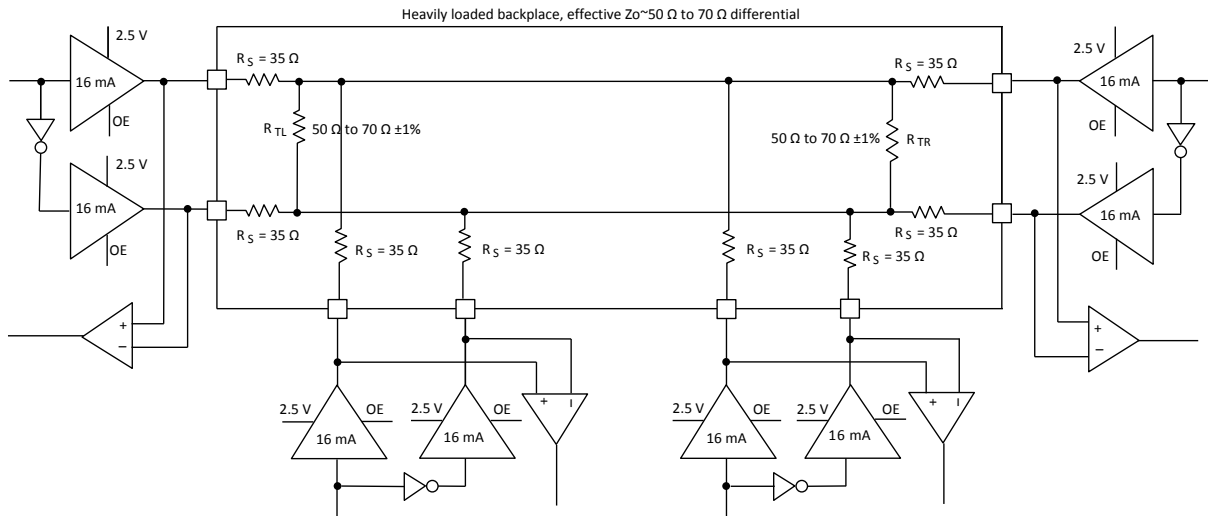
Standard	V <sub>CCIO</sub>			V <sub>REF</sub> (V)		
	Min	Typ	Max	Min	Typ	Max
LVC MOS33 <sup>1</sup>	3.135	3.3	3.465	—	—	—
LVC MOS33D <sup>3</sup> Output	3.135	3.3	3.465	—	—	—
LVC MOS25 <sup>1</sup>	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 <sup>1</sup>	1.14	1.2	1.26	—	—	—
LVTTL33 <sup>1</sup>	3.135	3.3	3.465	—	—	—
SSTL15_I, _II <sup>2</sup>	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II <sup>2</sup>	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II <sup>2</sup>	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12 <sup>2</sup>	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input <sup>3, 5</sup>	1.425	1.5	1.575	—	—	—
LVDS25 <sup>1, 3</sup> Output	2.375	2.5	2.625	—	—	—
subLVDS <sup>3</sup> (Input only)	—	—	—	—	—	—
SLVS <sup>3</sup> (Input only)	—	—	—	—	—	—
LVDS25E <sup>3</sup> Output	2.375	2.5	2.625	—	—	—
MLVDS <sup>3</sup> Output	2.375	2.5	2.625	—	—	—
LVPECL33 <sup>1, 3</sup> Output	3.135	3.3	3.465	—	—	—
BLVDS25 <sup>1, 3</sup> Output	2.375	2.5	2.625	—	—	—
HSULD12D <sup>2, 3</sup>	1.14	1.2	1.26	—	—	—
SSTL135D_I, II <sup>2, 3</sup>	1.28	1.35	1.42	—	—	—
SSTL15D_I, II <sup>2, 3</sup>	1.43	1.5	1.57	—	—	—
SSTL18D_I <sup>1, 2, 3</sup> , II <sup>1, 2, 3</sup>	1.71	1.8	1.89	—	—	—

**Notes:**

1. For input voltage compatibility, refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#).
2. V<sub>REF</sub> is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V<sub>CCAUX</sub> power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to [ECP5 and ECP5-5G sysIO Usage Guide \(TN1262\)](#) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V<sub>IH</sub> and V<sub>IL</sub>. It can also be implemented as LVC MOS12 with VCCIO at 1.2V, which would meet V<sub>IH</sub>/V<sub>IL</sub> spec on LVC MOS12.

### 3.14.7. MLVDS25

The ECP5/ECP5-5G devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.



**Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)**

**Table 3.17. MLVDS25 DC Conditions**

Parameter	Description	Typical		Unit
		Zo=50 Ω	Zo=70 Ω	
V <sub>CCIO</sub>	Output Driver Supply (±5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
R <sub>S</sub>	Driver Series Resistor (±1%)	35.00	35.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
R <sub>TR</sub>	Receiver Termination (±1%)	50.00	70.00	Ω
V <sub>OH</sub>	Output High Voltage	1.52	1.60	V
V <sub>OL</sub>	Output Low Voltage	0.98	0.90	V
V <sub>OD</sub>	Output Differential Voltage	0.54	0.70	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	21.74	20.00	mA

**Note:** For input buffer, see LVDS Table 3.13 on page 55.

### 3.14.8. SLVS

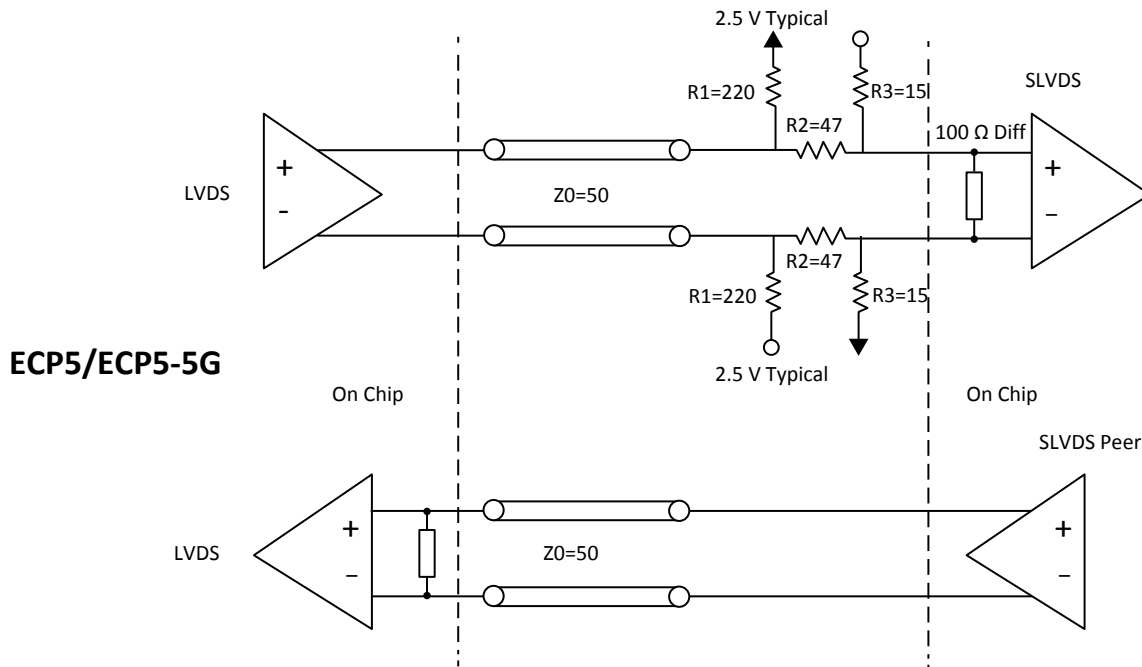
Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The ECP5/ECP5-5G devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5/ECP5-5G LVDS input parameters, as listed in Table 3.18.

**Table 3.18. Input to SLVS**

Parameter	ECP5/ECP5-5G LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5/ECP5-5G does not support SLVS output. However, SLVS output can be created using ECP5/ECP5-5G LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted external to meet SLVS levels.



**Figure 3.5. SLVS Interface**

### 3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

**Table 3.23. sysCLOCK PLL Timing**

Parameter	Descriptions	Conditions	Min	Max	Units
$f_{IN}$	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
$f_{OUT}$	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
$f_{VCO}$	PLL VCO Frequency	—	400	800	MHz
$f_{PFD}^3$	Phase Detector Input Frequency	—	10	400	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle	—	45	55	%
$t_{PH4}$	Output Phase Accuracy	—	-5	5	%
$t_{OPJIT}^1$	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
$t_{SPO}$	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
$t_W$	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
$t_{LOCK}^2$	PLL Lock-in Time	—	—	15	ms
$t_{UNLOCK}$	PLL Unlock Time	—	—	50	ns
$t_{IPJIT}$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{HI}$	Input Clock High Time	90% to 90%	0.5	—	ns
$t_{LO}$	Input Clock Low Time	10% to 10%	0.5	—	ns
$t_{RST}$	RST/ Pulse Width	—	1	—	ms
$t_{RSTREC}$	RST Recovery Time	—	1	—	ns
$t_{LOAD\_REG}$	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain "0" or	—	4	—	VCO cycles

**Notes:**

- Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
- Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
- Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PFD} > 10$  MHz. For  $f_{PFD} < 10$  MHz, the jitter numbers may not be met in certain conditions.

### 3.25.2. PCIe (5 Gb/s) – Preliminary AC and DC Characteristics

Over recommended operating conditions.

**Table 3.31. PCIe (5 Gb/s)**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
<b>Transmit<sup>1</sup></b>						
UI	Unit Interval	—	199.94	200	200.06	ps
B <sub>WTX-PKG-PLL2</sub>	Tx PLL bandwidth corresponding to PKGTX-PLL2	—	5	—	16	MHz
P <sub>KGTX-PLL2</sub>	Tx PLL Peaking	—	—	—	1	dB
V <sub>TX-DIFF-PP</sub>	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
V <sub>TX-DIFF-PP-LOW</sub>	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p
V <sub>TX-DE-RATIO-3.5dB</sub>	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
V <sub>TX-DE-RATIO-6dB</sub>	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
T <sub>MIN-PULSE</sub>	Instantaneous lone pulse width	—	—	—	—	UI
T <sub>TX-RISE-FALL</sub>	Transmitter rise and fall time	—	—	—	—	UI
T <sub>TX-EYE</sub>	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T <sub>TX-DJ</sub>	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T <sub>TX-RJ</sub>	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
T <sub>RF-MISMATCH</sub>	Tx rise/fall time mismatch	—	—	—	—	UI
R <sub>LTX-DIFF</sub>	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R <sub>LTX-CM</sub>	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
Z <sub>TX-DIFF-DC</sub>	DC differential Impedance	—	—	—	120	Ω
V <sub>TX-CM-AC-PP</sub>	Tx AC peak common mode voltage, peak-peak	—	—	—	—	mV, p-p
I <sub>TX-SHORT</sub>	Transmitter short-circuit current	—	—	—	90	mA
V <sub>TX-DC-CM</sub>	Transmitter DC common-mode voltage	—	0	—	1.2	V
V <sub>TX-IDLE-DIFF-DC</sub>	Electrical Idle Output DC voltage	—	0	—	5	mV
V <sub>TX-IDLE-DIFF-AC-p</sub>	Electrical Idle Differential Output peak voltage	—	—	—	—	mV
V <sub>TX-RCV-DETECT</sub>	Voltage change allowed during Receiver Detect	—	—	—	600	mV
T <sub>TX-IDLE-MIN</sub>	Min. time in Electrical Idle	—	20	—	—	ns
T <sub>TX-IDLE-SET-TO-IDLE</sub>	Max. time from EI Order Set to valid Electrical Idle	—	—	—	8	ns
T <sub>TX-IDLE-TO-DIFF-DATA</sub>	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
L <sub>TX-SKEW</sub>	Lane-to-lane output skew	—	—	—	—	ps



## 3.27. XAUI/CPRI LV E.30 Electrical and Timing Characteristics

### 3.27.1. AC and DC Characteristics

Over recommended operating conditions.

**Table 3.33. Transmit**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$T_{RF}$	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	$\Omega$
$J_{TX\_DDJ}^{2,3}$	Output data deterministic jitter	—	—	—	0.17	UI
$J_{TX\_TJ}^{1,2,3}$	Total output data jitter	—	—	—	0.35	UI

**Notes:**

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50  $\Omega$  impedance (100  $\Omega$  differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Over recommended operating conditions.

**Table 3.34. Receive and Jitter Tolerance**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$RL_{RX\_DIFF}$	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
$RL_{RX\_CM}$	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
$Z_{RX\_DIFF}$	Differential termination resistance	—	80	100	120	$\Omega$
$J_{RX\_DJ}^{1,2,3}$	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
$J_{RX\_RJ}^{1,2,3}$	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
$J_{RX\_SJ}^{1,2,3}$	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
$J_{RX\_TJ}^{1,2,3}$	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
$T_{RX\_EYE}$	Receiver eye opening	—	0.35	—	—	UI

**Notes:**

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50  $\Omega$  impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

## 3.28. CPRI LV E.24/SGMII(2.5Gbps) Electrical and Timing Characteristics

### 3.28.1. AC and DC Characteristics

**Table 3.35. Transmit**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$T_{RF}^1$	Differential rise/fall time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance	—	80	100	120	$\Omega$
$J_{TX\_DDJ}^{3,4}$	Output data deterministic jitter	—	—	—	0.17	UI
$J_{TX\_TJ}^{2,3,4}$	Total output data jitter	—	—	—	0.35	UI

**Notes:**

1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50  $\Omega$  impedance (100  $\Omega$  differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

### 3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

#### 3.30.1. AC and DC Characteristics

**Table 3.39. Transmit**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR <sub>SDO</sub>	Serial data rate	—	270	—	2975	Mb/s
T <sub>JALIGNMENT</sub> <sup>2</sup>	Serial output jitter, alignment	270 Mb/s <sup>6</sup>	—	—	0.2	UI
T <sub>JALIGNMENT</sub> <sup>2</sup>	Serial output jitter, alignment	1485 Mb/s	—	—	0.2	UI
T <sub>JALIGNMENT</sub> <sup>1, 2</sup>	Serial output jitter, alignment	2970 Mb/s	—	—	0.3	UI
T <sub>JTIMING</sub>	Serial output jitter, timing	270 Mb/s <sup>6</sup>	—	—	0.2	UI
T <sub>JTIMING</sub>	Serial output jitter, timing	1485 Mb/s	—	—	1	UI
T <sub>JTIMING</sub>	Serial output jitter, timing	2970 Mb/s	—	—	2	UI

**Notes:**

1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice SERDES device configured to 50 Ω output impedance connecting to the external cable driver with differential signaling.
4. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mb/s.
5. All LFE5UM/LFE5UM5G devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.
6. 270 Mb/s is supported with Rate Divider only.

**Table 3.40. Receive**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR <sub>SDI</sub>	Serial input data rate	—	270	—	2970	Mb/s

**Table 3.41. Reference Clock**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F <sub>VCLK</sub>	Video output clock frequency	—	54	—	148.5	MHz
DC <sub>v</sub>	Duty cycle, video clock	—	45	50	55	%

**Note:** SD-SDI (270 Mb/s) is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

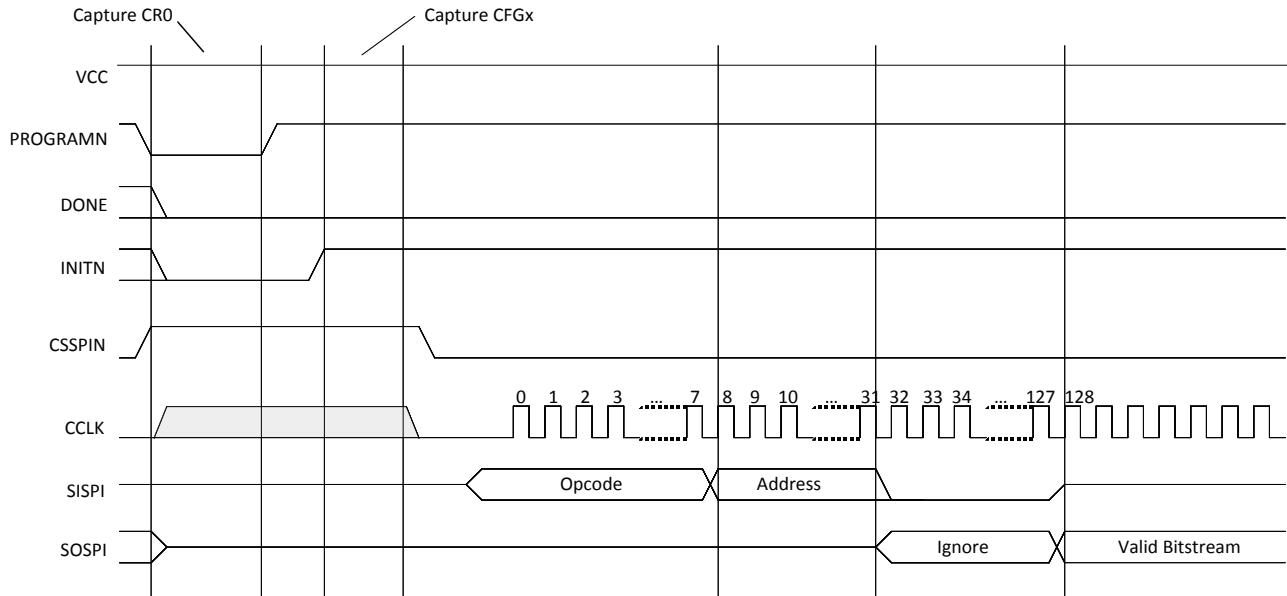


Figure 3.22. Master SPI Configuration Waveforms

### 3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.43. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
$f_{MAX}$	TCK clock frequency	—	25	MHz
$t_{BTCPH}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{BTCPL}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{BTS}$	TCK [BSCAN] setup time	10	—	ns
$t_{BTH}$	TCK [BSCAN] hold time	8	—	ns
$t_{BTRF}$	TCK [BSCAN] rise/fall time	50	—	mV/ns
$t_{BTCO}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{BTCOEN}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{BTCRS}$	BSCAN test capture register setup time	8	—	ns
$t_{BTCRH}$	BSCAN test capture register hold time	25	—	ns
$t_{BUTCO}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

## 4. Pinout Information

### 4.1. Signal Descriptions

Signal Name	I/O	Description
<b>General Purpose</b>		
P[L/R] [Group Number]_[A/B/C/D]	I/O	<p>[L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group.</p> <p>[A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration.</p> <p>PIO A and B are grouped as a pair, and PIO C and D are group as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer.</p> <p>Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω.</p>
P[T/B][Group Number]_[A/B]	I/O	<p>[T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tristated and default to have pull-down enabled after configuration.</p> <p>PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer.</p> <p>PIO A/B forms a pair of emulated differential output buffer.</p>
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V <sub>CC</sub>	—	Power supply pins for core logic. Dedicated pins. V <sub>CC</sub> = 1.1 V (ECP5), 1.2 V (ECP5UM5G)
V <sub>CCAUX</sub>	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. V <sub>CCAUX</sub> = 2.5 V.
V <sub>CCIOx</sub>	—	Dedicated power supply pins for I/O bank x. V <sub>CCIO8</sub> is used for configuration and JTAG.
VREF1_x	—	Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as VREF1 input. When not used, they may be used as I/O pins.
<b>PLL, DLL and Clock Functions</b>		
[LOC]_[GPLL][T, C]_IN	I	General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not configured as GPLL input pads, they can be used as general purpose I/O pins.
GR_PCLK[Bank][num]	I	General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to <a href="#">ECP5 sysClock PLL/DLL Design and Usage Guide (TN1263)</a> . These pins are shared I/O pins. When not configured as GR pins, they can be used as general purpose I/O pins.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/O pins. When not configured as PCLK pins, they can be used as general purpose I/O pins.

## 5. Ordering Information

### 5.1. ECP5/ECP5-5G Part Number Description

