Lattice Semiconductor Corporation - LFE5UM5G-85F-8BG554I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	259
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	554-FBGA
Supplier Device Package	554-CABGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um5g-85f-8bg554i

Figures

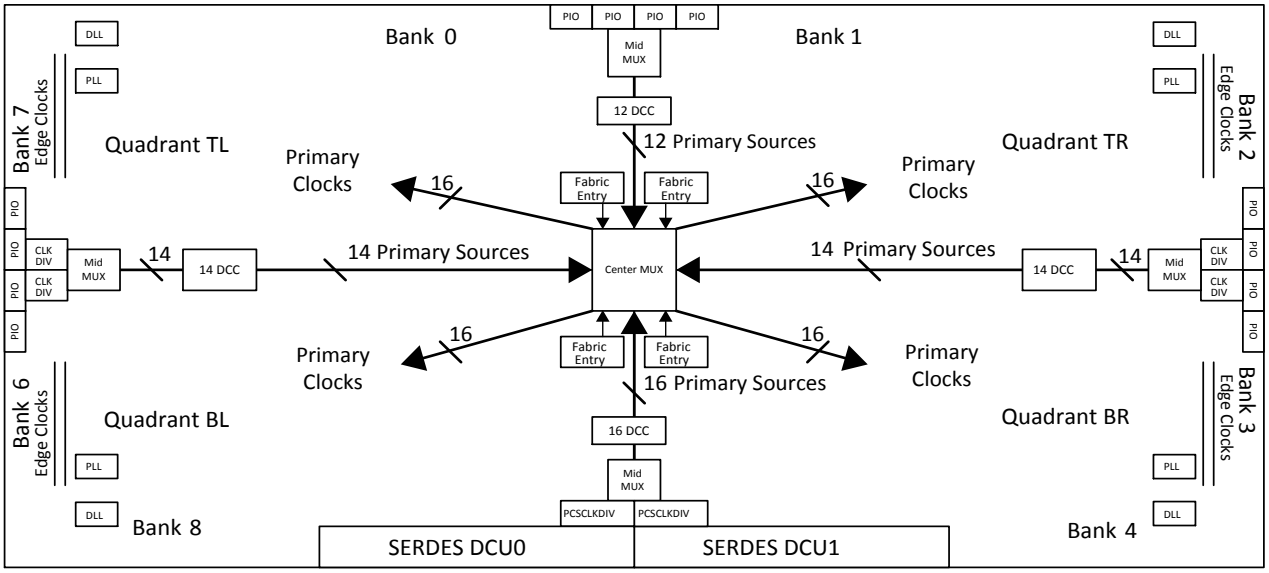


Figure 2.6. LFE5UM/LFE5UM5G-85 Clocking

2.5.1. Primary Clocks

The ECP5/ECP5-5G device family provides low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5/ECP5-5G device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5/ECP5-5G fabric. These routing muxes are shown in Figure 2.6. Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5/ECP5-5G Device. For more information about the primary clock tree and connections, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5.1.1. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

- 5*5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14, the ECP5/ECP5-5G sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5/ ECP5-5G sysDSP slice. Figure 2.14 shows the diagram of sysDSP, and Figure 2.15 shows the detailed diagram.

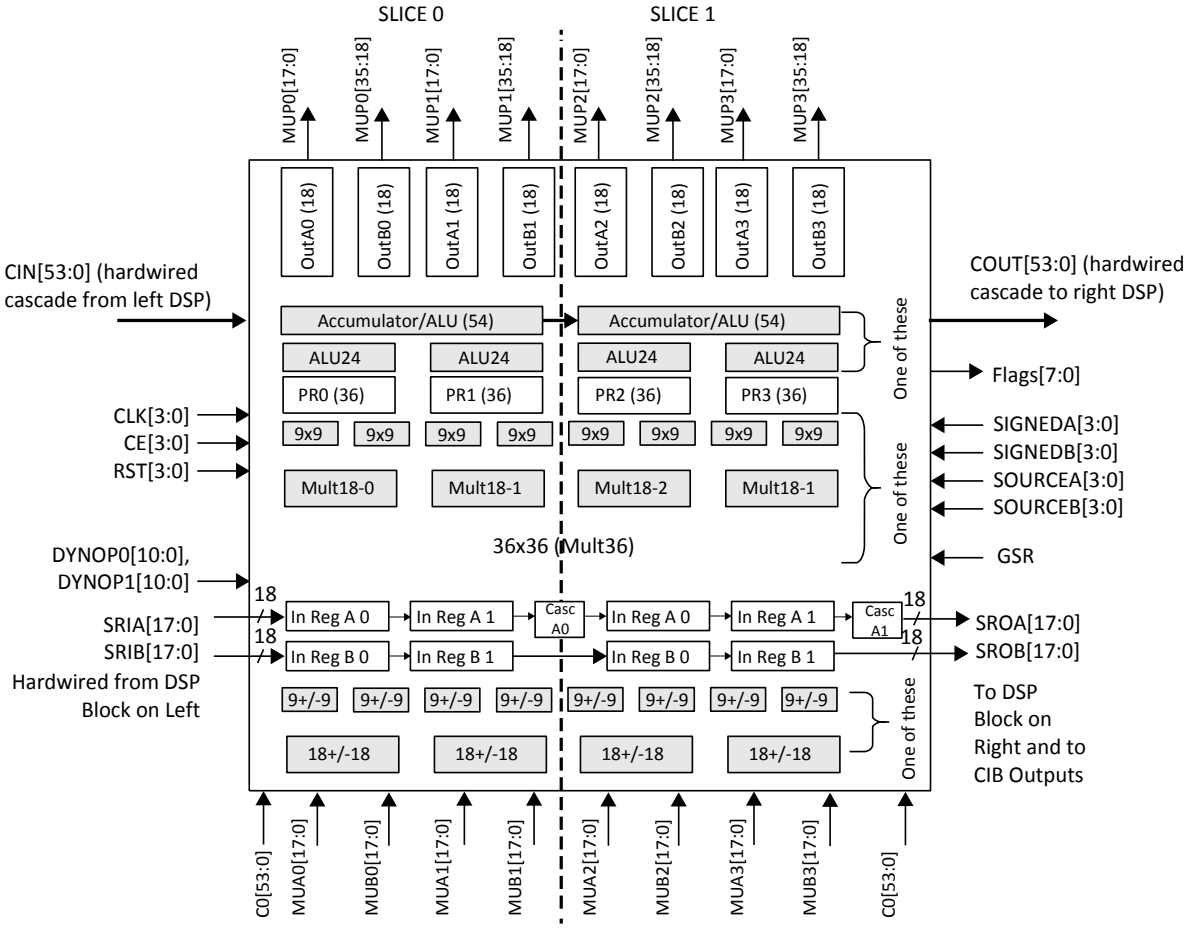


Figure 2.14. Simplified sysDSP Slice Block Diagram

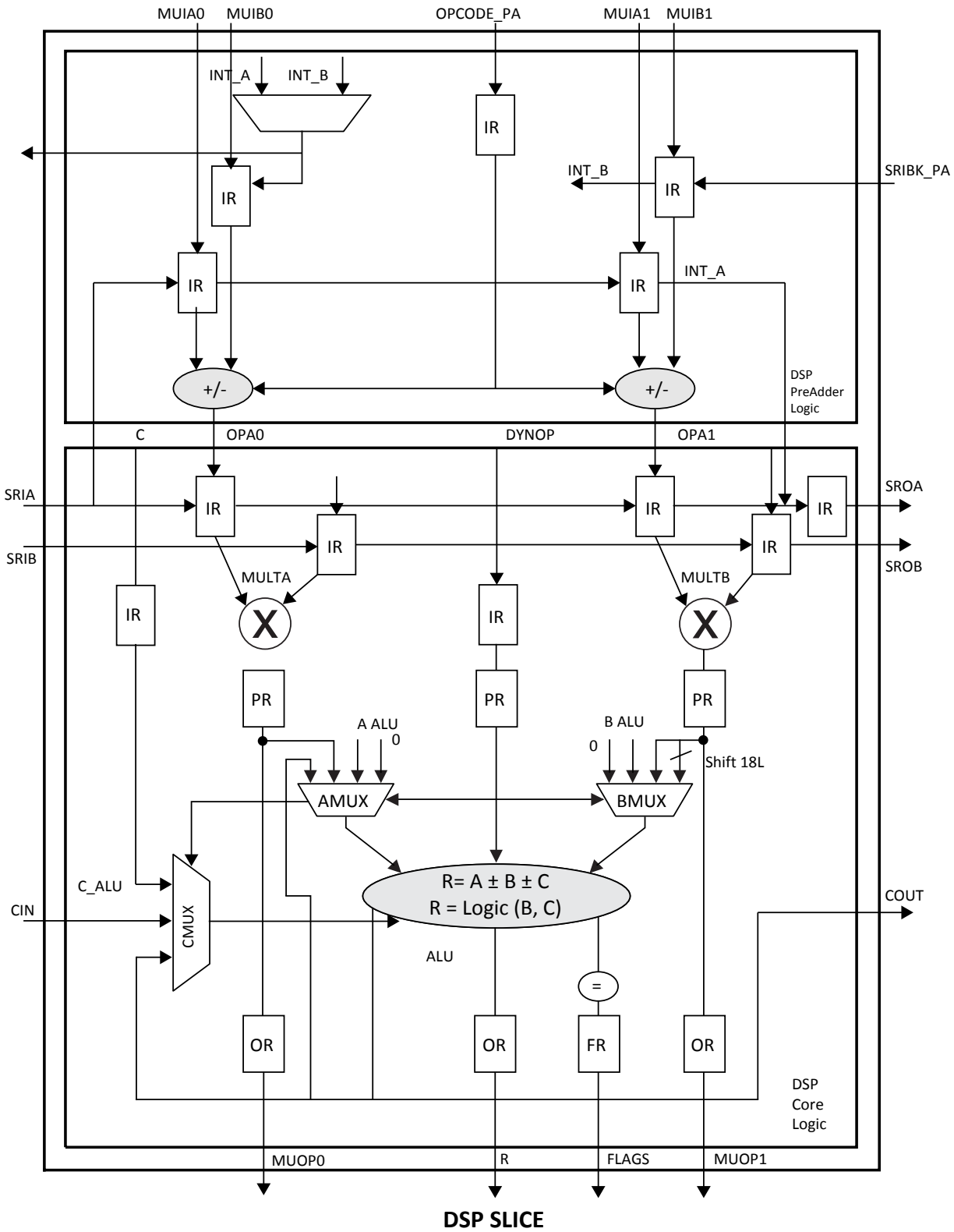
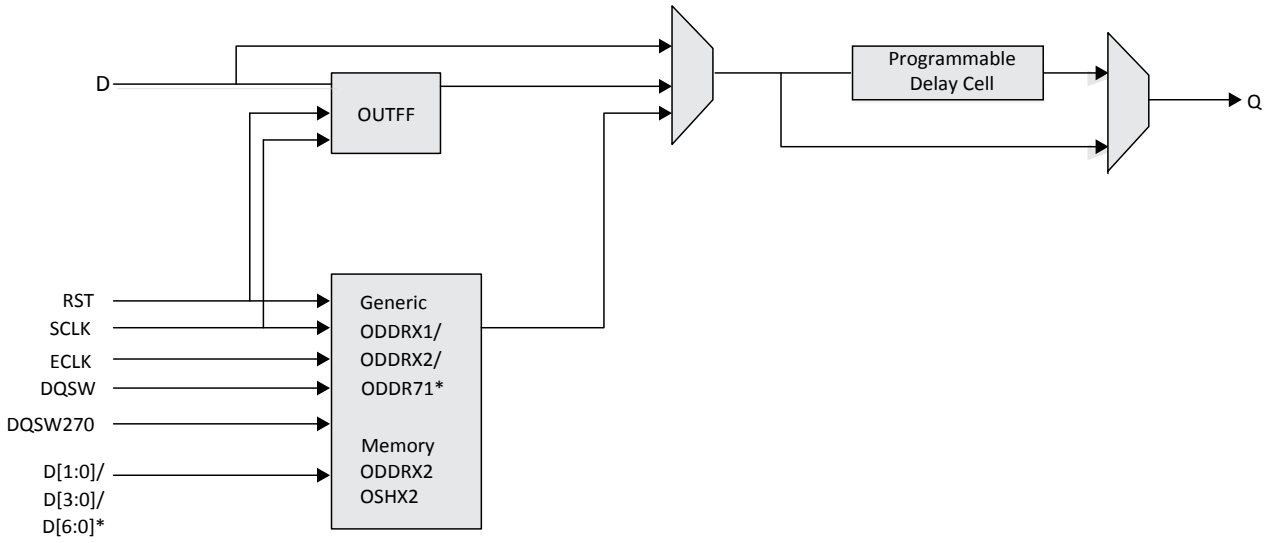


Figure 2.15. Detailed sysDSP Slice Diagram



*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).

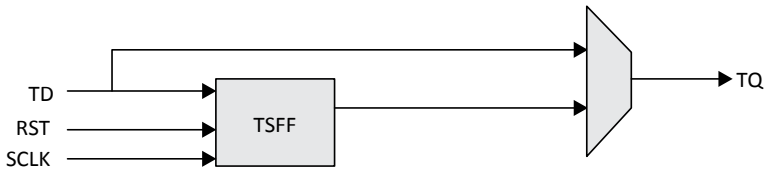


Figure 2.21. Tristate Register Block on Top Side

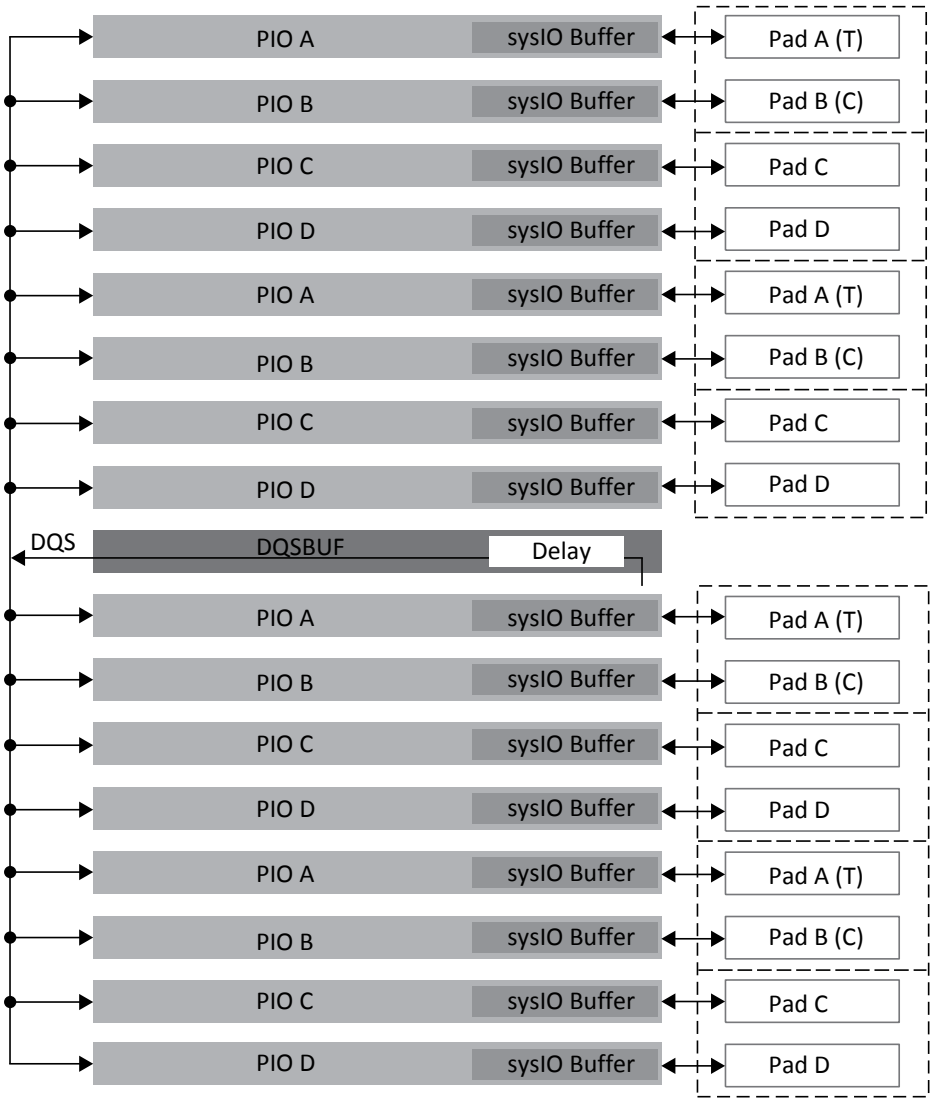


Figure 2.23. DQS Grouping on the Left and Right Edges

2.13.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces (DDR2/3, LPDDR2/3), the DQS strobe signal from the memory must be used to capture the data (DQ) in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifted is achieved by using DQSDEL programmable delay line in the DQS Delay Block (DQS read circuit). The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read and write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block shown in Figure 2.24 generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTL, LVPECL, and MIPI.

2.14.1. sysI/O Buffer Banks

ECP5/ECP5-5G devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank (Bank 8) is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O. For LFE5-85 devices, there is an additional I/O bank (Bank 4) that is not available in other device in the family.

In ECP5/ECP5-5G devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, the banks on the Left and Right sides of the device, have voltage reference input (shared I/O pin), VREF1 per bank, which allow it to be completely independent of each other. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5/ECP5-5G devices, single-ended output buffers and ratioed input buffers (LVTTL, and LVCMOS) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

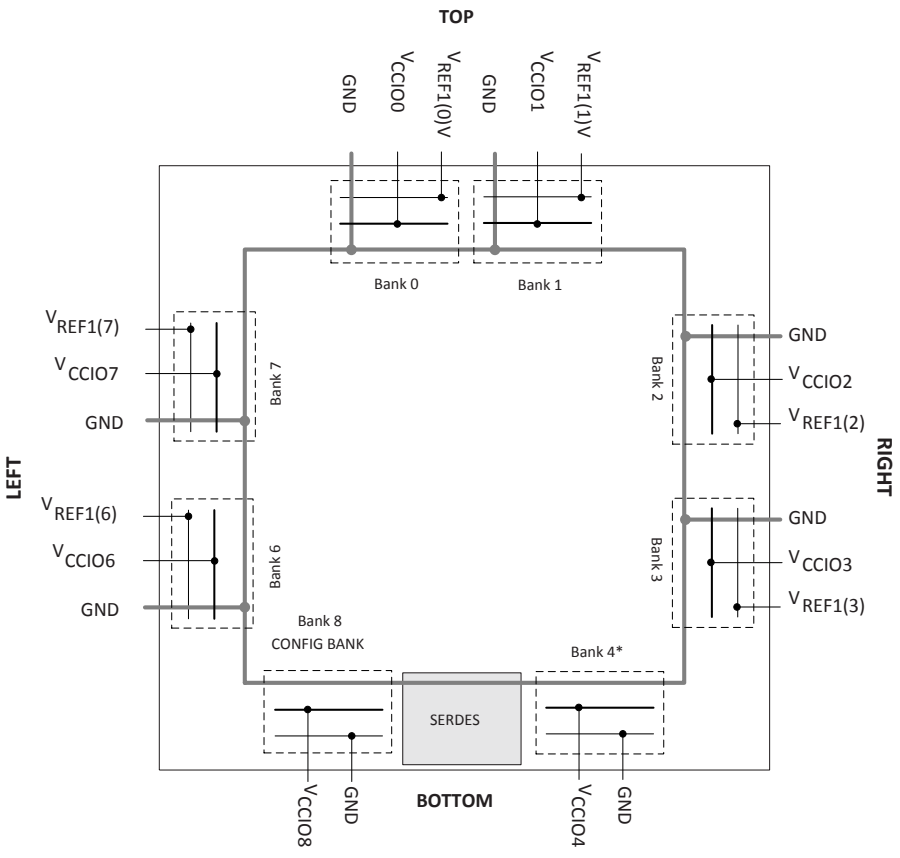


Figure 2.25. ECP5/ECP5-5G Device Family Banks

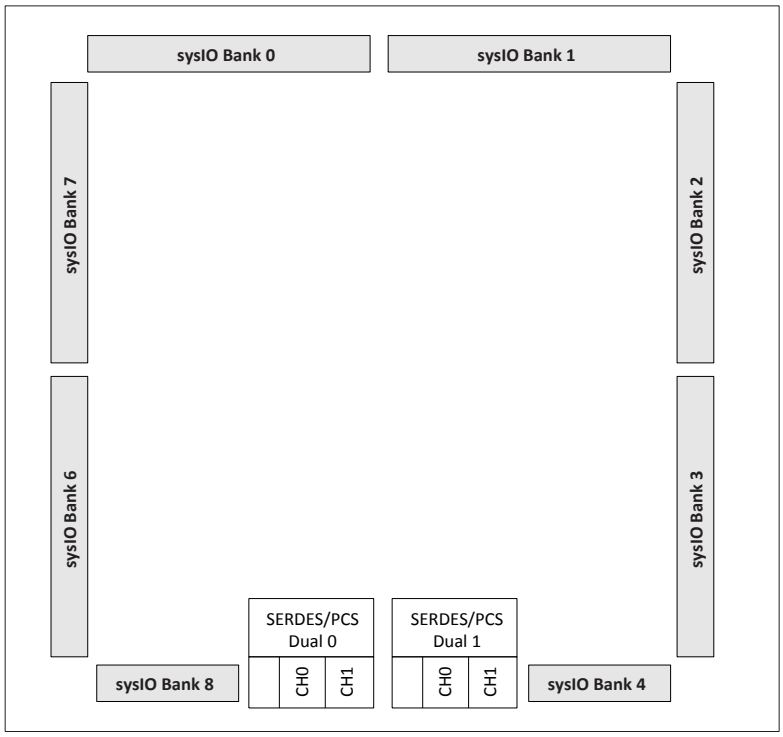


Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0 2.02	2500	x1, x2, x4	8b10b
	5000 [2]	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 [2]	x1	8b10b
SD-SDI (259M, 344M) [1]	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	—	—
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.
2. For ECP5-5G family devices only.

2.15.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration thru this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), with two duals (Four SERDES channels and PCS) and some additional logic from the core.

The LFE5UM/LFE5UM5G devices support a wide range of protocols. Within the same dual, the LFE5UM/ LFE5UM5G devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2.15 lists the allowable combination of primary and secondary protocol combinations.

2.16. Flexible Dual SERDES Architecture

The LFE5UM/LFE5UM5G SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual (consisting of two SERDES channels) is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LFE5UM/LFE5UM5G dual-channel architecture provides flexibility; more than one standard can be supported within the same dual.

Table 2.15 lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LFE5UM/LFE5UM5G Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LFE5UM/LFE5UM5G architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).

2.17. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5/ECP5-5G devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses VCCIO8 for power supply.

For more information, refer to ECP5 and ECP5-5G sysCONFIG Usage Guide (TN1260).

3.7. Hot Socketing Requirements

Table 3.6. Hot Socketing Requirements

Description	Min	Typ	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA
Input current per HDIN pin when device power supply is off, inputs driven[1, 2]	—	—	15	mA
Current per HDIN pin when device power ramps up, input driven[3]	—	—	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up[4]	—	—	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, no external AC coupling.
2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.
3. Device power supplies are ramping up (V_{CCA} and V_{CCAUX}), both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V_{CCHTX}, 8b/10b data, internal AC coupling.
4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to V_{CCHTX} by the far end receiver termination of 50 Ω single ended.

3.8. ESD Performance

Refer to the ECP5 and ECP5-5G Product Family Qualification Summary for complete qualification data, including ESD performance.

3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4]	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{CCIO}$	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	$V_{CCIO} < V_{IN} \le V_{IH(MAX)}$	—	—	100	µA
I_{PU}	I/O Active Pull-up Current, sustaining logic HIGH state	$0.7\ V_{CCIO} \le V_{IN} \le V_{CCIO}$	–30	—	—	µA
	I/O Active Pull-up Current, pulling down from logic HIGH state	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	—	—	–150	µA
I_{PD}	I/O Active Pull-down Current, sustaining logic LOW state	$0 \le V_{IN} \le V_{IL}$ (MAX)	30	—	—	µA
	I/O Active Pull-down Current, pulling up from logic LOW state	$0 \le V_{IN} \le V_{CCIO}$	—	—	150	µA
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to $V_{IH(MAX)}$	—	5	8	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to $V_{IH(MAX)}$	—	5	7	pf
V_{HYST}	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V	—	300	—	mV
		V_{CCIO} = 2.5 V	—	250	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as V_{REF}, maximum leakage= 25 µA.

3.12. sysI/O Recommended Operating Conditions

Table 3.11. sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3, 5]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
5. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.13. sysI/O Single-Ended DC Electrical Characteristics

Table 3.12. Single-Ended DC Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33	–0.3	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	16, 12, 8, 4	–16, –12, –8, –4
LVCMOS25	–0.3	0.7	1.7	3.465	0.4	V_{CCIO} – 0.4	12, 8, 4	–12, –8, –4
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	12, 8, 4	–12, –8, –4
LVCMOS15	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	8, 4	–8, –4
LVCMOS12	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	8, 4	–8, –4
LVTTL33	–0.3	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	16, 12, 8, 4	–16, –12, –8, –4
SSTL18_I (DDR2 Memory)	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.465	0.4	V_{CCIO} – 0.4	6.7	–6.7
SSTL18_II	–0.3	V_{REF} –	V_{REF} + 0.125	3.465	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL15 _I (DDR3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.31	V_{CCIO} – 0.31	7.5	–7.5
SSTL15_II (DDR3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.31	V_{CCIO} – 0.31	8.8	–8.8
SSTL135_I (DDR3L Memory)	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	3.465	0.27	V_{CCIO} – 0.27	7	–7
SSTL135_II (DDR3L Memory)	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	3.465	0.27	V_{CCIO} – 0.27	8	–8
MIPI D-PHY (LP)[3]	–0.3	0.55	0.88	3.465	—	—	—	—
HSUL12 (LPDDR2/3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.3	V_{CCIO} – 0.3	4	–4

Notes:

1. For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O (All I/Os used in the same V_{CCIO}).
2. Not all IO types are supported in all banks. Refer to ECP5 and ECP5-5G sysIO Usage Guide (TN1262) for details.
3. MIPI D-PHY LP input can be implemented by powering VCCIO to 1.5V, and select MIPI LP primitive to meet MIPI Alliance spec on V_{IH} and V_{IL}. It can also be implemented as LVCMOS12 with VCCIO at 1.2V, which would meet V_{IH}/V_{IL} spec on LVCOM12.

3.17. Maximum I/O Buffer Speed

Over recommended operating conditions.

Table 3.21. ECP5/ECP5-5G Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
MIPI D-PHY (HS Mode)	MIPI Video	400	MHz
SLVS	SLVS similar to MIPI	400	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL_12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	200	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	200	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	200	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	200	MHz
LVCMOS15	LVCMOS 1.5, V_{CCIO} = 1.5 V	200	MHz
LVCMOS12	LVCMOS 1.2, V_{CCIO} = 1.2 V	200	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	150	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	150	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, VCCIO = 3.3 V	150	MHz
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	150	MHz
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	150	MHz
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	150	MHz
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	150	MHz
LVCMOS12 (For all drives)	LVCMOS, 1.2 V	150	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Switching Test Conditions, Table 3.44 on page 90.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

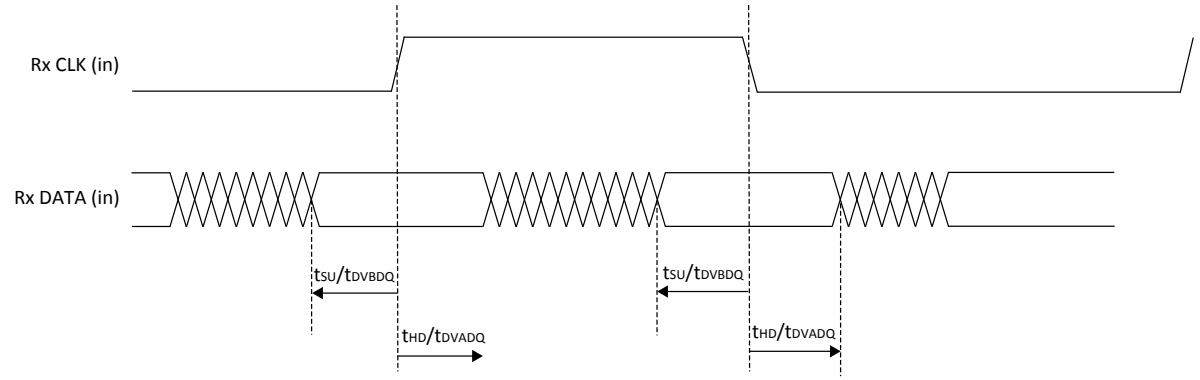


Figure 3.6. Receiver RX.CLK.Centered Waveforms

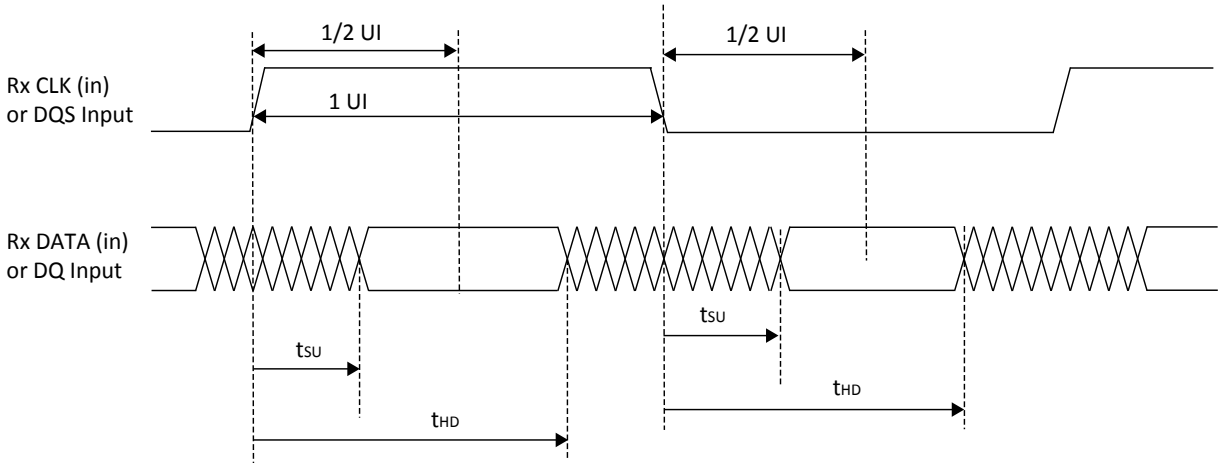


Figure 3.7. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

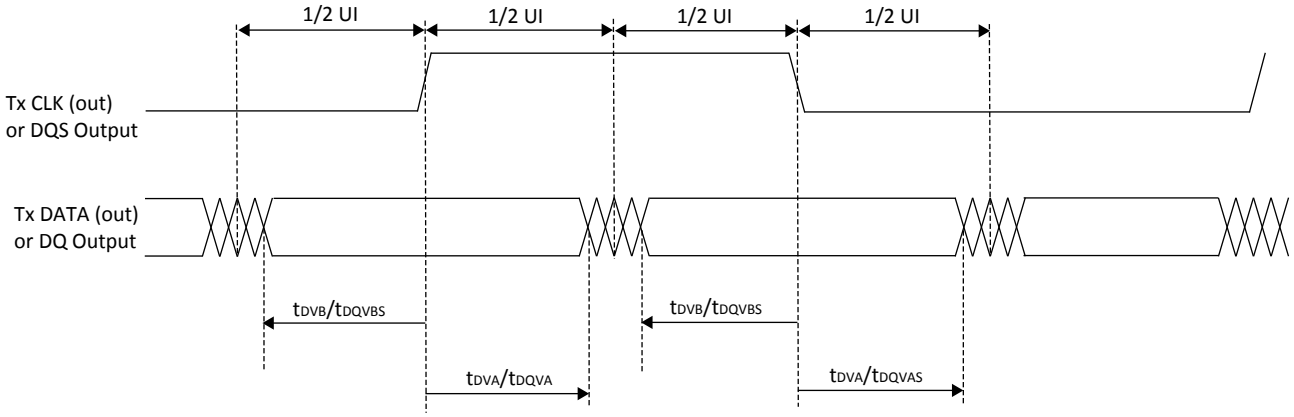


Figure 3.8. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

3.20. SERDES High-Speed Data Transmitter

Table 3.24. Serial Output Timing and Levels

Symbol	Description	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Peak-Peak Differential voltage on selected amplitude[1, 2]	–25%	—	25%	mV, p-p
$V_{TX-CM-DC}$	Output common mode voltage	—	V_{CCHTX} / 2	—	mV, p-p
T_{TX-R}	Rise time (20% to 80%)	50	—	—	ps
T_{TX-F}	Fall time (80% to 20%)	50	—	—	ps
$T_{TX-CM-AC-P}$	RMS AC peak common-mode output voltage	—	—	20	mV
Z_{TX_SE}	Single ended output impedance for 50/75 Ω	–20%	50/75	20%	Ω
	Single ended output impedance for 6K Ω	–25%	6K	25%	Ω
RL_{TX_DIFF}	Differential return loss (with package included) [3]	—	—	–10	dB
RL_{TX_COM}	Common mode return loss (with package included) [3]	—	—	–6	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at V_{CCHTX}±5%.
2. Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for settings of Tx amplitude.
3. Return los = −10 dB (differential), –6 dB (common mode) for 100 MHz ≤ f <= 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

Table 3.25. Channel Output Jitter

Description	Frequency	Min	Typ	Max	Unit
Deterministic	5 Gb/s	—	—	TBD	UI, p-p
Random	5 Gb/s	—	—	TBD	UI, p-p
Total	5 Gb/s	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	—	—	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	—	—	0.24	UI, p-p

Notes:

1. Values are measured with PRBS 2^7-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.
2. For ECP5-5G family devices only.

3.22. SERDES High-Speed Data Receiver

Table 3.27. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss (without package)	—	—	–10	dB

Notes:
1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5, and 1.76 for ECP5-5G.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.28. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	5 Gb/s	400 mV differential eye	—	—	TBD	UI, p-p
Random		400 mV differential eye	—	—	TBD	UI, p-p
Total		400 mV differential eye	—	—	TBD	UI, p-p
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Notes:
1. Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.
2. For ECP5-5G family devices only.

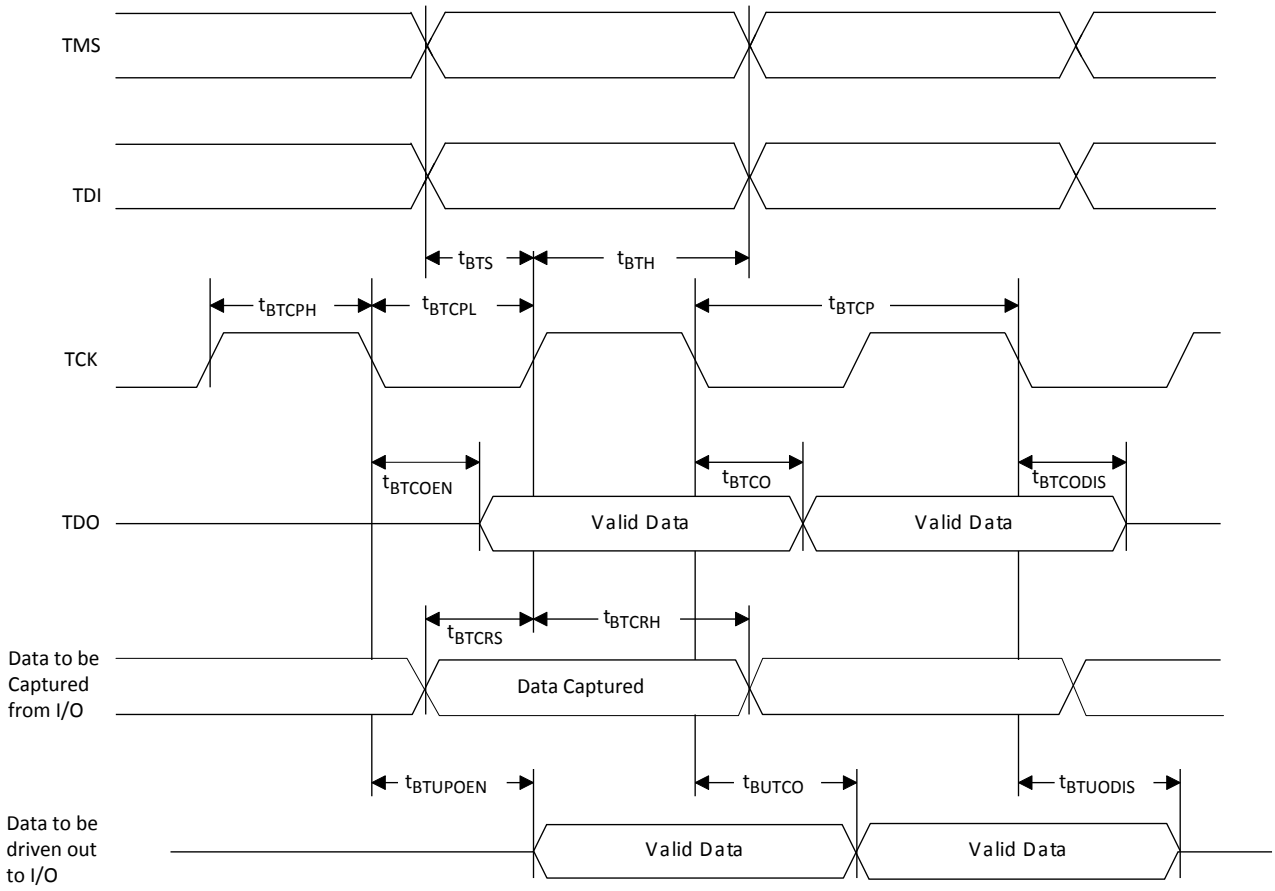
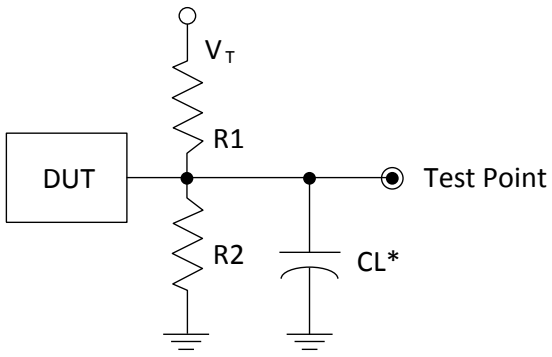


Figure 3.23. JTAG Port Timing Waveforms

3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.44.



*CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards

Pin Information Summary		LFE5UM/ LFE5UM5G-25		LFE5UM/LFE5UM5G-45			LFE5UM/LFE5UM5G-85			
Pin Type		285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA
TAP		4	4	4	4	4	4	4	4	4
Miscellaneous Dedicated Pins		7	7	7	7	7	7	7	7	7
GND		83	59	83	59	113	83	59	113	166
NC		1	8	1	2	33	1	0	17	29
Reserved		0	2	0	2	4	0	2	4	4
SERDES		14	28	14	28	28	14	28	28	28
VCCA (SERDES)	VCCA0	2	2	2	2	6	2	2	6	8
	VCCA1	0	2	0	2	6	0	2	6	9
VCCAUX (SERDES)	VCCAUXA0	2	2	2	2	2	2	2	2	2
	VCCAUXA1	0	2	0	2	2	0	2	2	2
GNDA (SERDES)		26	26	26	26	49	26	26	49	60
Total Balls		285	381	285	381	554	285	381	554	756
High Speed Differential Input / Output Pairs	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	10/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8	24/12
	Bank 3	14/7	16/8	14/7	16/8	24/12	14/7	16/8	24/12	32/16
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	13/6	16/8	13/6	16/8	24/12	13/6	16/8	24/12	32/16
	Bank 7	8/6	16/8	8/6	16/8	16/8	8/6	16/8	16/8	24/12
	Bank 8	0	0	0	0	0	0	0	0	0
Total High Speed Differential I/O Pairs		45/2	64/32	45/27	64/3	80/40	45/27	65/3	80/40	112/5
DQS Groups (> 11 pins in group)	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	1	2	1	2	2	1	2	2	3
	Bank 3	2	2	2	2	3	2	2	3	4
	Bank 4	0	0	0	0	0	0	0	0	0
	Bank 6	2	2	2	2	3	2	2	3	4
	Bank 7	1	2	1	2	2	1	2	2	3
	Bank 8	0	0	0	0	0	0	0	0	0
Total DQS Groups		6	8	6	8	10	6	8	10	14

(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section. • Deleted Serial RapidIO protocol under Embedded SERDES. • Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3. Mentioned transmit de-emphasis “pre- and post-cursors”.
		Architecture	Updated Overview section. • Revised description of PFU blocks. • Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section. • Changed PCI Express 2.0 to PCI Express Gen1 and Gen2. • Deleted Serial RapidIO protocol. • Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section. • Deleted “130 MHz ±15% CMOS” oscillator. • Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Added supply voltages V_{CCA} and V_{CCAUXA}.
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to t_{SKEW_PR} V_{CCA} and t_{SKEW_EDGE} and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.