E. FLattice Semiconductor Corporation - <u>LFE5UM5G-85F-8BG756I Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	21000
Number of Logic Elements/Cells	84000
Total RAM Bits	3833856
Number of I/O	365
Number of Gates	-
Voltage - Supply	1.045V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	756-FBGA
Supplier Device Package	756-CABGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe5um5g-85f-8bg756i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals. A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5/ECP5-5G devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5/ECP5-5G devices, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to ECP5 and ECP5-5G Memory Usage Guide (TN1264).



Table 2.4 provides a	description of	the signals	in the PLL blocks.
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Signal	Туре	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELODREG
PHASEDIR	Input	Dynamic Phase adjustment direction.
PHASESTEP	Input	Dynamic Phase adjustment step.
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL.
CLKOP	Output	Primary PLL output clock (with phase shift adjustment)
CLKOS	Output	Secondary PLL output clock (with phase shift adjust)
CLKOS2	Output	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	Output	Secondary PLL output clock3 (with phase shift adjust)
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

Table 2.4. PLL Blocks Signal Descriptions

For more details on the PLL you can refer to the ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (TN1263).

2.5. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5/ECP5-5G product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5/ECP5-5G also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2.6 on page 20 for LFE5UM/LFE5UM5G-85 device.



Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations				
	16,384 x 1				
	8,192 x 2				
Single Dort	4,096 x 4				
Single Port	2,048 x 9				
	1,024 x 18				
	512 x 36				
	16,384 x 1				
	8,192 x 2				
True Dual Port	4,096 x 4				
	2,048 x 9				
	1,024 x 18				
	16,384 x 1				
	8,192 x 2				
Decudo Dual Dort	4,096 x 4				
PSeudo Dual Port	2,048 x 9				
	1,024 x 18				
	512 x 36				

2.8.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.8.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.8.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.8.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- **Normal** Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- **Read-Before-Write** When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

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In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

The ECP5/ECP5-5G sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5/ECP5-5G slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	Ι

*Note: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to ECP5 and ECP5-5G sysDSP Usage Guide (TN1267).

2.10. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the ECP5/ECP5-5G devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5/ECP5-5G devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.





*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left and Right Sides

Name	Туре	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

Table 2.9. Output Block Port Description

2.12. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output. In DDR operation used mainly for DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to ECP5 and ECP5-5G High-Speed I/O Interface (TN1265).



Figure 2.21. Tristate Register Block on Top Side



2.15. SERDES and Physical Coding Sublayer

LFE5UM/LFE5UM5G devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s (ECP5), or up to 5 Gb/s (ECP5-5G) data rate. Figure 2.27 shows the position of the dual blocks for the LFE5-85. Table 2.13 shows the location of available SERDES Duals for all devices. The LFE5UM/LFE5UM5G SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s and 5 Gb/s) on ECP5-5G
- Ethernet (XAUI, GbE 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s), also E.48.LV2:4915 Mb/s in ECP5-5G
- JESD204A/B ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5) / 5 Gb/s (ECP5-5G)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

ECP5UM devices and ECP5-5G devices are pin-to-pin compatible. But, the ECP5UM devices require 1.1 V on VCCA, VCCHRX and VCCHTX supplies. ECP5-5G devices require 1.2 V on these supplies. When designing either family device with migration in mind, these supplies need to be connected such that it is possible to adjust the voltage level on these supplies.

When a SERDES Dual in a 2-Dual device is not used, the power VCCA power supply for that Dual should be connected. It is advised to connect the VCCA of unused channel to core if the user knows he will not use the Dual at all, or it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the VCCHTX to VCCA, and user can leave VCCHRX unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261).





Figure 2.27. SERDES/PCS Duals (LFE5UM/LFE5UM5G-85)

Table 2.13.	LFE5UM	/LFE5UM5G S	ERDES Standa	ard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0	2500	x1, x2, x4	8b10b
2.02	5000 ²	x1, x2	8b10b
Gigabit Ethernet	1250	x1	8b10b
SCMI	1250	x1	8b10b
SGIVIII	2500	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5	614.4 1228.8 2457.6 3072.0 4915.2 ²	x1	8b10b
SD-SDI (259M, 344M) ¹	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
	5000	_	_
JESD204A/B	3125	x1	8b/10b

Notes:

1. For SD-SDI rate, the SERDES is bypassed and SERDES input signals are directly connected to the FPGA routing.

2. For ECP5-5G family devices only.



Package	LFE5UM/LFE5UM5G-25	LFE5UM/LFE5UM5G-45	LFE5UM/LFE5UM5G-85
285 csfBGA	1	1	1
381 caBGA	1	2	2
554 caBGA	-	2	2
756 caBGA	-	-	2

Table 2.14. Available SERDES Duals per LFE5UM/LFE5UM5G Devices

2.15.1. SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCHTX and VCCHRX).



Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.15.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Some of the enhancements in LFE5UM/LFE5UM5G SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced Tx de-emphasis: Programmable pre- and post-cursors improves Tx output signaling
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function

Refer to ECP5 and ECP5-5G SERDES/PCS Usage Guide (TN1261) for more information.

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3.14.4. LVDS25E

The top and bottom sides of ECP5/ECP5-5G devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.



Figure 3.1. LVDS25E Output Termination Example

Table 3.14. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V _{CCIO}	Output Driver Supply (±5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
Rs	Driver Series Resistor (±1%)	158	Ω
R _P	Driver Parallel Resistor (±1%)	140	Ω
R _T	Receiver Termination (±1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
ZBACK	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

Note: For input buffer, see LVDS Table 3.13 on page 55.

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3.18. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.22. ECP5/ECP5-5G External Switching Characteristics

Dawawashaw	Description	Dovico -8		-7		-6		Unit	
Parameter			Min	Max	Min	Max	Min	Max	Unit
Clocks									
Primary Clock									
f _{MAX_PRI}	Frequency for Primary Clock Tree	_	—	370	—	303	—	257	MHz
t _{w_pri}	Clock Pulse Width for Primary Clock	_	0.8	—	0.9	-	1.0	-	ns
t _{skew_pri}	Primary Clock Skew within a Device	_	_	420	_	462	_	505	ps
Edge Clock									
f _{MAX_EDGE}	Frequency for Edge Clock Tree	_	_	400	_	350	_	312	MHz
tw_edge	Clock Pulse Width for Edge Clock	_	1.175	—	1.344		1.50		ns
t _{skew_edge}	Edge Clock Skew within a Bank	—	_	160	_	180	—	200	ps
Generic SDR Input									
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ithout PL	L					
t _{co}	Clock to Output - PIO Output Register	All Devices	—	5.4	_	6.1	—	6.8	ns
t _{su}	Clock to Data Setup - PIO Input Register	All Devices	0	_	0	-	0	-	ns
t _H	Clock to Data Hold - PIO Input Register	All Devices	2.7	_	3	-	3.3	-	ns
t _{su_del}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.2	_	1.33	_	1.46	_	ns
t _{h_del}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	_	0	_	0	_	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	_	400	_	350	_	312	MHz
General I/O Pin Pa	arameters Using Dedicated Primary	Clock Input w	ith PLL						
t _{copll}	Clock to Output - PIO Output Register	All Devices	_	3.5	_	3.8	_	4.1	ns
t _{supll}	Clock to Data Setup - PIO Input Register	All Devices	0.7	_	0.78	-	0.85	_	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.8	_	0.89	_	0.98	_	ns
t _{su_delpll}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.6	_	1.78	_	1.95	_	ns

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	.	_	1	-8	-	-7	-6		
Parameter	Description	Device	Min	Max	Min	Max	Min	Max	Unit
t _{h_delpll}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	_	0	_	0	_	ns
Generic DDR Input							•		
Generic DDRX1 Inp	uts With Clock and Data Centere	d at Pin (GDDI	RX1_RX.	SCLK.Cent	tered) Us	ing PCLK	Clock In	put - Fig	ure 3.6
t _{SU_GDDRX1_centered}	Data Setup Before CLK Input	All Devices	0.52	-	0.52	-	0.52	_	ns
t _{HD_GDDRX1_centered}	Data Hold After CLK Input	All Devices	0.52	_	0.52	_	0.52	_	ns
f _{DATA_GDDRX1_centered}	GDDRX1 Data Rate	All Devices	_	500	_	500	_	500	Mb/s
f _{MAX_GDDRX1_centered}	GDDRX1 CLK Frequency (SCLK)	All Devices	_	250	-	250	_	250	MHz
Generic DDRX1 Inp	uts With Clock and Data Aligned	at Pin (GDDR)	(1_RX.SC	LK.Aligne	ed) Using	PCLK Cl	ock Input	- Figure	3.7
$t_{su_GDDRX1_aligned}$	Data Setup from CLK Input	All Devices	-	-0.55	-	-0.55	-	-0.55	ns + 1/2 UI
$t_{HD_GDDRX1_aligned}$	Data Hold from CLK Input	All Devices	All Devices 0.55 —		0.55	-	0.55	_	ns + 1/2 UI
$f_{DATA_GDDRX1_aligned}$	GDDRX1 Data Rate	All Devices	—	500	-	500	—	500	Mb/s
$f_{MAX_GDDRX1_aligned}$	f _{MAX GDDRX1 aligned} GDDRX1 CLK Frequency (SCLK)		-	250	—	250	—	250	MHz
Generic DDRX2 Inp	uts With Clock and Data Centere	d at Pin (GDDI	RX2_RX.I	ECLK.Cent	tered) Us	ing PCLK	Clock In	put, Left	and
Right sides Only - F	igure 3.6	T			T	1	1	Т	
$t_{SU_GDDRX2_centered}$	Data Setup before CLK Input	All Devices	0.321	. –	0.403	—	0.471	—	ns
$t_{HD_GDDRX2_centered}$	Data Hold after CLK Input	All Devices	0.321	. —	0.403	_	0.471	_	ns
$f_{\text{DATA}_{GDDRX2}_{centered}}$	GDDRX2 Data Rate	All Devices	_	800	_	700	_	624	Mb/s
$f_{MAX_GDDRX2_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	-	400	—	350	—	312	MHz
Generic DDRX2 Inp	uts With Clock and Data Aligned	at Pin (GDDR)	(2_RX.EC	LK.Aligne	ed) Using	PCLK Cl	ock Input	, Left an	d Right
sides Only - Figure	3.7								1
t _{SU_GDDRX2_aligned}	Data Setup from CLK Input	All Devices	-	-0.344	—	-0.42	-	-0.495	ns + 1/2 UI
$t_{HD_GDDRX2_aligned}$	Data Hold from CLK Input	All Devices	0.344	—	0.42	_	0.495	_	ns + 1/2 UI
$f_{DATA_GDDRX2_aligned}$	GDDRX2 Data Rate	All Devices	_	800	—	700	—	624	Mb/s
f _{MAX_GDDRX2_aligned}	GDDRX2 CLK Frequency	All Devices	—	400	_	350	_	312	MHz
Video DDRX71 Inpu	uts With Clock and Data Aligned a	t Pin (GDDRX	71_RX.E	CLK) Usin	g PLL Clo	ck Input	, Left and	Right si	des Only
Figure 3.11									
t _{su_lvds71_i}	Data Setup from CLK Input (bit i)	All Devices	_	-0.271	—	-0.39	_	-0.41	ns+(1/2+i) * UI
t _{HD_LVDS71_i}	Data Hold from CLK Input (bit i)	All Devices	0.271	—	0.39	_	0.41	_	ns+(1/2+i) * UI
f _{DATA_LVDS71}	DDR71 Data Rate	All Devices	_	756	—	620	—	525	Mb/s
f _{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	_	378	—	310	—	262.5	MHz

Table 3.22. ECP5/ECP5-5G External Switching Characteristics (Continued)



3.21. SERDES/PCS Block Latency

Table 3.26 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Т	able 3.2	6. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit ³
Transmi	t Data Latency ¹						
T 1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	-	1	byte clk
11	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
Т2	8b10b Encoder	_	—	—	2	1	byte clk
Т3	SERDES Bridge transmit	_	—	—	2	1	byte clk
TA	Serializer: 8-bit mode	_	—	—	15 + ∆1	—	UI + ps
14	Serializer: 10-bit mode	_	—	—	18 + Δ 1	—	UI + ps
тс	Pre-emphasis ON	_	—	—	1 + ∆2	—	UI + ps
15	Pre-emphasis OFF	_	—	—	0 + ∆3	—	UI + ps
Receive	Data Latency ²						
D1	Equalization ON	_	—	—	Δ1	—	UI + ps
KI .	Equalization OFF	_	—	—	Δ2	—	UI + ps
22	Deserializer: 8-bit mode	_	—	—	10 + ∆3	—	UI + ps
R2	Deserializer: 10-bit mode	_	—	—	12 + ∆3	—	UI + ps
R3	SERDES Bridge receive	_	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	_	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	_	1	byte clk
57	FPGA Bridge - Gearing disabled with same clocks	4	_	5	_	1	byte clk
ñ/	FPGA Bridge - Gearing enabled	7	_	9	_	_	word clk

Notes:

1. $\Delta 1 = -245 \text{ ps}, \Delta 2 = +88 \text{ ps}, \Delta 3 = +112 \text{ ps}.$

2. $\Delta 1 = +118 \text{ ps}, \Delta 2 = +132 \text{ ps}, \Delta 3 = +700 \text{ ps}.$

3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).









*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3.16. sysCONFIG Parallel Port Write Cycle



Figure 3.17. sysCONFIG Slave Serial Port Timing



4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	DDR Strobe (DQS) and Data (DQ) Pins					
For Left and Right Edges of the Device Only							
	А	DQ					
	В	DQ					
	С	DQ					
	D	DQ					
	А	DQ					
	В	DQ					
P[L/K] [II-3]	С	DQ					
	D	DQ					
	А	DQS (P)					
	В	DQS (N)					
	С	DQ					
	D	DQ					
	А	DQ					
	В	DQ					
רניהן [11+3]	С	DQ					
	D	DQ					

Note: "n" is a row PIC number.

4.3. **Pin Information Summary**

4.3.1. **LFE5UM/LFE5UM5G**

Pin Information Summary	LFE5 LFE5UI	5UM/ M5G-25	LFE5UN	//LFE5U	M5G-45	LFE5UM/LFE5UM5G-85				
Pin Type	285 csfBG	381 caBGA	285 csfBGA	381 caBG	554 caBGA	285 csfBGA	381 caBG	554 caBGA	756 caBGA	
	Bank 0	6	24	6	27	32	6	27	32	56
	Bank 1	6	32	6	33	40	6	33	40	48
	Bank 2	21	32	21	32	32	21	34	32	48
General Purpose	Bank 3	28	32	28	33	48	28	33	48	64
Inputs/Outputs per Bank	Bank 4	0	0	0	0	0	0	0	14	24
	Bank 6	26	32	26	33	48	26	33	48	64
	Bank 7	18	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13
Total Single-Ended User I/O		118	197	118	203	245	118	205	259	365
VCC		13	20	13	20	24	13	20	24	36
VCCAUX (Core)		3	4	3	4	9	3	4	9	8
	Bank 0	1	2	1	2	3	1	2	3	4
	Bank 1	1	2	1	2	3	1	2	3	4
	Bank 2	2	3	2	3	4	2	3	4	4
VCCIO	Bank 3	2	3	2	3	3	2	3	3	4
	Bank 4	0	0	0	0	0	0	0	2	2
	Bank 6	2	3	2	3	4	2	3	4	4
	Bank 7	2	3	2	3	3	2	3	3	4
	Bank 8	2	2	2	2	2	2	2	2	2

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4.3.2. LFE5U

Pin Information Summary		L	LFE5U-12 LFE5U-25				LFE5	U-45		LFE5U-85					
Pin Type		256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	256 caBGA	285 csfBGA	381 caBGA	554 caBGA	285 csfBG	381 caBGA	554 caBGA	756 caBG
	Bank 0	24	6	24	24	6	24	24	6	27	32	6	27	32	56
	Bank 1	32	6	32	32	6	32	32	6	33	40	6	33	40	48
General	Bank 2	32	21	32	32	21	32	32	21	32	32	21	34	32	48
Purpose	Bank 3	32	28	32	32	28	32	32	28	33	48	28	33	48	64
Inputs/Outputs	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	14	24
per Bank	Bank 6	32	26	32	32	26	32	32	26	33	48	26	33	48	64
	Bank 7	32	18	32	32	18	32	32	18	32	32	18	32	32	48
	Bank 8	13	13	13	13	13	13	13	13	13	13	13	13	13	13
Total Single-Ende	d User	197	118	197	197	118	197	197	118	203	245	118	205	259	365
VCC		6	13	20	6	13	20	6	13	20	24	13	20	24	36
VCCAUX (Core)		2	3	4	2	3	4	2	3	4	9	3	4	9	8
	Bank 0	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 1	2	1	2	2	1	2	2	1	2	3	1	2	3	4
	Bank 2	2	2	3	2	2	3	2	2	3	4	2	3	4	4
VCCIO	Bank 3	2	2	3	2	2	3	2	2	3	3	2	3	3	4
VCCIO	Bank 4	0	0	0	0	0	0	0	0	0	0	0	0	2	2
	Bank 6	2	2	3	2	2	3	2	2	3	4	2	3	4	4
	Bank 7	2	2	3	2	2	3	2	2	3	3	2	3	3	4
	Bank 8	1	2	2	1	2	2	1	2	2	2	2	2	2	2
ТАР		4	4	4	4	4	4	4	4	4	4	4	4	4	4
Miscellaneous De	dicated	7	7	7	7	7	7	7	7	7	7	7	7	7	7
GND		27	123	99	27	123	99	27	123	99	198	123	99	198	267
NC		0	1	26	0	1	26	0	1	26	33	1	26	33	29
Reserved		0	4	6	0	4	6	0	4	6	12	4	6	12	12
Total Balls		256	285	381	256	285	381	256	285	381	554	285	381	554	756
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	16/8	16/8	10/8	17/9	16/8
High Speed Differ	ential	Bank	16/8	14/7	16/8	16/8	14/7	16/8	16/8	14/7	16/8	24/12	14/7	16/8	24/1
Input / Output Pa	irs	Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	16/8	13/6	16/8	16/8	13/6	16/8	16/8	13/6	16/8	24/12	13/6	16/8	24/1
		Bank	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8	8/6	16/8	16/8
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
Total High Speed		64/32	45/27	64/32	64/32	45/27	64/32	64/32	45/27	64/32	80/40	45/27	65/33	80/40	112/
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	2	1	2	2	1	2	2	1	2	2	1	2	2
DQS Groups	,	Bank	2	2	2	2	2	2	2	2	2	3	2	2	3
(> 11 pins in grou	p)	Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
		Bank	2	2	2	2	2	2	2	2	2	3	2	2	3
		Bank	2	1	2	2	1	2	2	1	2	2	1	2	2
		Bank	0	0	0	0	0	0	0	0	0	0	0	0	0
Total DQS Groups	5	8	6	8	8	6	8	8	6	8	10	6	8	10	14





5.2. Ordering Part Numbers

5.2.1. Commercial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256C	-6	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-7BG256C	-7	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-8BG256C	-8	Lead free caBGA	256	Commercial	12	No
LFE5U-12F-6MG285C	-6	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-7MG285C	-7	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-8MG285C	-8	Lead free csfBGA	285	Commercial	12	No
LFE5U-12F-6BG381C	-6	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-7BG381C	-7	Lead free caBGA	381	Commercial	12	No
LFE5U-12F-8BG381C	-8	Lead free caBGA	381	Commercial	12	No
LFE5U-25F-6BG256C	-6	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-7BG256C	-7	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-8BG256C	-8	Lead free caBGA	256	Commercial	24	No
LFE5U-25F-6MG285C	-6	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-7MG285C	-7	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-8MG285C	-8	Lead free csfBGA	285	Commercial	24	No
LFE5U-25F-6BG381C	-6	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-7BG381C	-7	Lead free caBGA	381	Commercial	24	No
LFE5U-25F-8BG381C	-8	Lead free caBGA	381	Commercial	24	No
LFE5U-45F-6BG256C	-6	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-7BG256C	-7	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-8BG256C	-8	Lead free caBGA	256	Commercial	44	No
LFE5U-45F-6MG285C	-6	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-7MG285C	-7	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-8MG285C	-8	Lead free csfBGA	285	Commercial	44	No
LFE5U-45F-6BG381C	-6	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-7BG381C	-7	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-8BG381C	-8	Lead free caBGA	381	Commercial	44	No
LFE5U-45F-6BG554C	-6	Lead free caBGA	554	Commercial	44	No
LFE5U-45F-7BG554C	-7	Lead free caBGA	554	Commercial	44	No

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Part number	Grade Package		Pins	Temp.	LUTs (K)	SERDES
LFE5UM5G-85F-8BG381C	-8	Lead free caBGA	381	Commercial	84	Yes
LFE5UM5G-85F-8BG554C	-8	Lead free caBGA	554	Commercial	84	Yes
LFE5UM5G-85F-8BG756C	-8	Lead free caBGA	756	Commercial	84	Yes

5.2.2. Industrial

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LFE5U-12F-6BG256I	-6	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-7BG256I	-7	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-8BG256I	-8	Lead free caBGA	256	Industrial	12	No
LFE5U-12F-6MG285I	-6	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-7MG285I	-7	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-8MG285I	-8	Lead free csfBGA	285	Industrial	12	No
LFE5U-12F-6BG381I	-6	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-7BG381I	-7	Lead free caBGA	381	Industrial	12	No
LFE5U-12F-8BG381I	-8	Lead free caBGA	381	Industrial	12	No
LFE5U-25F-6BG256I	-6	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-7BG256I	-7	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-8BG256I	-8	Lead free caBGA	256	Industrial	24	No
LFE5U-25F-6MG285I	-6	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-7MG285I	-7	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-8MG285I	-8	Lead free csfBGA	285	Industrial	24	No
LFE5U-25F-6BG381I	-6	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-7BG381I	-7	Lead free caBGA	381	Industrial	24	No
LFE5U-25F-8BG381I	-8	Lead free caBGA	381	Industrial	24	No
LFE5U-45F-6BG256I	-6	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-7BG256I	-7	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-8BG256I	-8	Lead free caBGA	256	Industrial	44	No
LFE5U-45F-6MG285I	-6	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-7MG285I	-7	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-8MG285I	-8	Lead free csfBGA	285	Industrial	44	No
LFE5U-45F-6BG381I	-6	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-7BG381I	-7	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-8BG381I	-8	Lead free caBGA	381	Industrial	44	No
LFE5U-45F-6BG554I	-6	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-7BG554I	-7	Lead free caBGA	554	Industrial	44	No
LFE5U-45F-8BG554I	-8	Lead free caBGA	554	Industrial	44	No
LFE5U-85F-6MG285I	-6	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-7MG285I	-7	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-8MG285I	-8	Lead free csfBGA	285	Industrial	84	No
LFE5U-85F-6BG381I	-6	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-7BG381I	-7	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-8BG381I	-8	Lead free caBGA	381	Industrial	84	No
LFE5U-85F-6BG554I	-6	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-7BG554I	-7	Lead free caBGA	554	Industrial	84	No
LFE5U-85F-8BG554I	-8	Lead free caBGA	554	Industrial	84	No



(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	All	Changed document status from Advance to Preliminary.
		General Description	Updated Features section.
			Deleted Serial RapidIO protocol under Embedded SERDES.
			Corrected data rate under Pre-Engineered Source Synchronous
			Changed DD3. LPDDR3 to DDR2/3, LPDDR2/3.
			Mentioned transmit de-emphasis "pre- and post-cursors".
		Architecture	Updated Overview section.
			Revised description of PFU blocks.
			 Specified SRAM cell settings in describing the control of SERDES/PCS duals.
			Updated SERDES and Physical Coding Sublayer section.
			Changed PCI Express 2.0 to PCI Express Gen1 and Gen2.
			Deleted Serial RapidIO protocol.
			 Updated Table 2.13. LFE5UM/LFE5UM5G SERDES Standard Support.
			Updated On-Chip Oscillator section.
			• Deleted "130 MHz ±15% CMOS" oscillator.
			 Updated Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)
		DC and Switching	Updated Absolute Maximum Ratings section. Added supply voltages
		Characteristics	V _{CCA} and V _{CCAUXA} .
			Updated sysI/O Recommended Operating Conditions section. Revised HSULD12D VCCIO values and removed table note.
			Updated sysI/O Single-Ended DC Electrical Characteristics section. Revised some values for SSTL15 _I, SSTL15 _II, SSTL135_I, SSTL15_II, and HSUL12.
			Updated External Switching Characteristics section. Changed parameters to $t_{\text{SKEW}_{PR}}V_{\text{CCA}}$ and $t_{\text{SKEW}_{\text{EDGE}}}$ and added LFE5-85 as device.
			Updated ECP5 Family Timing Adders section. Added SSTL135_II buffer type data. Removed LVCMOS33_20mA, LVCMOS25_20mA, LVCMOS25_16mA, LVCMOS25D_16mA, and LVCMOS18_16mA buffer types. Changed buffer type to LVCMOS12_4mA and LVCMOS12_8mA.
			Updated Maximum I/O Buffer Speed section. Revised Max values.
			Updated sysCLOCK PLL Timing section. Revised t_{DT} Min and Max values. Revised t_{OPJIT} Max value. Revised number of samples in table note 1.
			Updated SERDES High-Speed Data Transmitter section. Updated Table 3.24. Serial Output Timing and Levels and Table 3.25. Channel Output Jitter.



(Continued)

Date	Version	Section	Change Summary
August 2014	1.2	DC and Switching Characteristics	SERDES High-Speed Data Receiver section. Updated Table 3.26. Serial Input Data Specifications, Table 3.28. Receiver Total Jitter Tolerance Specification, and Table 3.29. External Reference Clock Specification (refclkp/refclkn).
			Modified section heading to XXAUI/CPRI LV E.30 Electrical and Timing Characteristics. Updated Table 3.33 Transmit and Table 3.34. Receive and Jitter Tolerance.
			Modified section heading to CPRI LV E.24 Electrical and Timing Characteristics. Updated Table 3.35. Transmit and Table 3.36. Receive and Jitter Tolerance.
			Modified section heading to Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics. Updated Table 3.37. Transmit and Table 3.38. Receive and Jitter Tolerance.
June 2014	1.1	Ordering Information	Updated ECP5/ECP5-5G Part Number Description and Ordering Part Numbers sections.
March 2014	1.0	All	Initial release.



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