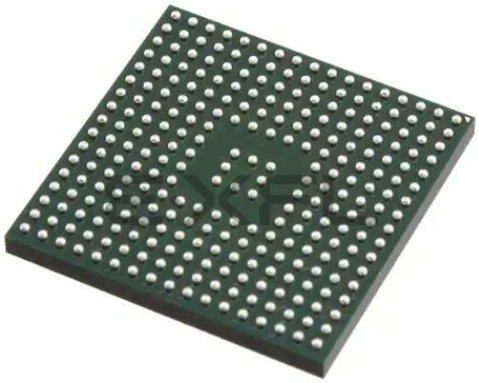

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	272-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9307-cr

Table of Contents

List of Figures

Real-Time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 KHz input clock. This compensation is accurate to ±1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9307 device will not boot.

Table K. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Table L. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Name - Description
XTALI	Main Oscillator Input
XTALO	Main Oscillator Output
VDD_PLL	Main Oscillator Power
GND_PLL	Main Oscillator Ground

Timers

The Watchdog Timer ensures proper operation by requiring periodic attention to prevent a reset-on-time-out.

Two 16-bit timers operate as free running down-counters or as periodic timers for fixed interval interrupts and have a range of 0.03 ms to 4.27 seconds.

One 32-bit timer, plus a 6-bit prescale counter, has a range of 0.03 µs to 73.3 hours.

One 40-bit debug timer, plus a 6-bit prescale counter, has a range of 1.0 µs to 12.7 days.

Interrupt Controller

The interrupt controller allows up to 62 interrupts to generate an Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) signal to the processor core. Thirty-two hardware priority assignments are provided for assisting IRQ vectoring, and two levels are provided for FIQ vectoring. This allows time critical interrupts to be processed in the shortest time possible. Internal interrupts may be programmed as active high or active low level sensitive inputs. GPIO pins programmed as interrupts may be programmed as active high level sensitive, active low level sensitive, rising edge triggered, falling edge triggered, or combined rising/falling edge triggered.

- Supports 64 interrupts from a variety of sources (such as UARTs, GPIO, and key matrix)
- Routes interrupt sources to either the ARM920T's IRQ or FIQ (Fast IRQ) inputs
- Three dedicated off-chip interrupt lines operate as active high level sensitive interrupts
- Any of the 16 GPIO lines maybe configured to generate interrupts
- Software supported priority mask for all FIQs and IRQs

Table M. External Interrupt Controller Pin Assignment

Pin Mnemonic	Pin Name - Description
INT[2:0]	External Interrupts 2, 1, 0

Dual LED Drivers

Two pins are assigned specifically to drive external LEDs.

Table N. Dual LED Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
GRLED	Green LED	General Purpose I/O
REDLED	Red LED	General Purpose I/O

General Purpose Input/Output (GPIO)

The 14 EGPIO pins may each be configured individually as an output, an input, or an interrupt input.

There are 22 pins that may alternatively be used as input, output, or open-drain pins, but do not support interrupts. These pins are:

- Key Matrix ROW[7:0], COL[7:0]
- Ethernet MDIO
- Both LED Outputs
- Two-wire Clock and Data
- GGPIO[2]
- HGPIO[7:2]

6 pins may alternatively be used as inputs only:

- CTSn, DSRn/DCDn
- 4 Interrupt Lines

2 pins may alternatively be used as outputs only:

- RTSn
- ARSTn

Table O. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15] EGPIO[13:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[7] FGPIO[5] FGPIO[0]	Expanded General Purpose Input / Output Pins with Interrupts

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 200 MHz (184 MHz for industrial conditions).

Table P. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table Q. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-Channel DMA Controller

The DMA module contains 12 separate DMA channels. These may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Timings

Timing Diagram Conventions

This data sheet contains one or more timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

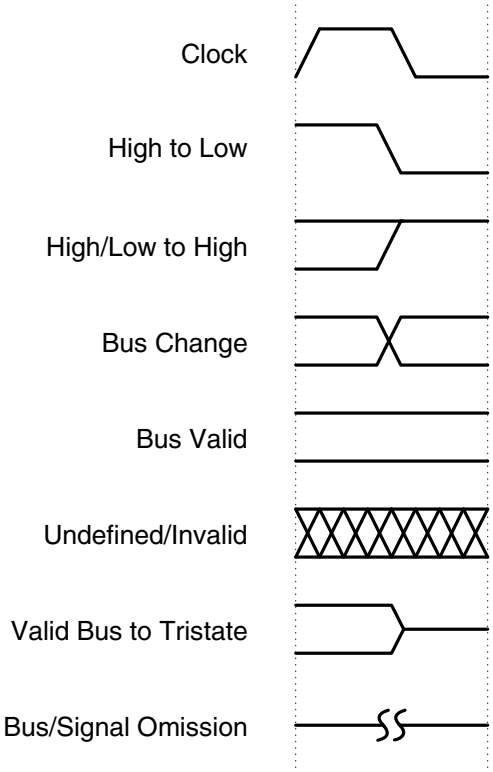


Figure 1. Timing Diagram Drawing Key

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements.

- T_A = 0 to 70° C
- CVDD = VDD_PLL = 1.8V
- RVDD = 3.3 V
- All grounds = 0 V
- Logic 0 = 0 V, Logic 1 = 3.3 V
- Output loading = 50 pF
- Timing reference levels = 1.5 V
- The Processor Bus Clock (HCLK) is programmable and is set by the user. The frequency is typically between 33 MHz and 100 MHz (92 MHz for industrial conditions).

Memory Interface

Figure 2 through Figure 5 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK high time	t_{clk_high}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK low time	t_{clk_low}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK rise/fall time	t_{clkrf}	-	2	4	ns
Signal delay from SDCLK rising edge time	t_d	-	-	8	ns
Signal hold from SDCLK rising edge time	t_h	1	-	-	ns
DQMn delay from SDCLK rising edge time	t_{DQd}	-	-	8	ns
DQMn hold from SDCLK rising edge time	t_{DQh}	1	-	-	ns
DA valid setup to SDCLK rising edge time	t_{DAs}	2	-	-	ns
DA valid hold from SDCLK rising edge time	t_{DAh}	3	-	-	ns

SDRAM Load Mode Register Cycle

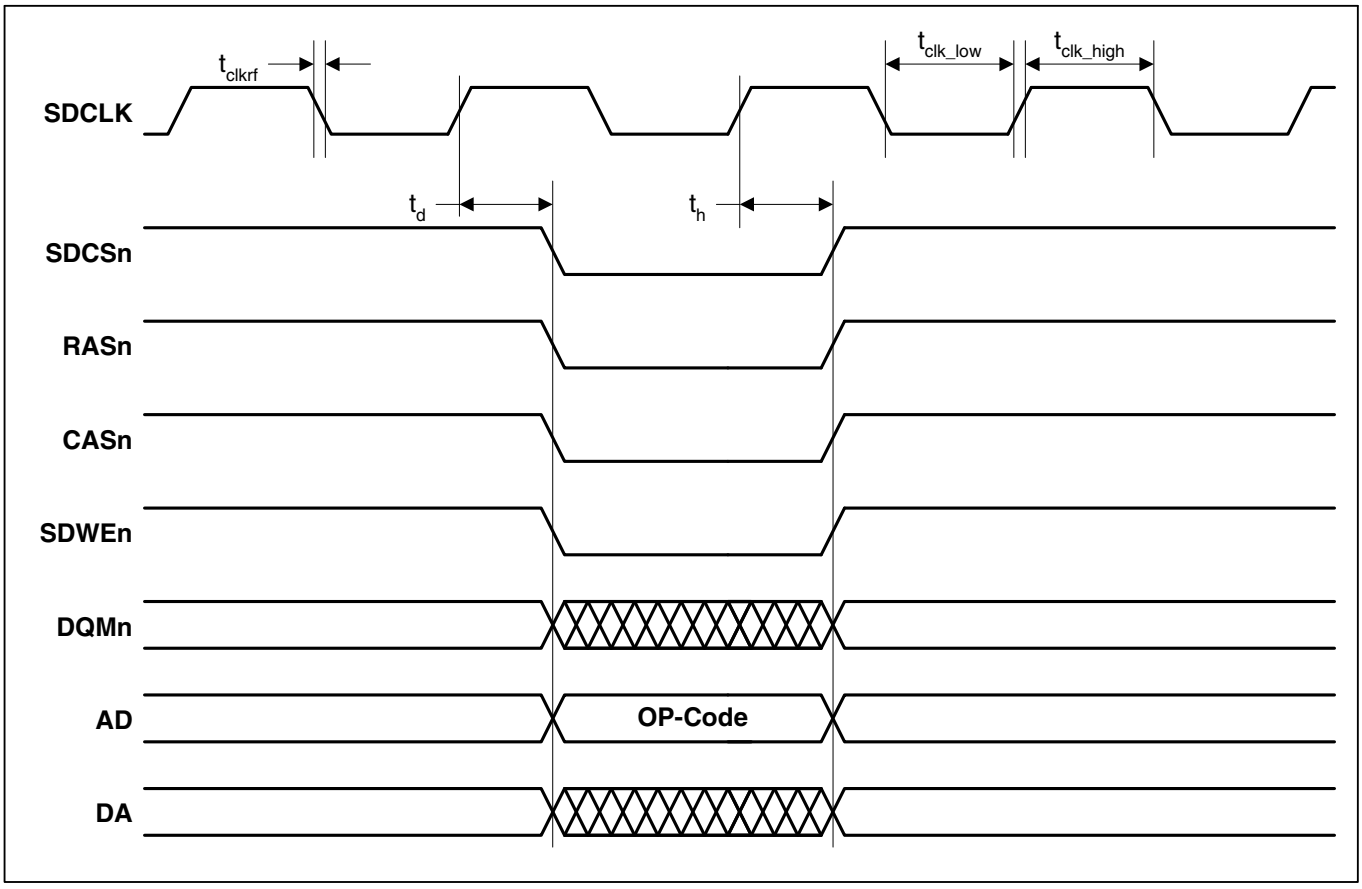


Figure 2. SDRAM Load Mode Register Cycle Timing Measurement

SDRAM Burst Write Cycle

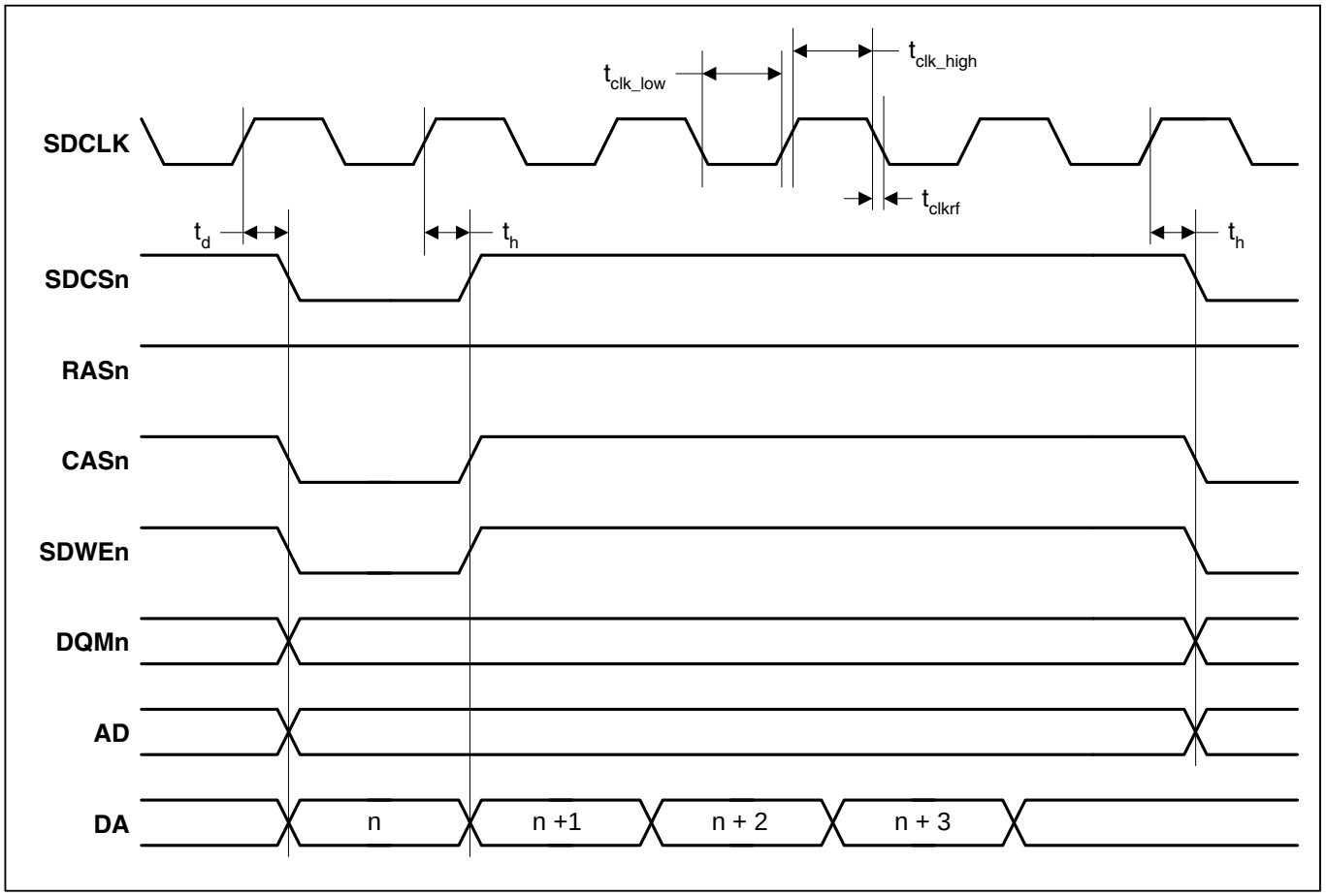
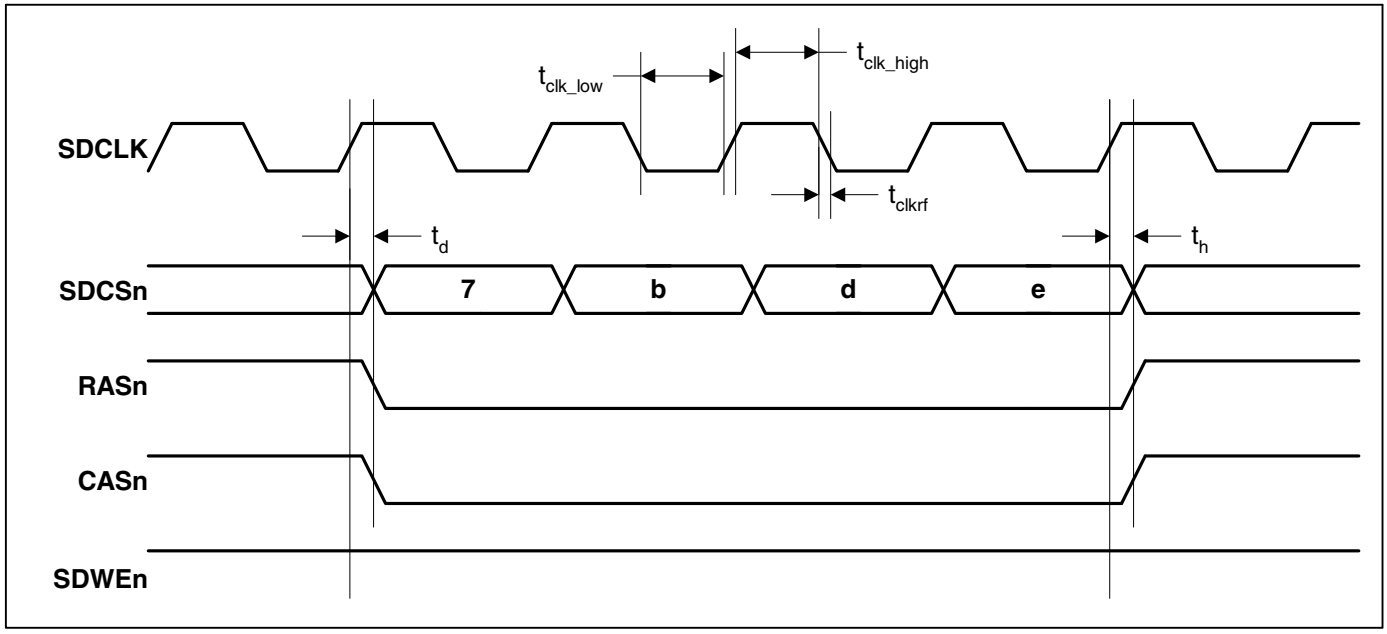


Figure 4. SDRAM Burst Write Cycle Timing Measurement

SDRAM Auto Refresh Cycle



Note: Chip select shown as bus to illustrate multiple devices being put into auto refresh in one access

Figure 5. SDRAM Auto Refresh Cycle Timing Measurement

Static Memory Single Word Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	t_{HCLK} - 3	-	-	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
WRn deassert to CSn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpw}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
WRn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn assert to DA valid	t_{DAV}	-	-	8	ns

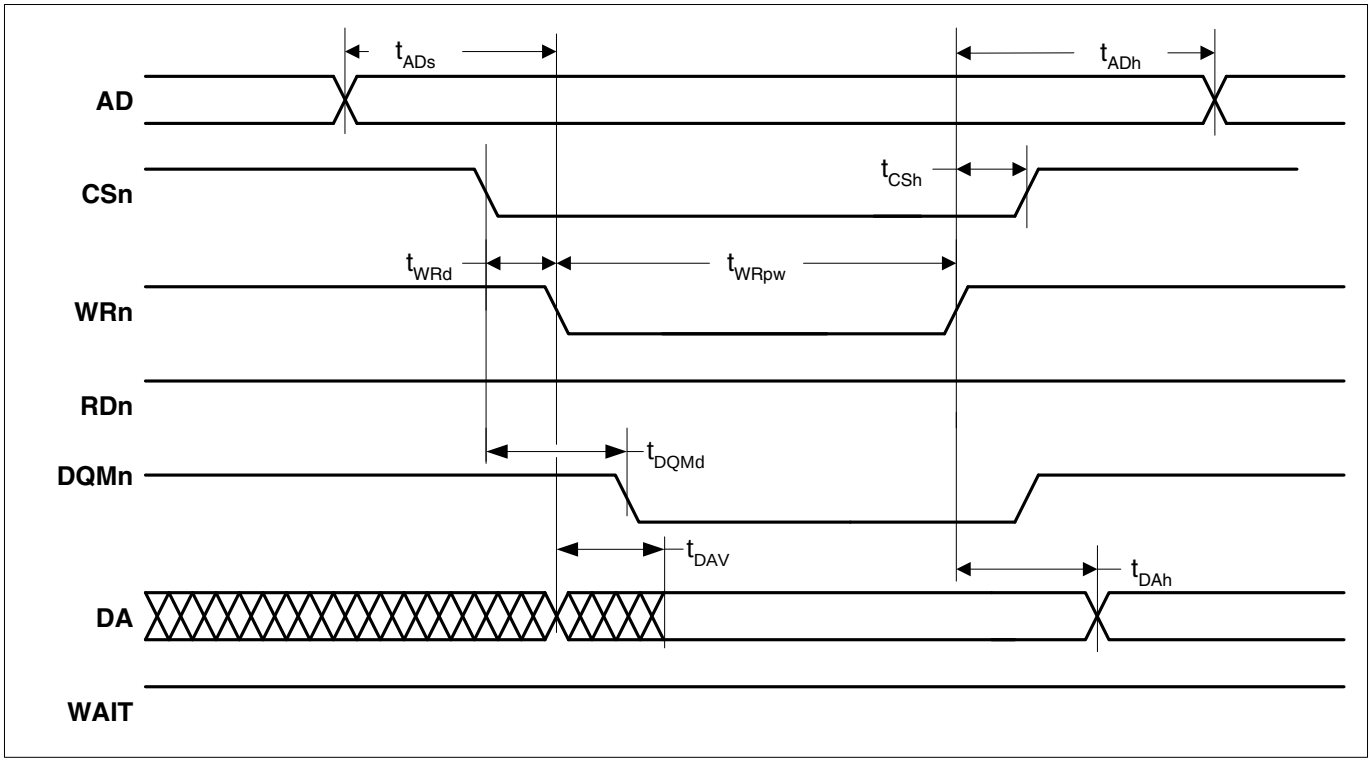


Figure 7. Static Memory Single Word Write Cycle Timing Measurement

Static Memory 32-bit Write on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	$t_{HCLK} \times 2$	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

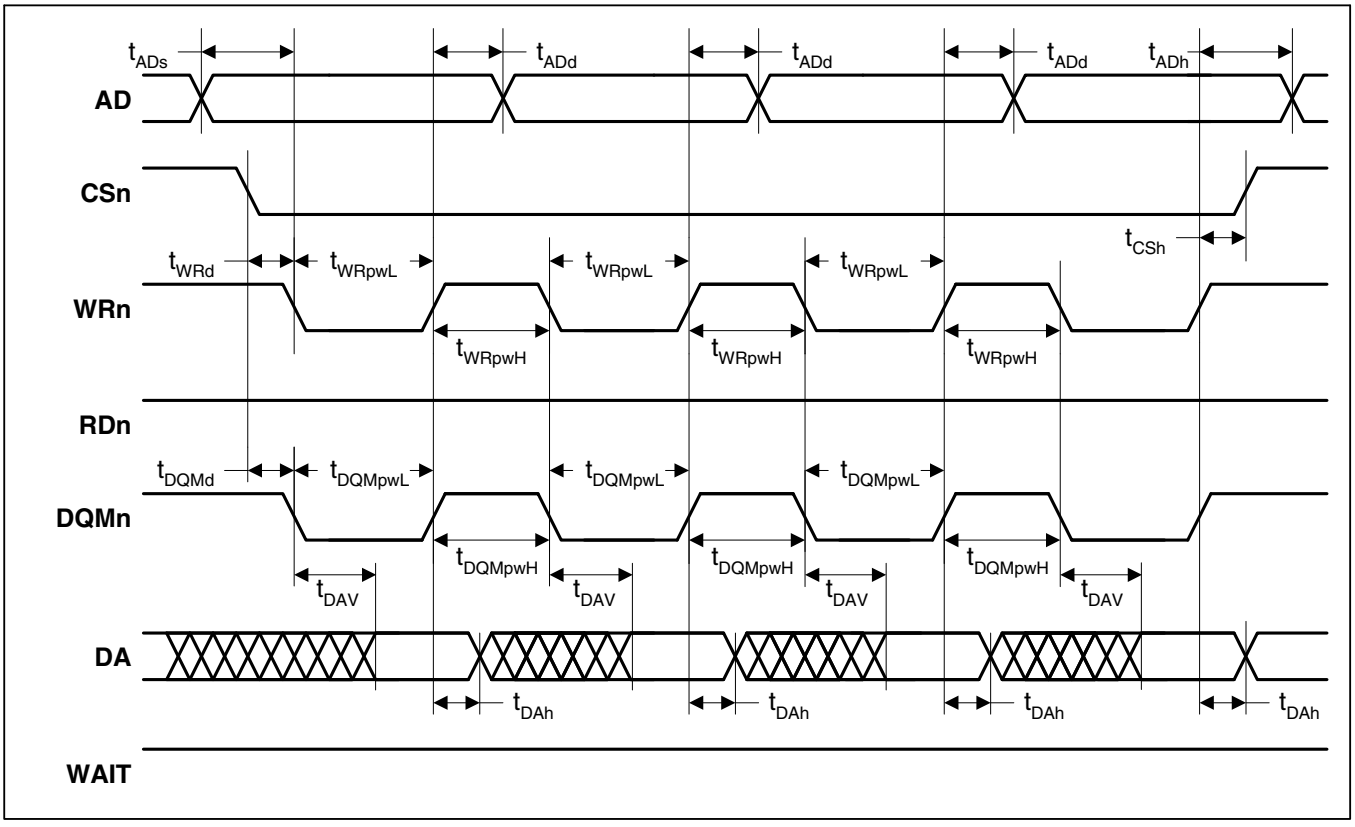


Figure 9. Static Memory Multiple Word Write 8-bit Cycle Timing Measurement

Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

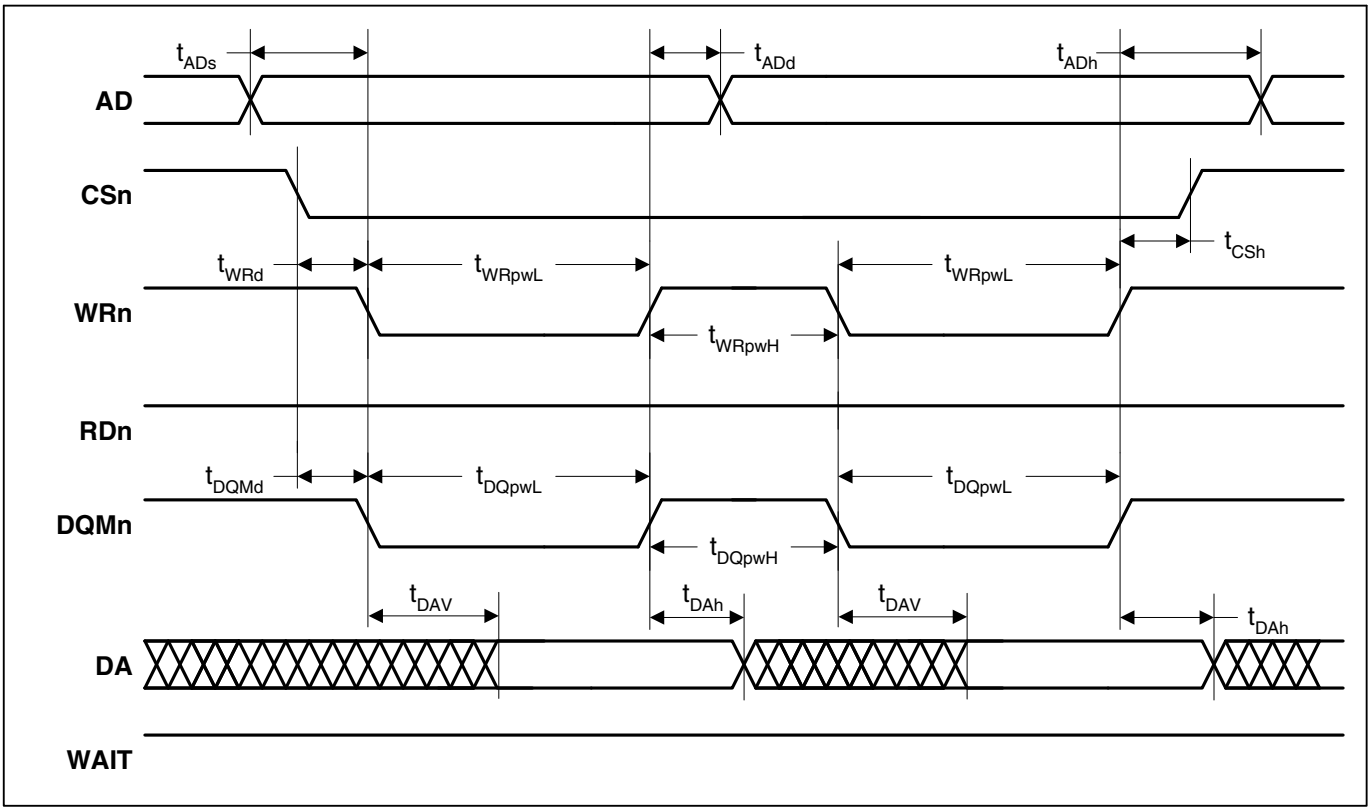


Figure 11. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

Static Memory Turnaround Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSnX deassert to CSnY assert time	t_{BTcyc}	-	$t_{HCLK} \times (IDCY+1)$	-	ns

Notes: 1. X and Y represent any two chip select numbers.
2. IDCY occurs on read-to-write and write-to-read.
3. IDCY is honored when going from a asynchronous device (CSx) to a synchronous device (/SDCSy).

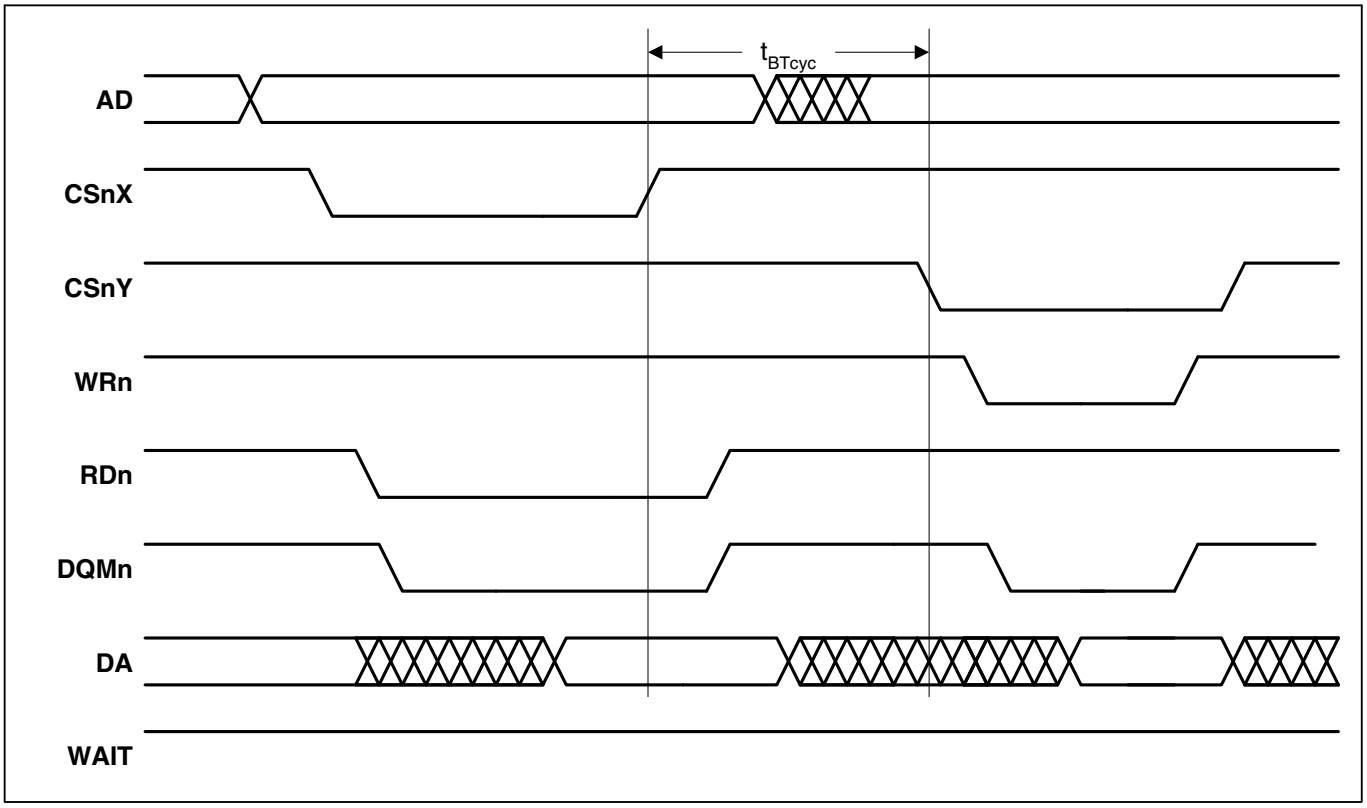


Figure 16. Static Memory Turnaround Cycle Timing Measurement

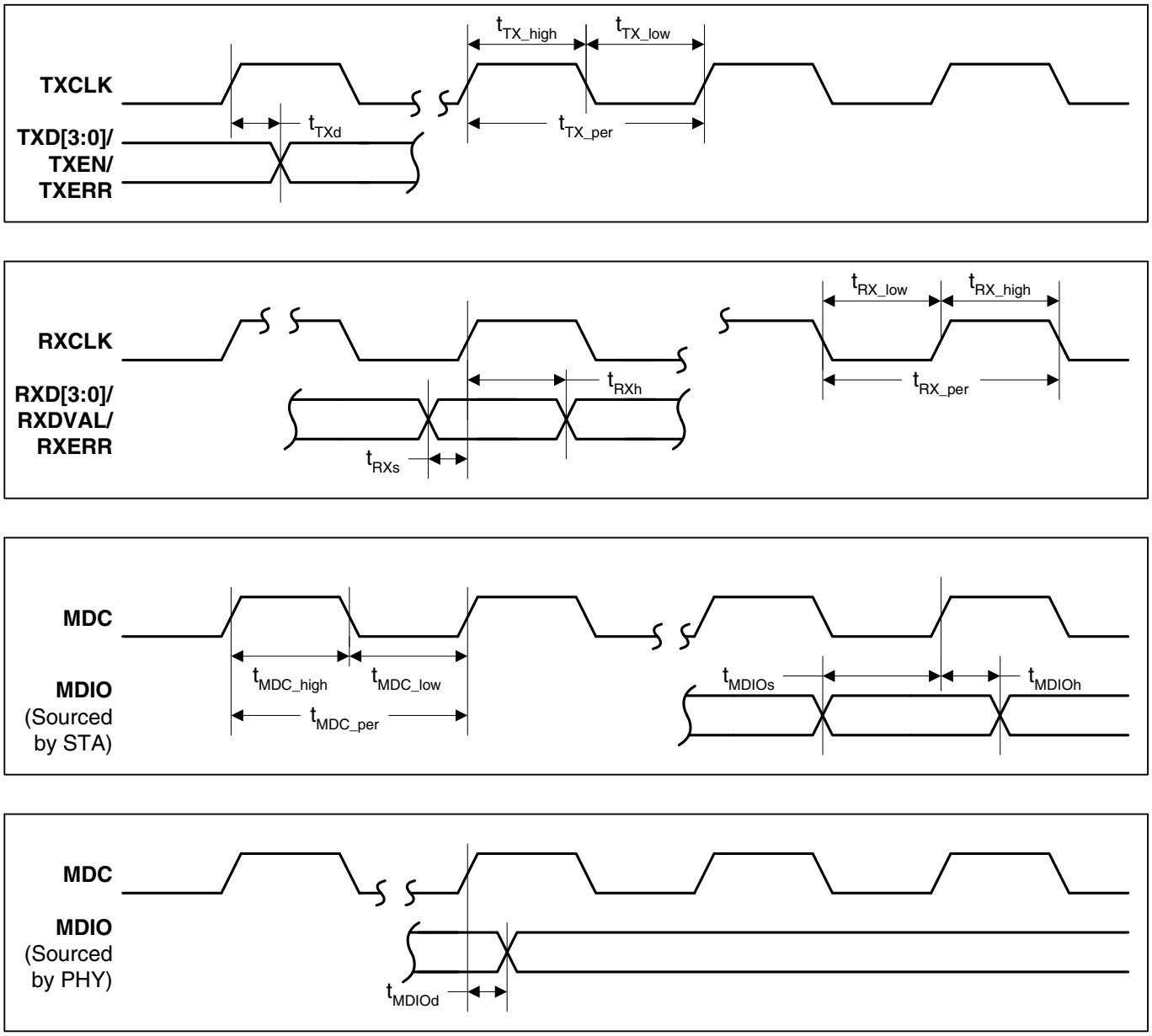


Figure 17. Ethernet MAC Timing Measurement

Audio Interface

The following table contains the values for the timings of each of the SPI modes.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	tspix_clk	-	ns
SCLK high time	t_{clk_high}	-	(tspix_clk) / 2	-	ns
SCLK low time	t_{clk_low}	-	(tspix_clk) / 2	-	ns
SCLK rise/fall time	t_{clkrf}	1	-	8	ns
Data from master valid delay time	t_{DMd}	-	-	3	ns
Data from master setup time	t_{DMs}	20	-	-	ns
Data from master hold time	t_{DMh}	40	-	-	ns
Data from slave setup time	t_{DSs}	20	-	-	ns
Data from slave hold time	t_{DSh}	40	-	-	ns

Note: The tspix_clk is programmable by the user.

Texas Instruments' Synchronous Serial Format

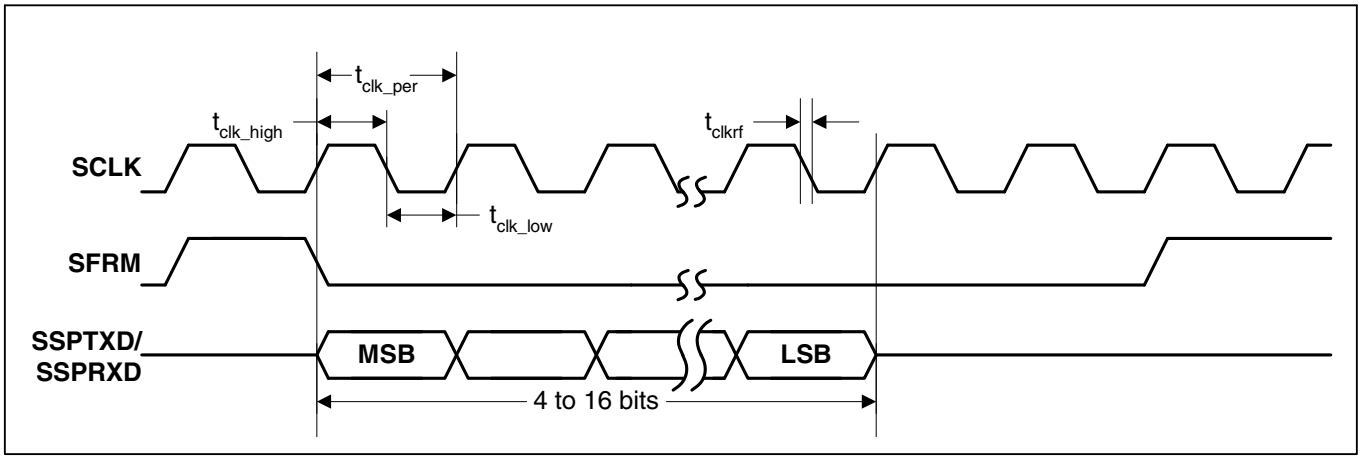


Figure 18. *TI* Single Transfer Timing Measurement

Microwire

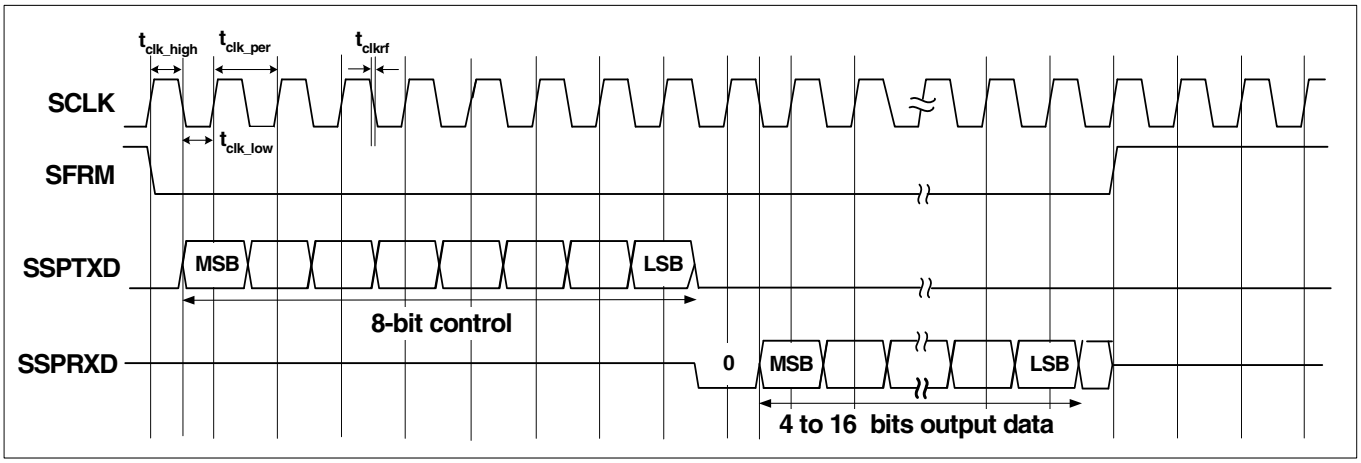


Figure 19. Microwire Frame Format, Single Transfer

Figure 27. 272 Pin TFBGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
U	NC	NC	P[8]	P[4]	P[1]	DA[6]	DA[3]	AD[10]	DA[0]	TDO	NC	SCLK[1]	SSPRX[1]	INT[1]	RTSn	USBm[1]	NC	U
T	NC	NC	V_CSYNC	P[7]	P[2]	DA[7]	AD[11]	AD[9]	DSRn	TMS	gndr	SFRM[1]	INT[2]	INT[0]	USBp[1]	NC	NC	T
R	P[9]	HSYNC	P[6]	P[5]	P[0]	AD[14]	DA[4]	DA[1]	DTRn	TDI	BOOT[0]	ASYNC	SSPTX[1]	PWMOUT	USBm[0]	ABITCLK	USBp[0]	R
P	SPCLK	P[10]	P[11]	P[3]	AD[15]	AD[13]	AD[12]	DA[2]	AD[8]	TCK	BOOT[1]	EEDAT	GRLED	RDLED	GGPIO[2]	RXD[1]	RXD[2]	P
N	P[14]	P[16]	P[15]	P[13]	P[12]	DA[5]	vddr	vddr	vddr	vddr	EECLK	ASDO	CTSn	RXD[0]	TXD[0]	TXD[1]	TXD[2]	N
M	BRIGHT	AD[0]	DQMn[1]	DQMn[2]	P[17]	gndr	gndr	vddc	vddc	gndr	gndr	ROW[6]	ROW[4]	ROW[1]	ROW[0]	ROW[3]	ROW[2]	M
L	DA[9]	AD[2]	AD[1]	DA[8]	BLANK	gndr						gndr	ROW[7]	ROW[5]	PLL_GND	XTALI	XTALO	L
K	AD[4]	DA[12]	DA[10]	DA[11]	vddr	gndr		gndc	gndc	gndc		vddc	COL[4]	PLL_VDD	COL[2]	COL[1]	COL[0]	K
J	AD[6]	DA[14]	AD[7]	DA[13]	vddr	vddc		gndc		gndc		vddc	vddr	COL[5]	COL[6]	CSn[0]	COL[3]	J
H	DA[18]	DA[20]	DA[19]	DA[16]	vddr	vddc		gndc	gndc	gndc		gndr	vddr	EGPIO[8]	PRSTn	COL[7]	RSTOn	H
G	DQMn[0]	CASn	DA[21]	AD[22]	vddr	gndr						gndr	EGPIO[9]	EGPIO[10]	EGPIO[11]	RTCXTALO	RTCXTALI	G
F	RASn	SDCSn[1]	SDCSn[0]	DQMn[3]	AD[5]	gndr	gndr	gndr	vddc	vddc	gndr	EGPIO[7]	EGPIO[5]	ADC_GND	EGPIO[6]	sYm	sYp	F
E	SDCSn[2]	SDWEN	DA[22]	AD[3]	DA[15]	AD[21]	DA[17]	vddr	vddr	vddr	MIIRXD[0]	TXERR	EGPIO[2]	EGPIO[4]	EGPIO[3]	sXp	sXm	E
D	SDCSn[3]	DA[23]	SDCLK	DA[24]	HGPIO[7]	HGPIO[6]	DA[28]	HGPIO[4]	AD[16]	MDC	RXERR	MIITXD[3]	EGPIO[12]	EGPIO[1]	EGPIO[0]	Ym	Yp	D
C	AD[23]	DA[26]	CSn[3]	DA[25]	AD[24]	AD[19]	HGPIO[5]	WRn	MDIO	MIIRXD[2]	TXCLK	MIITXD[0]	CLD	EGPIO[13]	TRSTn	Xp	Xm	C
B	AD[25]	CSn[2]	CSn[6]	AD[20]	DA[30]	AD[18]	HGPIO[3]	AD[17]	RXCLK	MIIRXD[1]	MIITXD[2]	TXEN	FGPIO[5]	EGPIO[15]	USBp[2]	ARSTn	ADC_VDD	B
A	CSn[1]	CSn[7]	SDCLKEN	DA[31]	DA[29]	DA[27]	HGPIO[2]	RDn	MIIRXD[3]	RXDVAL	MIITXD[1]	CRS	FGPIO[7]	FGPIO[0]	WAITn	USBm[2]	ASDI	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Pin List

The following Thin-profile Fine-pitch Ball Grid Array (TFBGA) ball assignment table is sorted in order of ball.

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	CSn[1]	E1	SDCSn[2]	J10	gndc	P1	SPCLK
A2	CSn[7]	E2	SDWEN	J12	vddc	P2	P[10]
A3	SDCLKEN	E3	DA[22]	J13	vddr	P3	P[11]
A4	DA[31]	E4	AD[3]	J14	COL[5]	P4	P[3]
A5	DA[29]	E5	DA[15]	J15	COL[6]	P5	AD[15]
A6	DA[27]	E6	AD[21]	J16	CSn[0]	P6	AD[13]
A7	HGPIO[2]	E7	DA[17]	J17	COL[3]	P7	AD[12]
A8	RDn	E8	vddr	K1	AD[4]	P8	DA[2]
A9	MIIRXD[3]	E9	vddr	K2	DA[12]	P9	AD[8]
A10	RXDVAL	E10	vddr	K3	DA[10]	P10	TCK
A11	MIITXD[1]	E11	MIIRXD[0]	K4	DA[11]	P11	BOOT[1]
A12	CRS	E12	TXERR	K5	vddr	P12	EEDAT
A13	FGPIO[7]	E13	EGPIO[2]	K6	gndr	P13	GRLED
A14	FGPIO[0]	E14	EGPIO[4]	K8	gndc	P14	RDLED
A15	WAITn	E15	EGPIO[3]	K9	gndc	P15	GGPIO[2]
A16	USBm[2]	E16	sXp	K10	gndc	P16	RXD[1]
A17	ASDI	E17	sXm	K12	vddc	P17	RXD[2]
B1	AD[25]	F1	RASn	K13	COL[4]	R1	P[9]
B2	CSn[2]	F2	SDCSn[1]	K14	PLL_VDD	R2	HSYNC
B3	CSn[6]	F3	SDCSn[0]	K15	COL[2]	R3	P[6]
B4	AD[20]	F4	DQMn[3]	K16	COL[1]	R4	P[5]
B5	DA[30]	F5	AD[5]	K17	COL[0]	R5	P[0]
B6	AD[18]	F6	gndr	L1	DA[9]	R6	AD[14]
B7	HGPIO[3]	F7	gndr	L2	AD[2]	R7	DA[4]
B8	AD[17]	F8	gndr	L3	AD[1]	R8	DA[1]
B9	RXCLK	F9	vddc	L4	DA[8]	R9	DTRn
B10	MIIRXD[1]	F10	vddc	L5	BLANK	R10	TDI
B11	MIITXD[2]	F11	gndr	L6	gndr	R11	BOOT[0]
B12	TXEN	F12	EGPIO[7]	L12	gndr	R12	ASYNC
B13	FGPIO[5]	F13	EGPIO[5]	L13	ROW[7]	R13	SSPTX[1]
B14	EGPIO[15]	F14	ADC_GND	L14	ROW[5]	R14	PWMOUT
B15	USBp[2]	F15	EGPIO[6]	L15	PLL_GND	R15	USBm[0]
B16	ARSTn	F16	sYm	L16	XTALI	R16	ABITCLK
B17	ADC_VDD	F17	sYp	L17	XTALO	R17	USBp[0]
C1	AD[23]	G1	DQMn[0]	M1	BRIGHT	T1	NC
C2	DA[26]	G2	CASn	M2	AD[0]	T2	NC
C3	CSn[3]	G3	DA[21]	M3	DQMn[1]	T3	V_CSYNC
C4	DA[25]	G4	AD[22]	M4	DQMn[2]	T4	P[7]
C5	AD[24]	G5	vddr	M5	P[17]	T5	P[2]
C6	AD[19]	G6	gndr	M6	gndr	T6	DA[7]
C7	HGPIO[5]	G12	gndr	M7	gndr	T7	AD[11]
C8	WRn	G13	EGPIO[9]	M8	vddc	T8	AD[9]

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Table S. Pin Descriptions

Pin Name	Block	Pad Type	Pull Type	Description
TCK	JTAG	I	PD	JTAG clock in
TDI	JTAG	I	PD	JTAG data in
TDO	JTAG	4ma	-	JTAG data out
TMS	JTAG	I	PD	JTAG test mode select
TRSTn	JTAG	I	PD	JTAG reset
BOOT[1:0]	System	I	PD	Boot mode select in
XTALI	PLL	A	-	Main oscillator input
XTALO	PLL	A	-	Main oscillator output
VDD_PLL	PLL	P	-	Main oscillator power, 1.8V
GND_PLL	PLL	G	-	Main oscillator ground
RTCXTALI	RTC	A	-	RTC oscillator input
RTCXTALO	RTC	A	-	RTC oscillator output
WRn	EBUS	4ma	-	SRAM Write strobe out
RDn	EBUS	4ma	-	SRAM Read/OE strobe out
WAITn	EBUS	I	PU	SRAM Wait in
AD[25:0]	EBUS	8ma	-	Shared Address bus out
DA[31:0]	EBUS	8ma	PU	Shared Data bus in/out
CSn[3:0]	EBUS	4ma	PU	Chip select out
CSn[7:6]	EBUS	4ma	PU	Chip select out
DQMn[3:0]	EBUS	8ma	-	Shared data mask out
SDCLK	SDRAM	8ma	-	SDRAM clock out
SDCLKEN	SDRAM	8ma	-	SDRAM clock enable out
SDCSn[3:0]	SDRAM	4ma	-	SDRAM chip selects out
RASn	SDRAM	8ma	-	SDRAM RAS out
CASn	SDRAM	8ma	-	SDRAM CAS out
SDWEn	SDRAM	8ma	-	SDRAM write enable out
P[17:0]	Raster	4ma	PU	Pixel data bus out
SPCLK	Raster	12ma	PU	Pixel clock in/out
HSYNC	Raster	8ma	PU	Horizontal synchronization/ line pulse out
V_CSYNC	Raster	8ma	PU	Vertical or composite synchronization/frame pulse out
BLANK	Raster	8ma	PU	Composite blanking signal out
BRIGHT	Raster	4ma	-	PWM brightness control out
PWMOUT	PWM	8ma		Pulse width modulator output
Xp, Xm	ADC	A	-	Touchscreen ADC X axis
Yp, Ym	ADC	A	-	Touchscreen ADC Y axis
sXp, sXm	ADC	A	-	Touchscreen ADC X axis feedback
sYp, sYm	ADC	A	-	Touchscreen ADC Y axis feedback
VDD_ADC	ADC	P	-	Touchscreen ADC power, 3.3V
GND_ADC	ADC	G	-	Touchscreen ADC ground
COL[7:0]	Key	8ma	PU	Key matrix column inputs
ROW[7:0]	Key	8ma	PU	Key matrix row outputs
USBp[2:0]	USB	A	-	USB positive signals
USBm[2:0]	USB	A	-	USB negative signals
TXD0	UART1	4ma	-	Transmit out
RXD0	UART1	I	PU	Receive in
CTSn	UART1	I	PU	Clear to send/transmit enable
DSRn	UART1	I	PU	Data set ready/Data Carrier Detect

Table S. Pin Descriptions *(Continued)*

Pin Name	Block	Pad Type	Pull Type	Description
DTRn	UART1	4ma	-	Data Terminal Ready output
RTSn	UART1	4ma	-	Ready to send
TXD1	UART2	4ma	-	Transmit/IrDA output
RXD1	UART2	I	PU	Receive/IrDA input
TXD2	UART3	4ma	-	Transmit
RXD2	UART3	I	PU	Receive
MDC	EMAC	4ma		Management data clock
MDIO	EMAC	4ma	PU	Management data input/output
RXCLK	EMAC	I	PD	Receive clock in
MIIRXD[3:0]	EMAC	I	PD	Receive data in
RXDVAL	EMAC	I	PD	Receive data valid
RXERR	EMAC	I	PD	Receive data error
TXCLK	EMAC	4ma	PU	Transmit clock in
MIITXD[3:0]	EMAC	I	PD	Transmit data out
TXEN	EMAC	4ma	PD	Transmit enable
TXERR	EMAC	4ma	PD	Transmit error
CRS	EMAC	I	PD	Carrier sense
CLD	EMAC	I	PU	Collision detect
GRLED	LED	12ma	-	Green LED
RDLED	LED	12ma	-	Red LED
EECLK	EEPROM	4ma	PU	EEPROM/Two-wire Interface clock
EEDAT	EEPROM	4ma	PU	EEPROM/Two-wire Interface data
ABITCLK	AC97	8ma	PD	AC97 bit clock
ASYNC	AC97	8ma	PD	AC97 frame sync
ASDI	AC97	I	PD	AC97 Primary input
ASDO	AC97	8ma	PU	AC97 output
ARSTn	AC97	8ma	-	AC97 reset
SCLK1	SPI1	8ma	PD	SPI bit clock
SFRM1	SPI1	8ma	PD	SPI Frame Clock
SSPRX1	SPI1	I	PD	SPI input
SSPTX1	SPI1	8ma	-	SPI output
INT[2:0]	INT	I	PD	External interrupts
PRSTn	Syscon	I	PU	Power on reset
RSTOn	Syscon	4ma	-	User Reset in out - open drain
EGPIO[15]	GPIO	I/O, 4ma	PU	Enhanced GPIO
EGPIO[13:0]	GPIO	I/O, 4ma	PU	Enhanced GPIO
FGPIO[7, 5, 0]	GPIO	I/O, 8ma	PU	GPIO
GGPIO[2]	GPIO	I/O, 8ma	PU	GPIO
HGPIO[7:2]	GPIO	I/O, 8ma	PU	GPIO
vddc	Power	P	-	Digital power, 1.8V
vddr	Power	P	-	Digital power, 3.3V
gndc	Ground	G	-	Digital ground
gndr	Ground	G	-	Digital ground

Table T illustrates the pin signal multiplexing and configuration options.

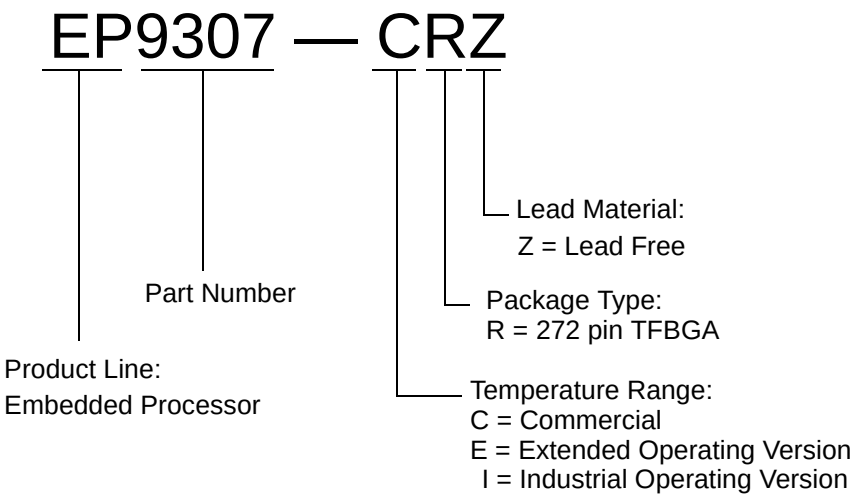
Table T. Pin Multiplex Usage Information

Physical Pin Name	Description	Multiplex signal name
COL[7:0]	GPIO	GPIO Port D[7:0]
ROW[7:0]	GPIO	GPIO Port C[7:0]
EGPIO[0]	Ring Indicator Input	RI
EGPIO[1]	1Hz clock monitor	CLK1HZ
EGPIO[2]	DMA request	DMARQ
EGPIO[3]	HDLC Clock	HDLCCLK1
EGPIO[4]	I2S Transmit Data 1	SDO1
EGPIO[5]	I2S Receive Data 1	SDI1
EGPIO[6]	I2S Transmit Data 2	SDO2
EGPIO[7]	DMA Request 0	DREQ0
EGPIO[8]	DMA Acknowledge 0	DACK0
EGPIO[9]	DMA EOT 0	DEOT0
EGPIO[10]	DMA Request 1	DREQ1
EGPIO[11]	DMA Acknowledge 1	DACK1
EGPIO[12]	DMA EOT 1	DEOT1
EGPIO[13]	I2S Receive Data 2	SDI2
EGPIO[15]	Device active / present	DASP
ABITCLK	I2S Serial clock	SCLK
ASYNC	I2S Frame Clock	LRCK
ASDO	I2S Transmit Data 0	SDO0
ASDI	I2S Receive Data 0	SDI0
ARSTn	I2S Master clock	MCLK
SCLK1	I2S Serial clock	SCLK
SFRM1	I2S Frame Clock	LRCK
SSPTX1	I2S Transmit Data 0	SDO0
SSPRX1	I2S Receive Data 0	SDI0

ORDERING INFORMATION

The order numbers for the device are:

EP9307-CRZ	0°C to +70°C	272 pin TFBGA	Lead Free
EP9307-IRZ	-40°C to +85°C	272 pin TFBGA	Lead Free



Note: Go to the Cirrus Logic Internet site at http://www.cirrus.com to find contact information for your local sales representative.